Real-Time Hyperspectral Signal Processing and Classification

2025 Midterm Presentation

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Overview

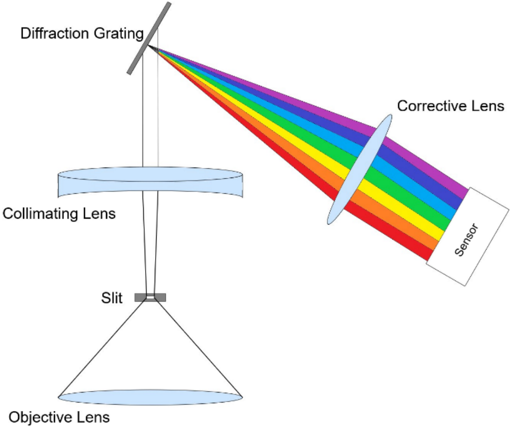
- Our goal is to implement real-time hyperspectral classification. This means that our model would be integrated with the data-collection process so that there is no need to handle large amounts of data after collection.
  - Currently it is often the case that large amounts of hyperspectral data will be collected in the field, then need to be processed seperately before any results can be acted upon.
- This naturally means that the main goal of our project is to minimize the latency of the classification process so it matches the pace of data collection.

Motivation

Real-time classification would provide immediate insight to field workers, allowing them to make important decisions quickly.

Background: Hyperspectral Imaging (HSI)

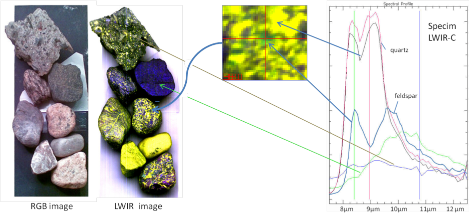
- HSI uses diffraction to sample a continuous range of spectral bands.
- Because of its high dimensionality, hyperspectral data tends to be large and difficult to process.
    - A typical RGB image has 3 channels. Our sensor uses 1604. 535x larger.

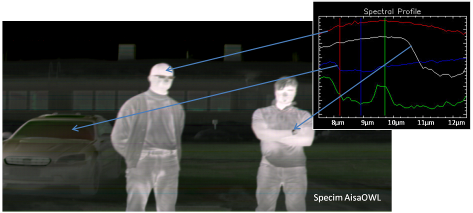


Left image: [1]
Right image: [11]

Background: HSI for Classification

- Hyperspectral imaging data can be used to classify objects in images. Their high wavelength spectrum makes them especially useful for environmental monitoring, agriculture, and more.
- For our project, we're interested in identifying regions of forests with an adbundance of bio-fuel which puts them at risk of forest-fires.

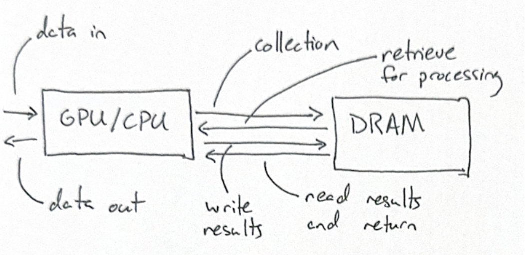


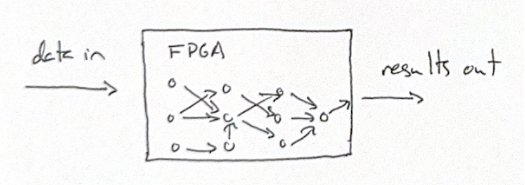


Top image: [2]
Bottom image: [3]

Background: FPGAs

- An FPGA (Field Programmable Gate Array) is a programmable circuit.
- They are built out of logic elements, DSP slices (for performing simple addition and multiplication), and local memory (consisting of static RAM).
- They consist of a 'fabric' of resources where everything is interconnected (hence programmable).





Research Question

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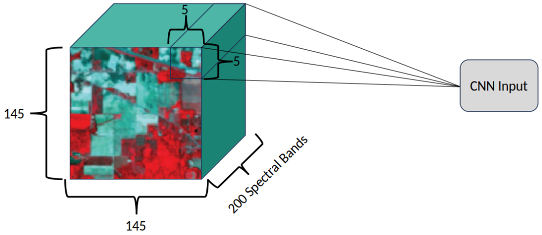
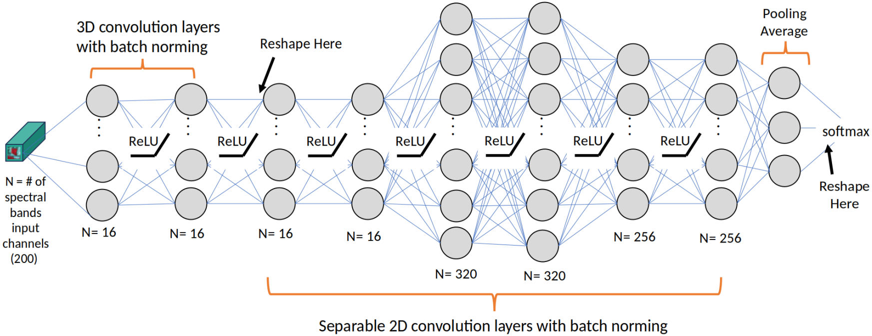
How much can different neural network model architectures for classifying hyperspectral data improve latency in an FPGA implementation without sacrificing accuracy?

Baseline

- Previous work at MSU successfully reduced band dimension on a HSI dataset and performed high accuracy classification on it.
- 99.7% accuracy using a large convolutional neural network.
- Performs roughly 2 billion elementary add/multiply operations for each pixel classified.





Both images: [6]

CNN Drawbacks

- A CNN allows us to gain spatial information about our image by taking into account pixels around each pixel
  - For real time classification, this requires storing data so our kernel can pass over it, interrupting the flow of data through our FPGA
- The CNN implementations are also quite large and might not be viable for our hardware needs.

Kolmogorov Arnold Networks (KAN)

- Directly learns the nonlinear activation functions of a network.
- In an FPGA, these functions could be encoded directly as lookup tables, allowing us to approximate results much more quickly.
- If pixel-classification is viable, we can avoid storing/transferring data from memory for a CNN kernel.

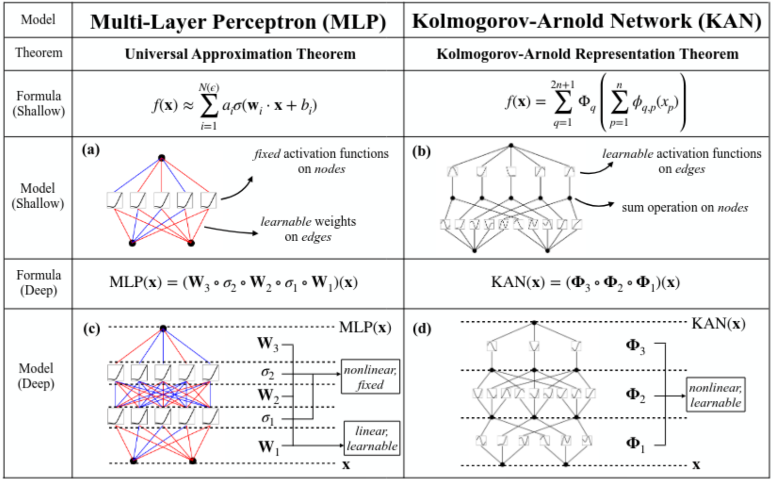


Figure 0.1: Multi-Layer Perceptrons (MLPs) vs. Kolmogorov-Arnold Networks (KANs)

Image: [7]

Work Done

- To properly benchmark and implement, we need to shift the models from the high level and opaque python implementations to something lower level.
- To do this, I transferred both the baseline CNN implementation and the KAN to C (for the latter, I created a custom C library that can be called directly from python).
  - This allows us to do preliminary benchmarking and provides an interface to swap out the computational parts of the classification directly to the FPGAs.
  - This process will likely form the basis of the rest of my work at the REU.

Concerns

- Despite the suitability of FPGAs for this task, could it be the case that GPUs are simply so good at ML tasks that the latency overhead wouldn't matter?

Highlights

- I've enjoyed looking into ML implementations at a lower level and I'm excited to begin swapping out some of my implementations with real FPGA hardware.

Summary

Our goal is to achieve real-time HSI classification using a custom FPGA implementation. The real-time nature of this implementation would be highly useful for field work and real applications, but requires overcoming engineering challenges related to our hardware.

Acknowledgements

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- I would also like to thank Nat Sweeney, Zackery Backman, and Dirk Kaiser for the work that they have done and continue to do on the project.

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