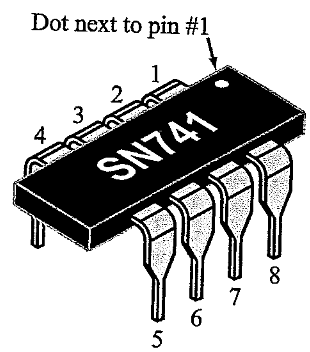
C H A P T E R

Operational Amplifiers

Contents



The introduction of the IC *operational amplifier* in the 1960s has led to the development of a wide array of *signal processing circuits*, enabling the creation of an ever-increasing number of *electronic applications*.

Objectives

Learn to:

- Describe the basic properties of an op amp and state the constraints of the ideal op-amp model.
- Explain the role of negative feedback and the tradeoff between circuit gain and dynamic range.
- Analyze and design inverting amplifiers, summing amplifiers, difference amplifiers, and voltage followers.
- Combine multiple op-amp circuits together to perform signal processing operations.
- Analyze and design high-gain, high-sensitivity instrumentation amplifiers.
- Design an n-bit digital-to-analog converter.
- Use the MOSFET in analog and digital circuits.
- Apply Multisim to analyze and simulate circuits that include op amps.

Overview

Since its first realization by Bob Widlar in 1963 and then its introduction by Fairchild Semiconductor in 1968, the *operational amplifier*, or *op amp* for short, has become the workhorse of many signal-processing circuits. It acquired the adjective *operational* because it is a versatile device capable not only of amplifying a signal but also inverting it (reversing its polarity), integrating it, or differentiating it. When multiple signals are connected to its input, the op amp can perform additional mathematical operations—including addition and subtraction. Consequently, op-amp circuits often are cascaded together in various arrangements to support a variety of different applications. In this chapter, we will explore several op-amp circuit configurations, including amplifiers, summers, voltage followers, and digital-to-analog converters.

4-1 Op-Amp Characteristics

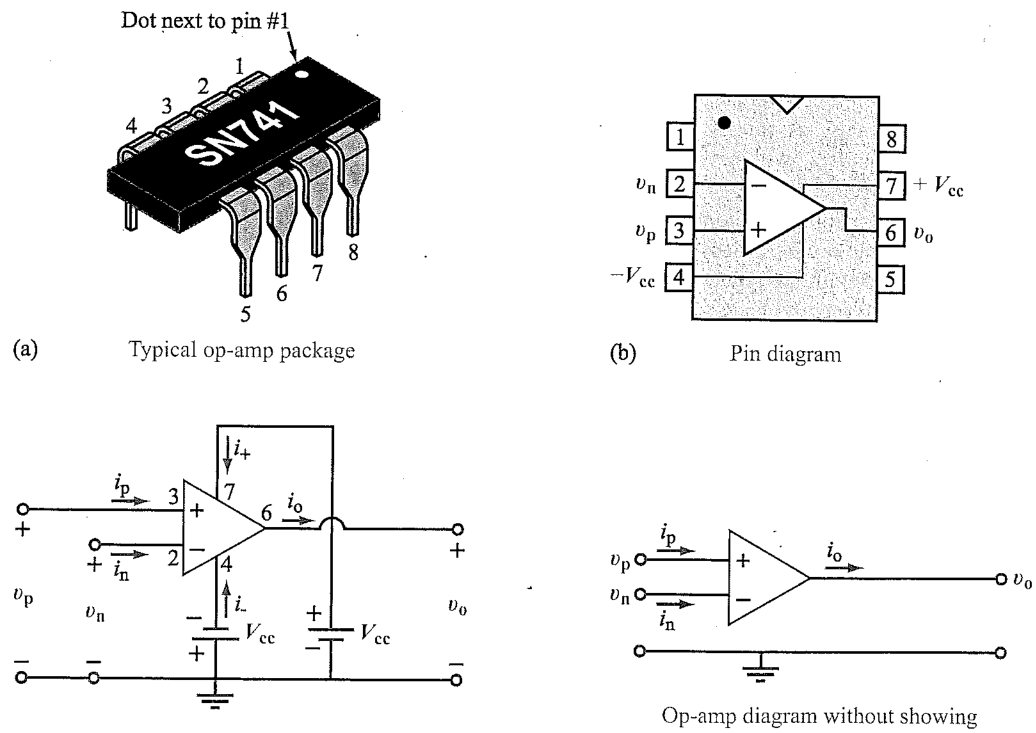
The internal architecture of an op-amp circuit consists of many interconnected transistors, diodes, resistors and capacitors—all fabricated on a chip of silicon. Despite its internal complexity, however, *an op amp can be modeled in terms of a relatively simple equivalent circuit that exhibits a* ***linear*** *input-output response.* This equivalence allows us to apply the tools we developed in the preceding chapters to analyze (as well as design) a large array of op-amp circuits and to do so with relative ease.

4-1.1 Nomenclature

Commercially available op amps are fabricated in encapsulated packages of various shapes. A typical example is the eight-pin *DIP configuration* shown in Fig. 4-1(a) [DIP stands for dual-in-line package]. The pin diagram for the op amp is shown in Fig. 4-1(b), and its circuit symbol (the triangle) is displayed in Fig. 4-1(c). Of the eight pins (terminals) only five need to be connected to an outside circuit, namely:

Op-Amp Pin Designation

Pin 2	inverting (or *negative*) input voltage, v_n
Pin 3	noninverting (or *positive*) input voltage, v_p
Pin 4	negative (−) terminal of power supply V_{cc}
Pin 7	positive (+) terminal of power supply V_{cc}
Pin 6	output voltage, v_o



(a) Typical op-amp package

(b) Pin diagram

(c) Complete circuit diagram

(d) Op-amp diagram without showing V_{cc} sources explicitly

Figure 4-1: Operational amplifier.

The op amp has two input voltage terminals (v_p and v_n) and one output voltage terminal (v_o).

> ▶ The terms ***noninverting*** and ***inverting*** are associated with the property of the op amp that its output voltage v_o is directly proportional to both the noninverting input voltage v_p and the negative of the inverting input voltage v_n. ◀

Kirchhoff's current law applies to any volume of space, including an op amp. Hence, for the five terminals connected to the op amp, KCL mandates that

$$i_o = i_p + i_n + i_+ + i_-, \tag{4.1}$$

where i_p, i_n, and i_o may be constant (dc) or time-varying currents. Currents i_+ and i_- are dc currents generated by the dc power supply V_{cc}.

> ▶ From here on forward, *we will ignore the pins connected to V_{cc} when we draw circuit diagrams involving op amps, because so long as the op amp is operated in its linear region, V_{cc} will have no bearing on the operation of the circuit.* ◀

Hence, in the future, the op-amp triangle usually will be drawn with only three terminals, as shown in Fig. 4-1(d). Moreover, voltages v_p, v_n, and v_o will be defined relative to a common reference or ground. The (+) and (−) labels printed on the op-amp triangle simply denote the noninverting and inverting pins of the op amp not the polarities of v_p or v_n.

Ignoring the pins associated with the power-supply voltage V_{cc} does not mean we can ignore currents i_+ and i_-. To avoid making the mistake of writing a KCL equation on the basis of the simplified diagram given in Fig. 4-1(d), we explicitly state that fact by writing

$$i_o \neq i_p + i_n. \tag{4.2}$$

4-1.2 Transfer Characteristics

The plot shown in Fig. 4-2, which depicts the input-output voltage-transfer characteristic of the op amp, is divided into three regions of operation, denoted the ***negative saturation***, ***linear***, and ***positive saturation*** regions. In the linear region, the output voltage v_o is related to the input voltages v_p and v_n by

$$v_o = A(v_p - v_n), \tag{4.3}$$

where A is called the *op-amp gain*, or the *open-loop gain*. Strictly speaking, this relationship is valid only when the op

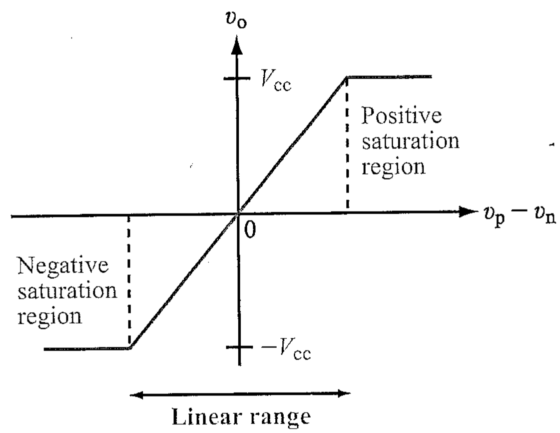


Figure 4-2: Op-amp transfer characteristics. The linear range extends between $v_o = -V_{cc}$ and $+V_{cc}$.

amp is not connected to an external circuit on the output side (open loop), but as will become clearer in future sections, it continues to hold (approximately) if the output circuit satisfies certain conditions. The open-loop gain is specific to the op-amp device itself, in contrast with the ***circuit gain*** or ***closed-loop gain***, G, which defines the gain of the entire circuit. Thus, if v_s is the signal voltage of the circuit connected at the input side of the op-amp circuit (Fig. 4-3), and v_L is the voltage across the load connected at its output side, then

$$v_L = G v_s. \tag{4.4}$$

According to Eq. (4.3), v_o is related linearly to the difference between v_p and v_n or to either one of them if the other is held constant. Excluding circuits that contain magnetically coupled transformers, in a regular circuit, no voltage can exceed the net voltage level of the power supply.

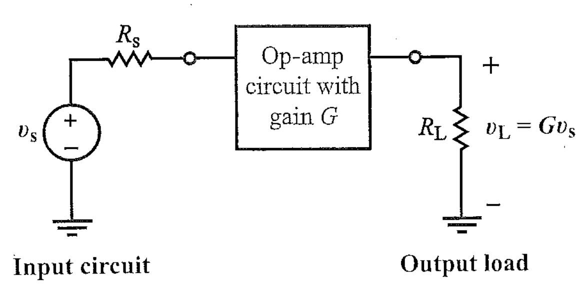


Figure 4-3: Circuit gain G is the ratio of the output voltage v_L to the signal input voltage v_s.

Table 4-1: Characteristics and typical ranges of op-amp parameters. The rightmost column represents the values assumed by the ideal op-amp model.

Op-Amp Characteristics	Parameter	Typical Range	Ideal Op Amp
• Linear input-output response	Open-loop gain A	10^4 to 10^8 (V/V)	∞
• High input resistance	Input resistance R_i	10^6 to 10^{13} Ω	∞ Ω
• Low output resistance	Output resistance R_o	1 to 100 Ω	0 Ω
• Very high gain	Supply voltage V_{cc}	5 to 24 V	As specified by manufacturer

▶ The maximum value that v_o can attain is $|V_{cc}|$. The op amp goes into a saturation mode if $|A(v_p - v_n)| > |V_{cc}|$, which can occur on both the negative and positive sides of the linear region. ◀

As we will discuss shortly, the op-amp gain A is typically on the order of 10^5 or greater, and the supply voltage is on the order of volts or tens of volts. In the linear region, v_o is bounded between $-V_{cc}$ and $+V_{cc}$, which means that $(v_p - v_n)$ is bounded between $-V_{cc}/A$ and $+V_{cc}/A$. For $V_{cc} = 10$ V and $A = 10^6$, the operating range of $(v_p - v_n)$ is -10 μV to $+10$ μV. It is important to keep this in mind as we deal with circuits containing operational amplifiers.

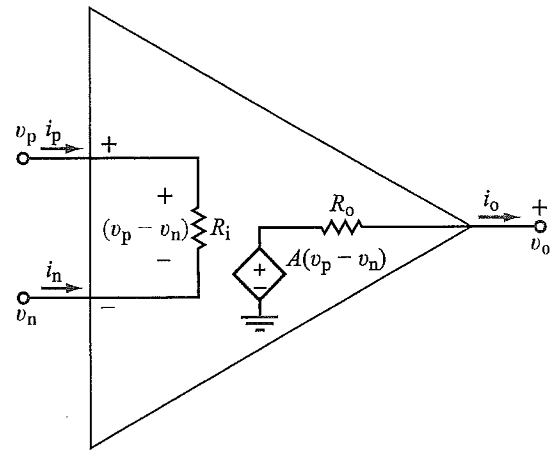


Figure 4-4: Equivalent circuit model for an op amp operating in the linear range. Voltages v_p, v_n, and v_o are referenced to ground.

4-1.3 Equivalent-Circuit Model

When operated in its linear region, the op-amp input-output behavior can be modeled in terms of the equivalent circuit shown in Fig. 4-4. The equivalent circuit consists of a voltage-controlled voltage source of magnitude $A(v_p - v_n)$, an input resistance R_i, and an output resistance R_o. Table 4-1 lists the typical range of values that each of these op-amp parameters may assume. Based on these values, we note that an op amp is characterized by:

(1) *High input resistance* R_i: at least 1 MΩ, which is highly desirable from the standpoint of voltage transfer from an input circuit (as discussed previously in Section 3-6).

(2) *Low output resistance* R_o: which is desirable from the standpoint of transfering the op-amp's output voltage to a load circuit.

(3) *High voltage gain* A: which is the key, as we will see later, to allowing us to further simplify the equivalent circuit into an "ideal" op-amp model with infinite gain.

Example 4-1: Noninverting Amplifier

The circuit shown in Fig. 4-5 uses an op amp to amplify the input signal voltage v_s. Obtain an expression for the circuit gain $G = v_o/v_s$, and then evaluate it for $V_{cc} = 10$ V, $A = 10^6$, $R_i = 10$ MΩ, $R_o = 10$ Ω, $R_1 = 80$ kΩ, and $R_2 = 20$ kΩ.

Solution: For reference purposes, we label the output as terminal a and the node from which a current is fed back into the op amp as terminal b. The current i_3 flowing from terminal b to terminal a is the same as the current i_4 flowing from terminal a towards R_o. When expressed in terms of node voltages, the equality $i_3 = i_4$ gives

$$\frac{v_n - v_o}{R_1} = \frac{v_o - A(v_p - v_n)}{R_o} \quad \text{(node } a\text{)}. \tag{4.5}$$

At node b, KCL gives $i_1 + i_2 + i_3 = 0$ or

$$\frac{v_n - v_p}{R_i} + \frac{v_n}{R_2} + \frac{v_n - v_o}{R_1} = 0. \quad \text{(node } b\text{)}. \tag{4.6}$$

Additionally,

$$v_p = v_s. \tag{4.7}$$

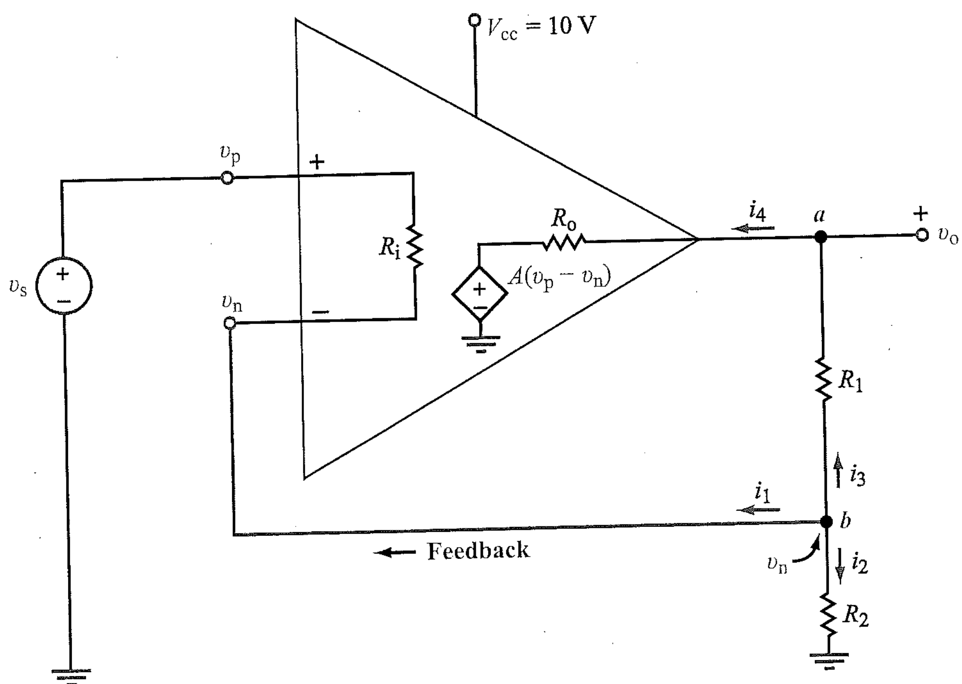


Figure 4-5: Noninverting amplifier circuit of Example 4-1.

Solution of these simultaneous equations leads to the following expression for the circuit gain G:

$$G = \frac{v_o}{v_s} = \frac{[AR_i(R_1 + R_2) + R_2R_o]}{AR_2R_i + R_o(R_2 + R_i) + R_1R_2 + R_i(R_1 + R_2)}. \tag{4.8}$$

For $V_{cc} = 10$ V, $A = 10^6$, $R_i = 10^7$ Ω, $R_o = 10$ Ω, $R_1 = 80$ kΩ, and $R_2 = 20$ kΩ, we have

$$G = \frac{v_o}{v_s} = 4.999975 \approx 5.0. \tag{4.9}$$

In the expression for G, the two parameters A and R_i are several orders of magnitude larger than all of the others. Also, R_o is in series with R_1, which is 8000 times larger. Hence, we would incur minimal error if we let $A \to \infty$, $R_i \to \infty$, and $R_o \to 0$, in which case the expression for G reduces to

$$G \approx \frac{R_1 + R_2}{R_2} \quad \text{(ideal op-amp model).} \tag{4.10}$$

This approximation, based on the ideal op-amp model that will be introduced in Section 4-3, gives

$$G = \frac{80 \text{ k}\Omega + 20 \text{ k}\Omega}{20 \text{ k}\Omega} = 5.$$

Concept Question 4-1: How is the linear range of an op amp defined?

Concept Question 4-2: What is the difference between the op-amp gain A and the circuit gain G?

Concept Question 4-3: An op amp is characterized by three important input-output attributes. What are they?

Exercise 4-1: In the circuit of Example 4-1 shown in Fig. 4-5, insert a series resistance R_s between v_s and v_p and then repeat the solution to obtain an expression for G. Evaluate G for $R_s = 10$ Ω and use the same values listed in Example 4-1 for the other quantities. What impact does the insertion of R_s have on the magnitude of G?

Answer:

$$G = \frac{[A(R_i + R_s)(R_1 + R_2) + R_2R_o]}{[AR_2(R_i + R_s) + R_o(R_2 + R_i + R_s) + R_1R_2 + (R_i + R_s)(R_1 + R_2)]}$$
$$= 4.999977 \quad \text{(negligible impact).}$$

(See)

4-2 Negative Feedback

Feedback refers to taking a part of the output signal and feeding it back into the input. It is called *positive feedback* if it increases the intensity of the input signal, and it is called *negative feedback* if it decreases it. Positive feedback causes the op amp to saturate, thereby forcing its output voltage υ_o to become equal to its supply voltage V_{cc}. This behavior is used to advantage in certain types of applications but they are outside the scope of this book. Negative feedback, on the other hand, is an essential ingredient of all of the op-amp circuits covered in this and forthcoming chapters.

Why do op-amp circuits need feedback and why negative feedback specifically? It seems counter-intuitive to want to decrease the input signal when the intent is to amplify it! We will answer this question by examining the circuit of Example 4-1 in some detail. To facilitate the discussion we have reproduced the circuit diagram (into a smaller version) and inserted it in Fig. 4-6(a).

When we say an op amp has a supply voltage V_{cc} of 10 V, we actually mean that a positive (10 V) dc voltage source is connected to pin 7 of its package and another, negative (−10 V) source is connected to its pin 4 [Fig. 4-1(b)]. The op-amp circuit cannot generate an output voltage υ_o that exceeds its supply voltage. Hence, υ_o is bounded to $\pm V_{cc}$ which means

$$|\upsilon_o| \leq V_{cc},$$

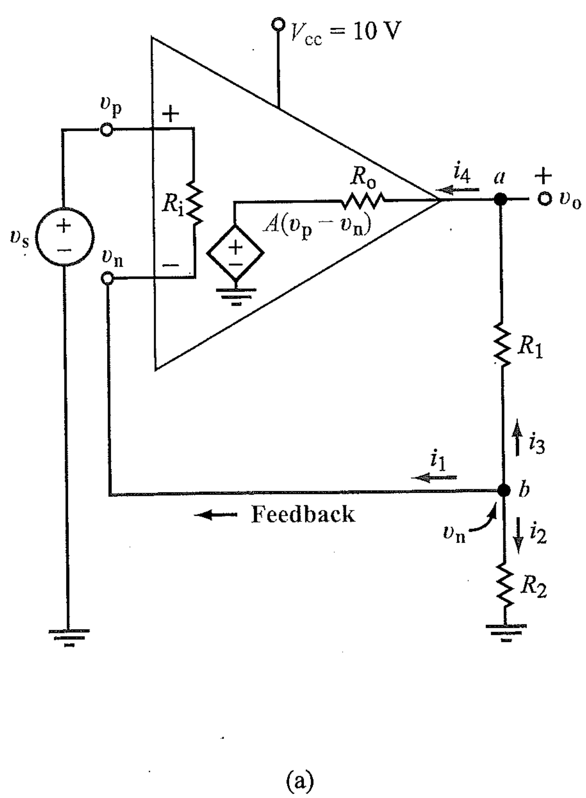
or equivalently,

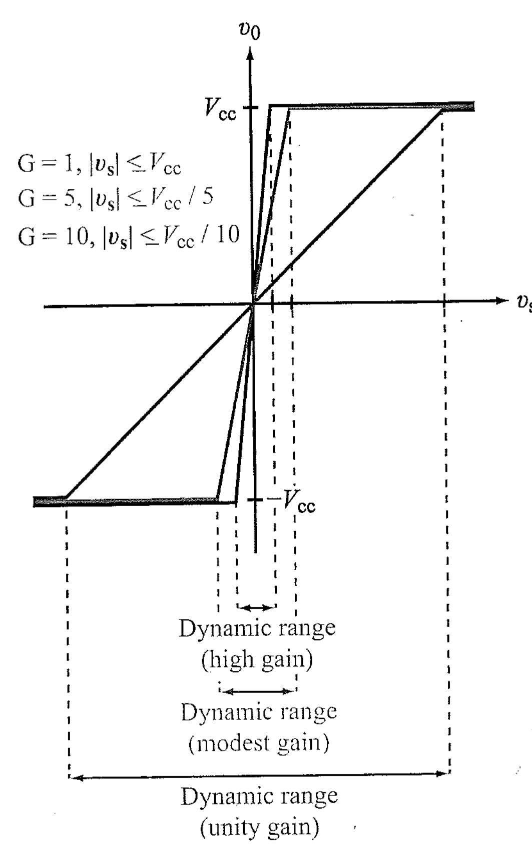
$$-V_{cc} \leq \upsilon_o \leq V_{cc}. \tag{4.11}$$

Thus, the *linear dynamic range* of υ_o extends from $-V_{cc}$ to $+V_{cc}$.

According to Example 4-1, υ_o is related to the signal voltage υ_s by

$$\upsilon_o = G\upsilon_s, \tag{4.12}$$





(b) Input-output transfer plots

Figure 4-6: Tradeoff between gain and dynamic range.

with

$$G \approx \frac{R_1 + R_2}{R_2} . \tag{4.13}$$

Inserting Eq. (4.12) into Eq. (4.11) gives

$$|G v_s| \le V_{cc}, \tag{4.14}$$

or

$$|v_s| \le \frac{V_{cc}}{G} , \tag{4.15}$$

which states that the linear dynamic range of v_s is inversely proportional to the circuit gain G.

(a) **Unity Gain:** If $R_2 = \infty$ [open circuit between node b and ground in the circuit of Fig. 4-6(a)], Eq. (4.13) gives $G \approx 1$. The corresponding dynamic range of v_s extends from $-V_{cc}$ to $+V_{cc}$, the same as the output. The input-output transfer plot relating v_o to v_s is displayed in green in Fig. 4-6(b).

(b) **Modest Gain:** If we choose $R_1/R_2 = 4$, Eq. (4.13) gives $G = 5$, and the dynamic range of v_s now extends from $-(10/15) = -2$V to $+2$ V. Thus, the gain is higher than the unity-gain case by a factor of 5, but the dynamic range of v_s is narrower by the same factor.

(c) **Maximum Gain:** If R_1 is removed (replaced with an open circuit between nodes a and b) and R_2 is set equal to zero (short circuit), no feedback will take place in the circuit of Fig. 4-6(a). Use of the exact expression for G given by Eq. (4.8) leads to $G = A$. Since $A = 10^6$, the absence of feedback provides a huge gain, but operationally v_s becomes limited to a very narrow range extending from $-10\ \mu$V to $+10\ \mu$V.

▶ Application of negative feedback offers a tradeoff between circuit gain and dynamic range. ◀

Concept Question 4-4: Why is negative feedback used in op-amp circuits?

Concept Question 4-5: How large is the circuit gain G in the absence of feedback? How large is it with 100 percent feedback [equivalent to setting $R_1 = 0$ in the circuit of Fig. 4-6(a)]?

Exercise 4-2: To evaluate the tradeoff between the circuit gain G and the linear dynamic range of v_s, apply Eq. (4.8) to find the magnitude of G and then determine the corresponding dynamic range of v_s for each of the following values of R_2: 0 (no feedback), 800 Ω, 8.8 kΩ, 40 kΩ, 80 kΩ, and 1 MΩ. Except for R_2, all other quantities remain unchanged.

Answer:

R_2	G	v_s Range
0	10^6	$-10\ \mu$V to $+10\ \mu$V
800 Ω	101	-99 mV to $+99$ mV
8.8 kΩ	10.1	-0.99 V to $+0.99$ V
40 kΩ	3	-3.3 V to $+3.3$ V
80 kΩ	2	-5 V to $+5$ V
1 MΩ	1.08	-9.26 V to $+9.26$ V

(See)

4-3 Ideal Op-Amp Model

We noted in Section 4-1 that the op amp has a very large input resistance R_i on the order of 10^7 Ω, a relatively small output resistance R_o on the order of 1–100 Ω, and an open-loop gain $A \approx 10^6$. Usually, the series resistances of the input circuit connected to terminals v_p and v_n are several orders of magnitude smaller than R_i. Consequently, not only will very little current flow through the input circuit, but also the voltage drop across the input-circuit resistors will be negligibly small in comparison with the voltage drop across R_i. These considerations allow us to simplify the equivalent circuit of the op amp by replacing it with the ideal op-amp circuit model shown in Fig. 4-7, in which R_i has been replaced with on open circuit. An open circuit between terminals v_p and v_n implies the following *ideal op-amp current constraint*:

$$i_p = i_n = 0 \quad \textbf{(ideal op-amp model).} \tag{4.16}$$

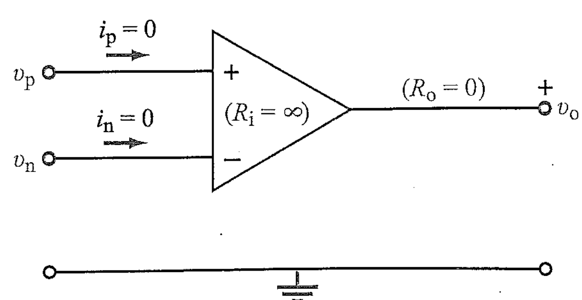


Figure 4-7: Ideal op-amp model.

In reality, i_p and i_n are very small but not identically zero; for if they were, there would be no amplification through the op amp. Nevertheless, the current condition given by Eq. (4.16) will prove quite useful.

Similarly, at the output side, if the load resistor connected in series with R_o is several orders of magnitude larger than R_o, then R_o can be ignored by setting it equal to zero. Finally, in the ideal op-amp model, the large open-loop gain A is made infinite—the consequence of which is that

$$\upsilon_p - \upsilon_n = \frac{\upsilon_o}{A} \to 0 \qquad \text{as } A \to \infty.$$

Hence, we obtain the ***ideal op-amp voltage constraint***

$$\upsilon_p = \upsilon_n \qquad \textbf{(ideal op-amp model).} \tag{4.17}$$

In summary:

▶ The ideal op-amp model characterizes the op amp in terms of an equivalent circuit in which $R_i = \infty$, $R_o = 0$, and $A = \infty$. ◀

The operative consequences are given by Eqs. (4.16) and (4.17) and in Table 4-2.

Table 4-2: Characteristics of the ideal op-amp model.

Ideal Op Amp	
• Current constraint	$i_p = i_n = 0$
• Voltage constraint	$\upsilon_p = \upsilon_n$
• $A = \infty$ $R_i = \infty$	$R_o = 0$

To illustrate the utility of the ideal op-amp model, let us re-examine the circuit we analyzed earlier in Example 4-1, but we will do so this time using the ideal model. The new circuit, as shown in Fig. 4-8, includes a source resistance R_s, but because the op amp draws no current ($i_p = 0$), there is no voltage drop across R_s. Hence,

$$\upsilon_p = \upsilon_s, \tag{4.18}$$

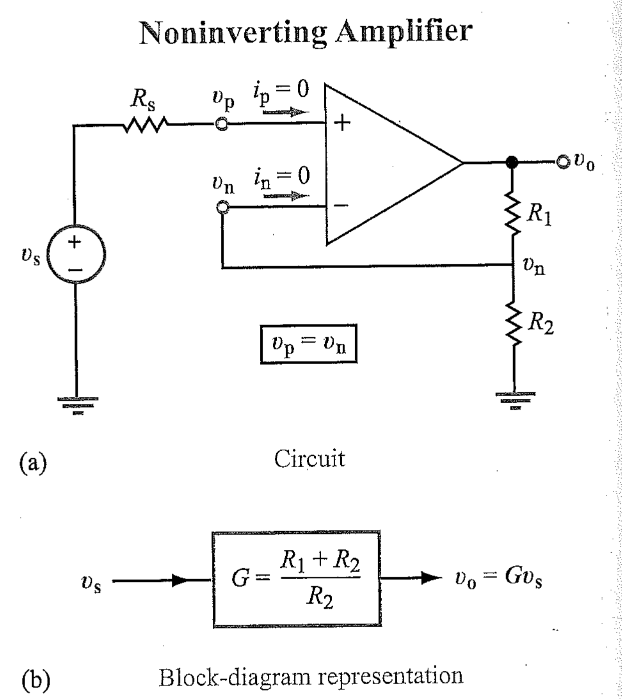


Figure 4-8: Noninverting amplifier circuit: (a) using ideal op-amp model and (b) equivalent block-diagram representation.

and on the output side, υ_o and υ_n are related through voltage division by

$$\upsilon_o = \left(\frac{R_1 + R_2}{R_2}\right)\upsilon_n. \tag{4.19}$$

Using these two equations, in conjunction with $\upsilon_p = \upsilon_n$ (from Eq. (4.17)), we end up with the following result for the circuit gain G:

$$G = \frac{\upsilon_o}{\upsilon_s} = \left(\frac{R_1 + R_2}{R_2}\right), \tag{4.20}$$

which is identical with Eq. (4.10).

▶ From here on forward, we will use the ideal op-amp model exclusively. ◀

The ***input resistance*** of the noninverting amplifier circuit shown in Fig. 4-8 is the Thévenin resistance of the op-amp circuit as seen by the input source υ_s. Because $i_p = 0$, it is easy to show that $R_{input} = R_i \approx \infty$, where R_i is the input resistance of the op amp (typically on the order of $10^9\ \Omega$).

Concept Question 4-6: What are the current and voltage constraints of the ideal op amp?

Concept Question 4-7: What are the values of the input and output resistances of the ideal op amp?

Concept Question 4-8: In the ideal op-amp model, R_o is set equal to zero. To satisfy such an approximation, does the load resistance need to be much larger or much smaller than R_o? Explain.

Exercise 4-3: Consider the noninverting amplifier circuit of Fig. 4-8(a) under the conditions of the ideal op-amp model. Assume $V_{cc} = 10$ V. Determine the value of G and the corresponding dynamic range of v_s for each of the following values of R_1/R_2: 0, 1, 9, 99, 10^3, 10^6.

Answer:

R_1/R_2	G	v_s Range
0	1	−10 V to +10 V
1	2	−5 V to +5 V
9	10	−1 V to +1 V
99	100	−0.1 V to +0.1 V
1000	~ 1000	−10 mV to +10 mV (approx.)
10^6	$\sim 10^6$	−10 μV to +10 μV (approx.)

(See)

4-4 Inverting Amplifier

▶ In an *inverting amplifier* op-amp circuit, the input source is connected to terminal v_n (instead of to terminal v_p) through an ***input source resistance*** R_s, and terminal v_p is connected to ground. ◀

Feedback from the output continues to be applied at v_n (through a *feedback resistance* R_f), as shown in Fig. 4-9. It is called an *inverting* amplifier because (as we will see shortly) the circuit gain G is negative.

To relate the output voltage v_o to the input signal voltage v_s, we start by writing down the node-voltage equation at terminal v_n as

$$i_1 + i_2 + i_n = 0 \tag{4.21}$$

or

$$\frac{v_n - v_s}{R_s} + \frac{v_n - v_o}{R_f} + i_n = 0. \tag{4.22}$$

Inverting Amplifier

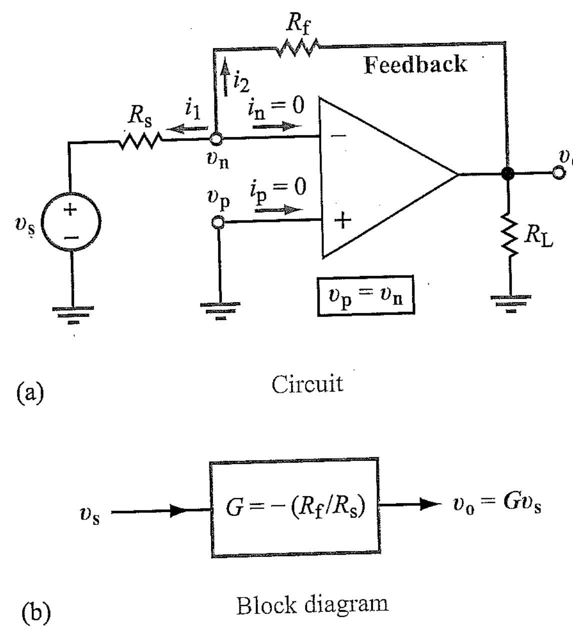


Figure 4-9: Inverting amplifier circuit and its block-diagram equivalent.

Upon invoking the op-amp current constraint given by Eq. (4.16), namely $i_n = 0$, and the voltage constraint $v_n = v_p$, as well as recognizing that $v_p = 0$ (because terminal v_p is connected to ground), we obtain the relationship

$$v_o = -\left(\frac{R_f}{R_s}\right) v_s. \tag{4.23}$$

The circuit voltage gain of the inverting amplifier therefore is given by

$$G = \frac{v_o}{v_s} = -\left(\frac{R_f}{R_s}\right). \tag{4.24}$$

▶ In addition to amplifying v_s by the ratio (R_f/R_s), the inverting amplifier also reverses the polarity of v_s. ◀

▶ v_o is independent of the magnitude of the load resistance R_L, so long as R_L is much larger than the op-amp output resistance R_o (which is an implicit assumption of the ideal op-amp model). ◀

Because $v_n = 0$, a Thévenin analysis of the circuit in Fig. 4-9(a) would reveal that the *input resistance* of the inverting amplifier circuit (as seen by source v_s) is $R_{input} = R_{Th} = R_s$.

▶ **Caution:** Under the ideal op-amp model, it is not possible to compute i_o, the current that flows into the op amp from output terminal v_o. Hence, it is inappropriate to apply KCL at that terminal. ◀

Example 4-2: Amplifier with Input Current Source

For the circuit shown in Fig. 4-10(a): (a) obtain an expression for the input-output transfer function $K_t = v_o/i_s$ and evaluate it for $R_1 = 1$ kΩ, $R_2 = 2$ kΩ, $R_f = 30$ kΩ, and $R_L = 10$ kΩ; and (b) determine the linear dynamic range of i_s if $V_{cc} = 20$ V.

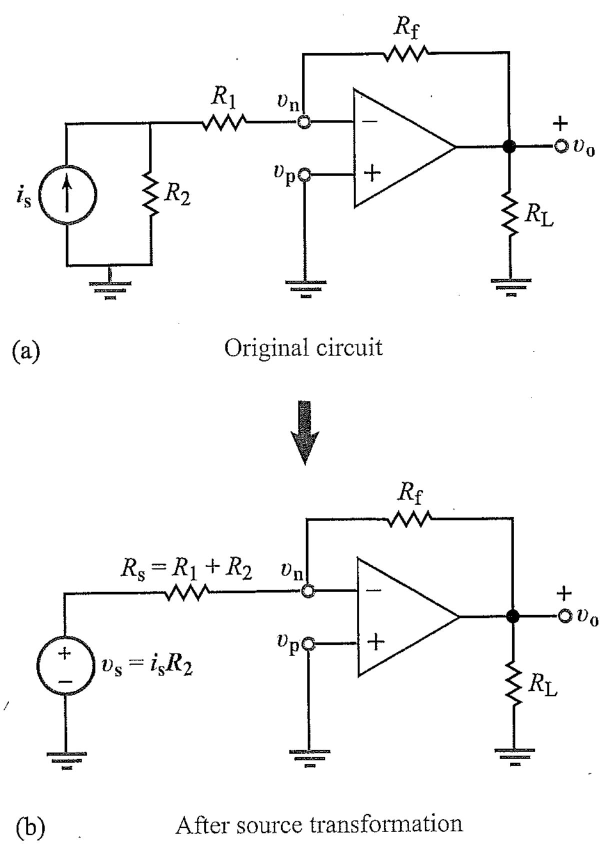


Figure 4-10: Inverting amplifier circuit of Example 4-2.

Solution:

(a) Application of the source transformation method converts the combination of i_s and R_2 into a voltage source $v_s = i_s R_2$, in series with a resistance R_2. Upon combining R_2 in series with R_1, we obtain the new circuit shown in Fig. 4-10(b), which is identical in form with the inverting amplifier circuit of Fig. 4-9, except that now the source resistance is $R_s = (R_1 + R_2)$. Hence, application of Eq. (4.23) gives

$$v_o = -\left(\frac{R_f}{R_1 + R_2}\right) v_s = -\left(\frac{R_f}{R_1 + R_2}\right) R_2 i_s, \qquad (4.25)$$

from which we obtain the transfer function

$$K_t = \frac{v_o}{i_s} = -\frac{R_f R_2}{R_1 + R_2}. \qquad (4.26)$$

For $R_1 = 1$ kΩ, $R_2 = 2$ kΩ, and $R_f = 30$ kΩ,

$$K_t = \frac{v_o}{i_s} = -2 \times 10^4 \qquad \text{(V/A)}.$$

(b) From the expression for K_t,

$$i_s = -\frac{v_o}{2 \times 10^4},$$

and since $|v_o|$ is bounded by $V_{cc} = 20$ V, the linear range for i_s is bounded by

$$|i_s| = \left|\frac{V_{cc}}{2 \times 10^4}\right| = \left|\frac{20}{2 \times 10^4}\right| = 1 \text{ mA}.$$

Thus, the linear range of i_s extends from −1 mA to +1 mA.

Concept Question 4-9: How does feedback control the gain of the inverting-amplifier circuit?

Concept Question 4-10: The expression given by Eq. (4.24) states that the gain of the inverting amplifier is independent of the magnitude of R_L. Would the expression remain valid if $R_L = 0$? Explain.

Exercise 4-4: The input to an inverting-amplifier circuit consists of $v_s = 0.2$ V and $R_s = 10$ Ω. If $V_{cc} = 12$ V, what is the maximum value that R_f can assume before saturating the op amp?

Answer: $G_{max} = -60$, $R_f = 600$ Ω. (See)

4-5 Summing Amplifier

By connecting multiple sources in parallel at terminal v_n of the inverting amplifier, the circuit becomes an *adder* (or more precisely a *scaled inverting adder*). After we demonstrate how such a circuit (usually called a *summing amplifier*) works for two input voltages v_1 and v_2, we will extend it to multiple sources.

For the circuit shown in Fig. 4-11(a), our goal is to relate the output voltage v_o to v_1 and v_2. To do so, we apply the source-transformation technique so as to cast the input circuit in the form of a single voltage source v_s in series with a source resistance R_s. The steps involved in the transformation are illustrated in Fig. 4-11(b) and (c). Voltage to current transformation gives $i_{s_1} = v_1/R_1$ and $i_{s_2} = v_2/R_2$, which can be combined together into a single current source as

$$i_s = i_{s_1} + i_{s_2} = \frac{v_1}{R_1} + \frac{v_2}{R_2} = \frac{v_1R_2 + v_2R_1}{R_1R_2}. \tag{4.27}$$

Similarly, the two parallel resistors add up to

$$R_s = \frac{R_1R_2}{R_1 + R_2}. \tag{4.28}$$

If we transform (i_s, R_s) into a voltage source (v_s, R_s), we get

$$v_s = i_sR_s = \left(\frac{v_1R_2 + v_2R_1}{R_1R_2}\right)\frac{R_1R_2}{R_1 + R_2} = \frac{v_1R_2 + v_2R_1}{R_1 + R_2}. \tag{4.29}$$

The circuit in Fig. 4-11(c) is identical in form with that of the inverting amplifier of Fig. 4-9. Hence, by applying the input-output voltage relationship given by Eq. (4.23), we have

$$\begin{aligned} v_o &= -\left(\frac{R_f}{R_s}\right)v_s = -\frac{R_f}{\left(\dfrac{R_1R_2}{R_1 + R_2}\right)}\left(\frac{v_1R_2 + v_2R_1}{R_1 + R_2}\right) \\ &= -\left(\frac{R_f}{R_1}\right)v_1 - \left(\frac{R_f}{R_2}\right)v_2. \end{aligned} \tag{4.30}$$

This expression for v_o can be written in the form

$$v_o = G_1v_1 + G_2v_2, \tag{4.31}$$

where $G_1 = -(R_f/R_1)$ is the (negative) gain applied to source voltage v_1, and $G_2 = -(R_f/R_2)$ is the gain applied to v_2. Thus:

> ▶ The summing amplifier scales v_1 by G_1 and v_2 by G_2 and adds them together. ◀

For the special case where $R_1 = R_2 = R$,

$$v_o = -\left(\frac{R_f}{R}\right)[v_1 + v_2] \quad \textbf{(equal gain)}, \tag{4.32}$$

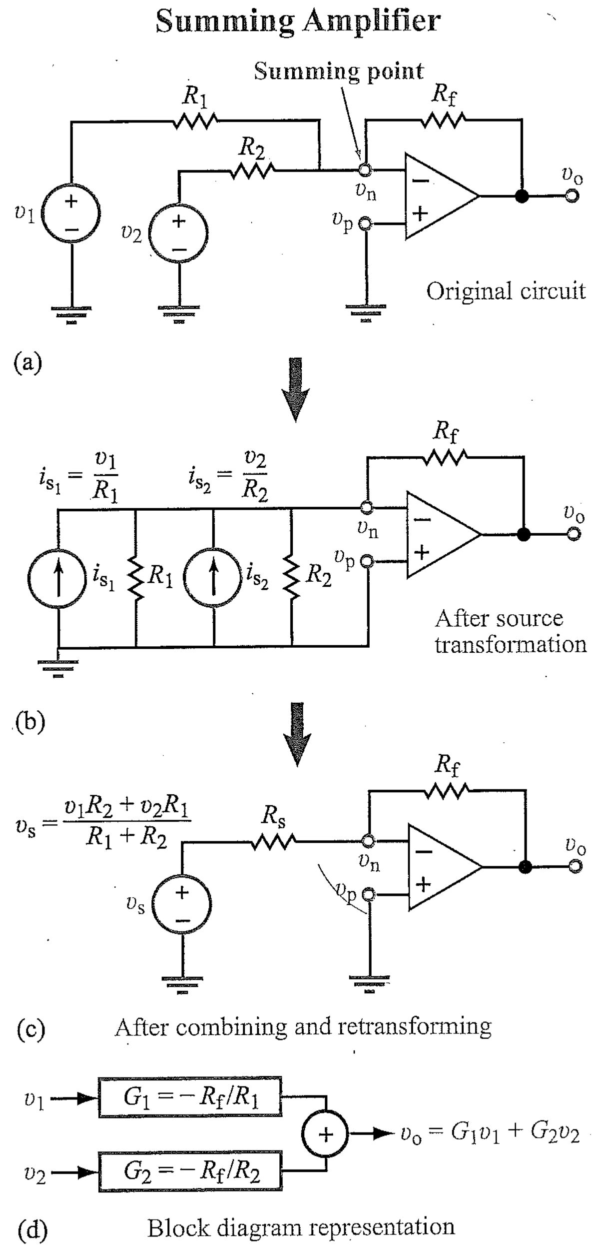
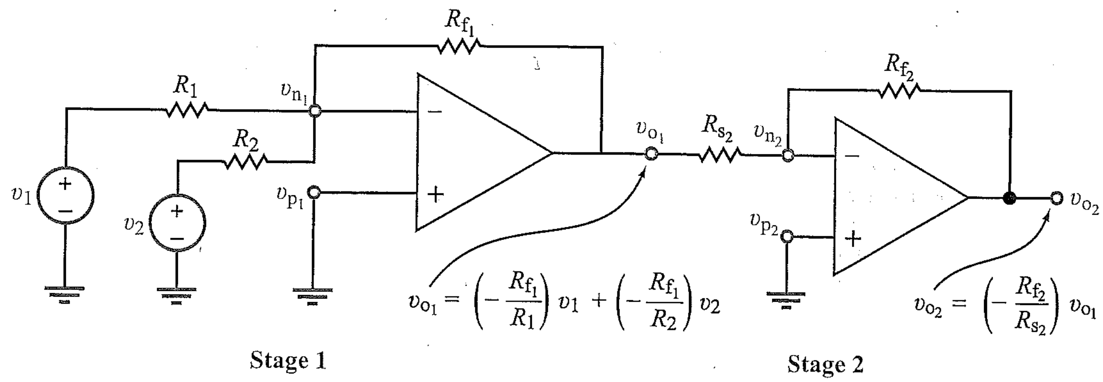


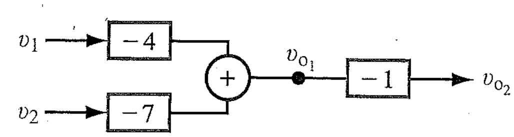
Figure 4-11: Summing amplifier.

and if additionally, $R_f = R_1 = R_2$, then $G_1 = G_2 = -1$. In this case, the summing amplifier becomes an inverted adder as characterized by

$$v_o = -(v_1 + v_2) \quad \textbf{(inverted adder)}. \tag{4.33}$$



(a) Two-stage circuit



(b) Block diagram

Figure 4-12: Two-stage circuit realization of $v_o = 4v_1 + 7v_2$.

Generalizing to the case where the input consists of n input voltage sources v_1 to v_n (associated with source resistances R_1 to R_n, respectively) and all are connected in parallel at the same summing point (terminal v_n), the output voltage becomes

$$v_o = \left(-\frac{R_f}{R_1}\right) v_1 + \left(-\frac{R_f}{R_2}\right) v_2 + \cdots + \left(-\frac{R_f}{R_n}\right) v_n. \tag{4.34}$$

Example 4-3: Summing Circuit

Use inverting amplifiers to design a circuit that performs the operation

$$v_o = 4v_1 + 7v_2.$$

Solution: The desired circuit has to amplify v_1 by a factor of 4, amplify v_2 by a factor of 7, and add the two together. A summing amplifier can do that, but it also inverts the sum. Hence, we will need to use a two-stage circuit with the first stage providing the desired operation within a "−" sign and then follow it up with an inverting amplifier with a gain of (-1). The two-stage circuit is shown in Fig. 4-12.

For the first stage, we need to select values for R_1, R_2, and R_{f_1} such that

$$\frac{R_{f_1}}{R_1} = 4 \qquad \text{and} \qquad \frac{R_{f_1}}{R_2} = 7.$$

Since we have only two constraints, we can satisfy the specified ratios with an infinite number of combinations. Arbitrarily, we choose $R_{f_1} = 56$ kΩ, which then specifies the other resistors as

$$R_1 = 14\ \text{k}\Omega \qquad \text{and} \qquad R_2 = 8\ \text{k}\Omega.$$

For the second stage, a gain of (-1) requires that

$$\frac{R_{f_2}}{R_{s_2}} = 1.$$

Arbitrarily, we choose $R_{f_2} = R_{s_2} = 20$ kΩ.

To perform the summing operation, the solution offered in Example 4-3 employed two inverting amplifier circuits—one to perform an inverted sum, and a second one to provide multiplication by (-1). Alternatively, the same result can be achieved by using a single op amp in a noninverting amplifier circuit, as shown in Fig. 4-13.

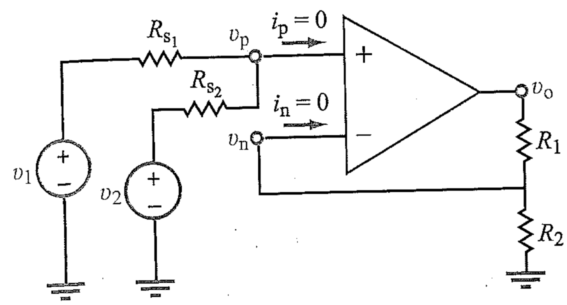


Figure 4-13: Noninverting summer.

From our analysis in Section 4-3, we established that the output voltage v_o of the noninverting amplifier circuit is related to v_p by

$$\frac{v_o}{v_p} = G = \frac{R_1 + R_2}{R_2}. \quad (4.35)$$

For the circuit in Fig. 4-13, in view of the ideal op-amp constraint that the op amp draws no current ($i_p = 0$), it is a straightforward task to show that

$$v_p = \frac{v_1 R_{s_2} + v_2 R_{s_1}}{R_{s_1} + R_{s_2}}. \quad (4.36)$$

Combining Eqs. (4.35) and (4.36) leads to

$$v_o = G\left[\left(\frac{R_{s_2}}{R_{s_2} + R_{s_1}}\right) v_1 + \left(\frac{R_{s_1}}{R_{s_1} + R_{s_2}}\right) v_2\right]. \quad (4.37)$$

To realize a coefficient of 4 for v_1 and a coefficient of 7 for v_2, it is necessary that

$$\frac{G R_{s_2}}{R_{s_1} + R_{s_2}} = 4$$

and

$$\frac{G R_{s_1}}{R_{s_1} + R_{s_2}} = 7.$$

A possible solution that satisfies these two constraints is $R_{s_1} = 7$ kΩ, $R_{s_2} = 4$ kΩ, and $G = 11$. Furthermore, the specified value of G can be satisfied by choosing $R_1 = 50$ kΩ and $R_2 = 5$ kΩ.

Concept Question 4-11: What type of op-amp circuits (inverting, noninverting, and others) might one use to perform the operation $v_o = G_1 v_1 + G_2 v_2$ with G_1 and G_2 both positive?

Concept Question 4-12: What is an inverting adder?

Exercise 4-5: The circuit shown in Fig. 4-12(a) is to be used to perform the operation

$$v_o = 3v_1 + 6v_2.$$

If $R_1 = 1.2$ kΩ, $R_{s_2} = 2$ kΩ, and $R_{f_2} = 4$ kΩ, select values for R_2 and R_{f_1} so as to realize the desired result.

Answer: $R_{f_1} = 1.8$ kΩ, $R_2 = 600$ Ω. (See)

4-6 Difference Amplifier

When an input signal v_2 is connected to terminal v_p of a noninverting amplifier circuit, the output is a scaled version of v_2. A similar outcome is generated by an inverting amplifier circuit when an input voltage v_1 is connected to the op amp's v_n terminal, except that in addition to scaling v_1 its polarity is reversed as well. The *difference amplifier* circuit combines these two functions to perform *subtraction*.

In the difference-amplifier circuit of Fig. 4-14(a), the input signals are v_1 and v_2, R_2 is the feedback resistance, R_1 is the source resistance of v_1, and resistances R_3 and R_4 serve to control the scaling factor (gain) of v_2. To obtain an expression that relates the output voltage v_o to the inputs v_1 and v_2, we apply KCL at nodes v_n and v_p. At v_n, $i_1 + i_2 + i_n = 0$, which is equivalent to

$$\frac{v_n - v_1}{R_1} + \frac{v_n - v_o}{R_2} + i_n = 0 \qquad (\text{node } v_n). \quad (4.38)$$

At v_p, $i_3 + i_4 + i_p = 0$, or

$$\frac{v_p - v_2}{R_3} + \frac{v_p}{R_4} + i_p = 0 \qquad (\text{node } v_p). \quad (4.39)$$

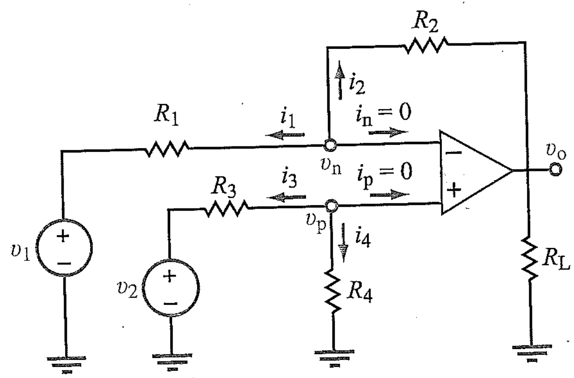
Upon imposing the ideal op-amp constraints $i_p = i_n = 0$ and $v_p = v_n$, we end up with

$$v_o = \left[\left(\frac{R_4}{R_3 + R_4}\right)\left(\frac{R_1 + R_2}{R_1}\right)\right] v_2 - \left(\frac{R_2}{R_1}\right) v_1, \quad (4.40)$$

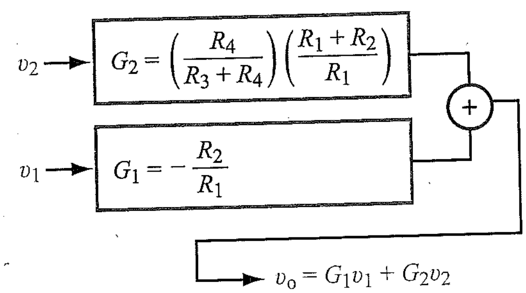
which can be cast in the form

$$v_o = G_2 v_2 + G_1 v_1, \quad (4.41)$$

Difference Amplifier



(a) Difference circuit



(b) Block diagram

Figure 4-14: Difference-amplifier circuit.

where the scale factors (gains) are given by

$$G_2 = \left(\frac{R_4}{R_3 + R_4}\right)\left(\frac{R_1 + R_2}{R_1}\right) \tag{4.42a}$$

and

$$G_1 = -\left(\frac{R_2}{R_1}\right). \tag{4.42b}$$

According to Fig. 4-14(b) which is a block-diagram representation of the difference amplifier circuit:

> ▶ The difference amplifier scales υ_2 by positive gain G_2, υ_1 by negative gain G_1 and adds them together. ◀

For the difference amplifier to function as a subtraction circuit with equal gain, its resistors have to be interrelated by

$$R_2 R_3 = R_1 R_4, \tag{4.43}$$

in which case Eq. (4.41) reduces to

$$\upsilon_o = \left(\frac{R_2}{R_1}\right)(\upsilon_2 - \upsilon_1) \qquad \textbf{(equal gain)}. \tag{4.44}$$

Exact subtraction with no scaling requires that $R_1 = R_2$.

Exercise 4-6: The difference-amplifier circuit of Fig. 4-14 is used to realize the operation

$$\upsilon_o = (6\upsilon_2 - 2) \text{ V}.$$

Given that $R_3 = 5$ kΩ, $R_4 = 6$ kΩ, and $R_2 = 20$ kΩ, specify values for υ_1 and R_1.

Answer: $\upsilon_1 = 0.2$ V, $R_1 = 2$ kΩ. (See)

4-7 Voltage Follower

In electronic circuits, we often need to incorporate the functionality of a relatively simple (but important) circuit that serves to insulate the input source from variations in the load resistance R_L. Such a circuit is called a ***voltage follower*** or ***buffer***. To appreciate the utility of the voltage follower, let us first examine the circuit shown in Fig. 4-15(a). An input circuit represented by its Thévenin equivalent (υ_s, R_s), is connected to a load R_L. The output voltage is

$$\upsilon_o = \frac{\upsilon_s R_L}{R_s + R_L} \qquad \text{(without voltage follower)}, \tag{4.45}$$

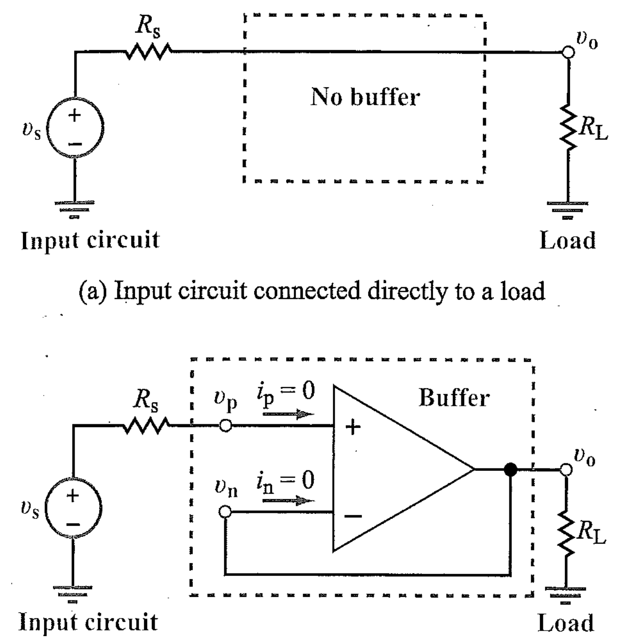
which obviously is dependent on both R_s and R_L.

In contrast, when the op-amp voltage follower circuit shown in Fig. 4-15(b) is inserted in between the input circuit and the load, the output voltage becomes completely independent of both R_s and R_L. Because $i_p = 0$, it follows that $\upsilon_p = \upsilon_s$. Furthermore, in view of the op-amp constraint $\upsilon_p = \upsilon_n$ and because the output node is connected directly to υ_n, it follows that

$$\upsilon_o = \upsilon_p = \upsilon_s \qquad \text{(with voltage follower)}, \tag{4.46}$$

and this is true regardless of the values of R_s and R_L (excluding R_s = open circuit and/or R_L = short circuit, either of which would invalidate the entire circuit). Thus:

> ▶ The output of the voltage follower ***follows*** the input signal while remaining immune to changes in R_L. ◀



(a) Input circuit connected directly to a load

(b) Input circuit separated by a buffer

Figure 4-15: The voltage follower provides no voltage gain ($\upsilon_o = \upsilon_s$), but it insulates the input circuit from the load.

A circuit that offers this type of protection is often called a *buffer*.

> **Concept Question 4-13:** What is the function of a voltage follower, and why is it called a "buffer"?
>
> **Concept Question 4-14:** How much voltage gain is provided by the voltage follower?

Exercise 4-7: Express υ_o in terms of υ_1, υ_2, and υ_3 for the circuit in Fig. E4-7.

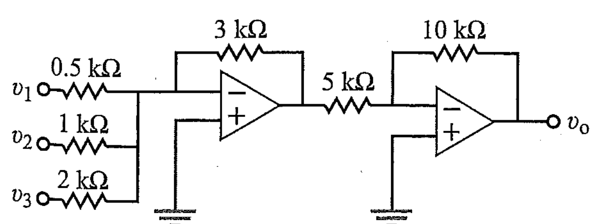


Figure E4-7

Answer: $\upsilon_o = 12\upsilon_1 + 6\upsilon_2 + 3\upsilon_3$. (See)

4-8 Op-Amp Signal-Processing Circuits

Table 4-3 provides a summary of the op-amp circuits we have considered thus far, together with their functional characteristics in the form of block-diagram representations. These circuits can be used in various combinations to realize specific signal-processing operations. We note that the input-output transfer functions are independent of the load resistance R_L that may be connected between the output terminal υ_o and ground. In the case of the noninverting amplifier, the transfer function is also independent of the source resistance R_s.

> ▶ When cascading multiple stages of op-amp circuits in series, care must be exercised to ensure that none of the op amps is driven into saturation by the cumulative gain of the multiple stages. ◀

When analyzing circuits that involve op amps, whether in configurations similar to or different from those we encountered so far in this chapter, the basic rules to remember are as follows:

Basic Rules of Op-Amp Circuits

(1) KCL and KVL always apply everywhere in the circuit, but KCL fails at the output node when applying the ideal op-amp model.

(2) The op amp will operate in the linear range so long as $|\upsilon_o| < |V_{cc}|$.

(3) The ideal op-amp model assumes that the source resistance R_s (connected to terminals υ_p or υ_n) is much smaller than the op-amp input resistance R_i (which usually is no less than 10 MΩ), and the load resistance R_L is much larger than the op-amp output resistance R_o (which is on the order of tens of ohms).

(4) The ideal op-amp constraints are $i_p = i_n = 0$ and $\upsilon_p = \upsilon_n$.

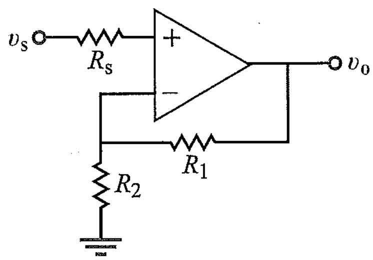
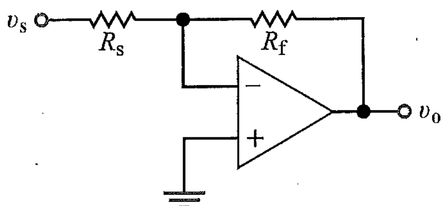
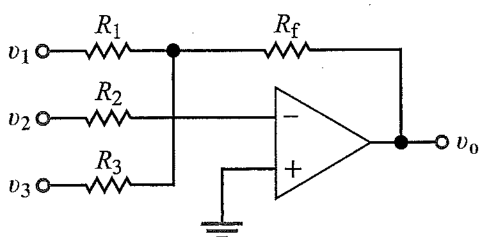
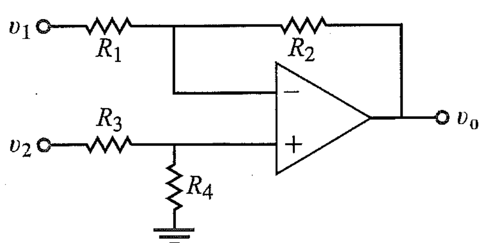
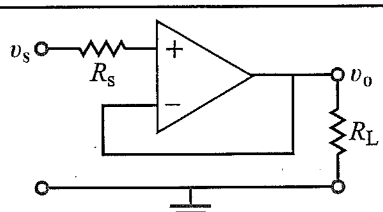
Example 4-4: Interesting Op-Amp Circuit

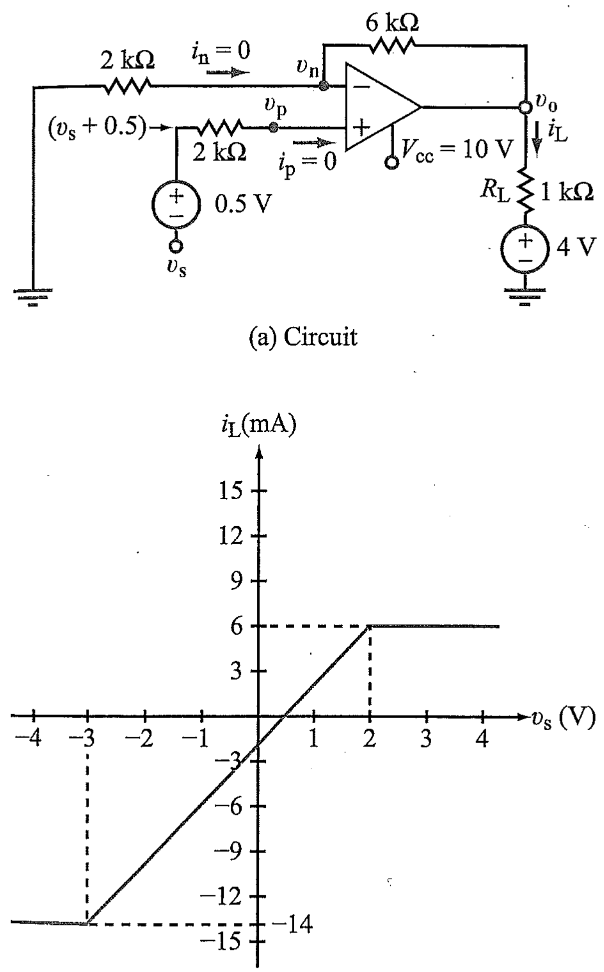
Generate a plot for i_L at the output side of the circuit shown in Fig. 4-16(a) versus υ_s, covering the full linear range of υ_s.

Solution: At node υ_n, KCL gives

$$\frac{\upsilon_n}{2k} + \frac{\upsilon_n - \upsilon_o}{6k} = 0,$$

Table 4-3: Summary of op-amp circuits.

Op-Amp Circuit	Block Diagram
	$v_s \longrightarrow \boxed{G = \dfrac{R_1 + R_2}{R_2}} \longrightarrow v_o = Gv_s$ **Noninverting Amp** (v_o independent of R_s)
	$v_s \longrightarrow \boxed{G = -\dfrac{R_f}{R_s}} \longrightarrow v_o = Gv_s$ **Inverting Amp**
	$v_1 \longrightarrow \boxed{G_1 = -R_f/R_1}$ $v_2 \longrightarrow \boxed{G_2 = -R_f/R_2} \longrightarrow (+) \longrightarrow v_o = G_1v_1 + G_2v_2 + G_3v_3$ $v_3 \longrightarrow \boxed{G_3 = -R_f/R_3}$ **Inverting Summer**
	$v_1 \longrightarrow \boxed{G_1 = -\dfrac{R_2}{R_1}}$ $(+) \longrightarrow v_o = G_1v_1 + G_2v_2$ $v_2 \longrightarrow \boxed{G_2 = \left(\dfrac{R_1 + R_2}{R_1}\right)\left(\dfrac{R_4}{R_3 + R_4}\right)}$ **Subtracting Amp**
	$v_s \longrightarrow \boxed{G = 1} \longrightarrow v_o = v_s$ **Voltage Follower** (v_o independent of R_s and R_L)



(a) Circuit

(b) $i_L - v_s$ transfer plot

Figure 4-16: Circuit for Example 4-4.

which leads to

$$v_o = 4v_n.$$

At node v_p, KCL gives

$$\frac{v_p - (v_s - 0.5)}{2k} = 0,$$

which leads to

$$v_p = v_s + 0.5.$$

By imposing the op-amp constraint $v_p = v_n$, we have

$$v_o = 4v_n = 4(v_s + 0.5) = 4v_s + 2.$$

At the output side,

$$i_L = \frac{v_o - 4}{1k} = \frac{4v_s + 2 - 4}{1k} = (4v_s - 2) \text{ mA}.$$

For $v_o = V_{cc} = 10$ V,

$$10 = 4v_s + 2, \qquad \text{or } v_s = 2 \text{ V},$$

and for $v_o = -V_{cc} = -10$ V,

$$-10 = 4v_s + 2, \qquad \text{or } v_s = -3 \text{ V}.$$

Hence, linear range of v_s is

$$-3 \text{ V} \leq v_s \leq 2 \text{ V} \qquad \text{(linear range)}.$$

Figure 4-16(b) displays a plot of i_L versus v_s over the latter's linear range.

Example 4-5: Elevation Sensor

A hand-held elevation sensor uses a pair of capacitors separated by a flexible metallic membrane ([Fig. 4-17(a)] to measure the height h above sea level. The lower chamber in Fig. 4-17(a) is sealed, and its pressure is P_0, which is the standard atmospheric pressure at sea level. The pressure in the upper chamber, which is open to the outside air, is P. When at sea level, $P = P_0$, so the membrane assumes a flat shape and the two capacitances are equal. Since atmospheric pressure decreases with elevation, a rise in altitude results in a change in the pressure P in the upper chamber, causing the membrane to bend upwards [Fig. 4-17(b)], thereby changing the capacitances of the two capacitors. The sensor measures a voltage v_s that is proportional to the change in capacitance.

Based on measurements of v_s as a function of h, the data was found to exhibit an approximately linear variation given by

$$v_s = 2 + 0.2h \qquad \text{(V)}, \tag{4.47}$$

where h is in km. The sensor is designed to operate over the range $0 \leq h \leq 10$ km. Design a circuit whose output voltage v_o (in volts) is an exact indicator of the height h (in km).

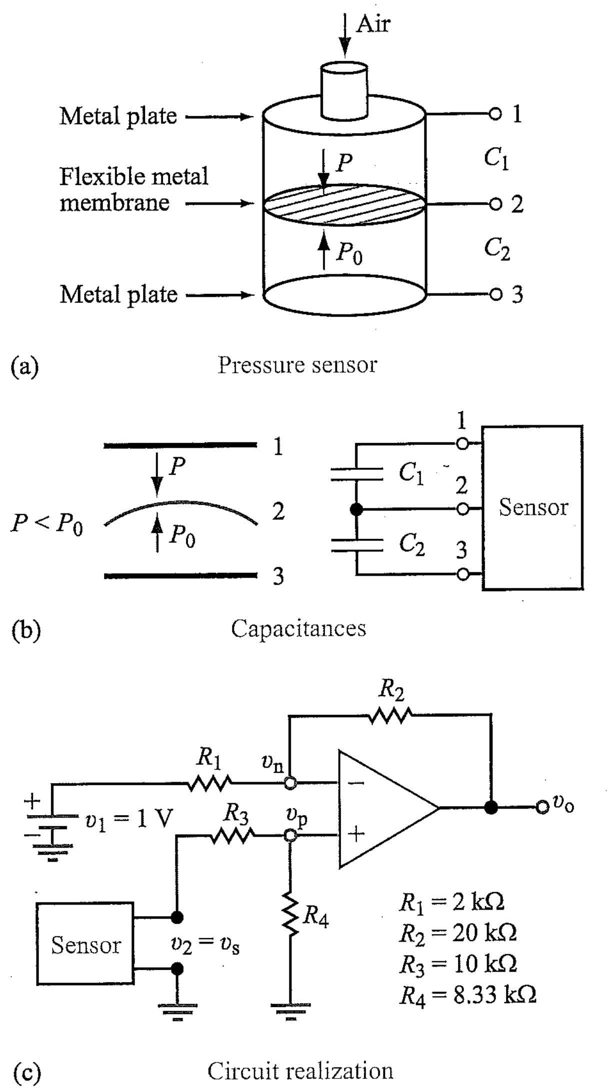


Figure 4-17: Design of a circuit for the pressure sensor of Example 4-5 with P_0 = pressure at sea level and P = pressure at height h.

Solution: Based on the given information, the sensor voltage v_s will serve as the input to the circuit we are asked to design, and the output v_o will represent the height elevation h. We therefore need a circuit that can perform the operation

$$v_o = h = \frac{1}{0.2}\,v_s - \frac{2}{0.2} = 5v_s - 10, \qquad (4.48)$$

where we have inverted Eq. (4.47) to solve for h in terms of v_s. The functional form of Eq. (4.48) indicates that we have only one active (variable) input, namely v_s, which we need to amplify by a factor of 5 but also need to subtract 10 V from it. There are multiple circuit configurations that can achieve the desired operation, including the subtractor circuit shown in Fig. 4-17(c). According to Eq. (4.40), the output of the difference amplifier is given by

$$v_o = \left[\left(\frac{R_4}{R_3+R_4}\right)\left(\frac{R_1+R_2}{R_1}\right)\right] v_2 - \left(\frac{R_2}{R_1}\right) v_1. \qquad (4.49)$$

Equation (4.49) can be made to correspond to Eq. (4.48) if we select the following

(a) $v_s = v_2$

(b) v_1 as a dc voltage source such that $(R_2/R_1)v_1 = 10$ V, which can be satisfied by arbitrarily selecting $v_1 = 1$ V and $(R_2/R_1) = 10$

(c) values for R_1 through R_4 that simultaneously satisfy the conditions

$$\frac{R_2}{R_1} = 10 \qquad \text{and} \qquad \left(\frac{R_4}{R_3+R_4}\right)\left(\frac{R_1+R_2}{R_1}\right) = 5$$

A possible set of values that meets these conditions is

$$R_1 = 2\ \text{k}\Omega, \qquad R_2 = 20\ \text{k}\Omega,$$
$$R_3 = 10\ \text{k}\Omega, \qquad R_4 = 8.33\ \text{k}\Omega.$$

Before we conclude the design, we should check to make sure that the op amp will operate in its linear range over the full range of operation of the sensor. According to Eq. (4.47), as h varies from zero to 10 km, v_s varies from 2 V to 4 V. The corresponding range of variation of v_o, from Eq. (4.48), is from zero to 10 V. Hence, we should choose an op amp designed to function with a dc supply voltage V_{cc} that exceeds 10 V.

Example 4-6: Circuit with Multiple Op Amps

Relate the output voltage v_o to the input voltages v_1 and v_2 of the circuit in Fig. 4-18.

Solution: By comparing the circuit connections surrounding the four op amps with those given in Table 4-3, we recognize op amps 1 and 2 as noninverting amplifiers, op amp 3 as an inverting amplifier with a gain of −1 (equal input and feedback resistors R_4), and op amp 4 as an inverting summing amplifier with equal gain (same input resistances R_6 at summing point).

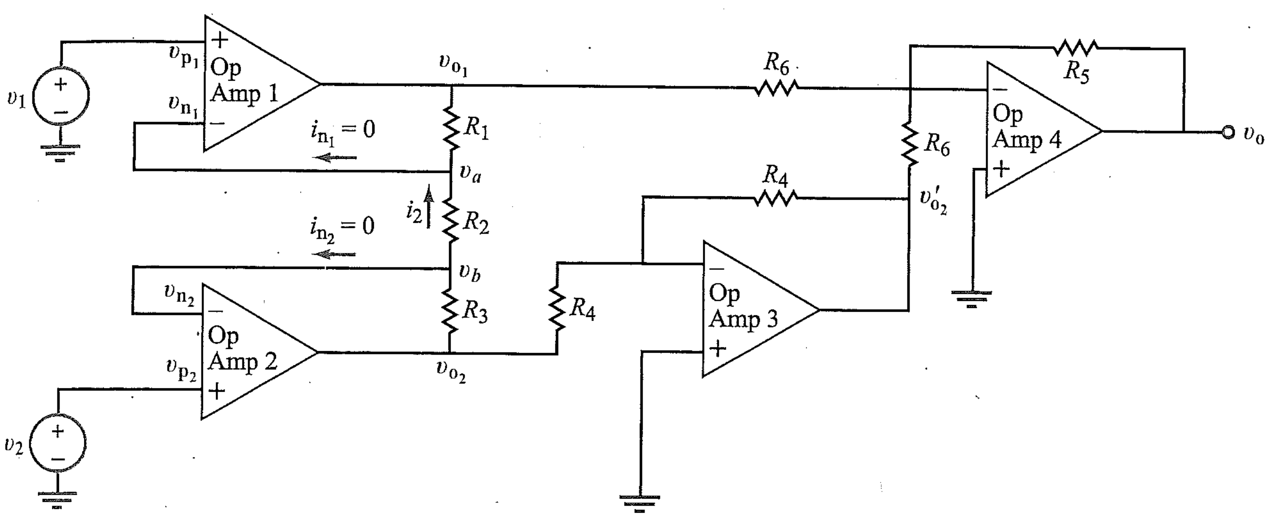


Figure 4-18: Example 4-6.

We start by examining the pair of input op amps. For op amp 1, $v_{p_1} = v_1$ and $v_{p_1} = v_{n_1}$ (op amp voltage constraint). Hence,

$$v_a = v_{n_1} = v_1.$$

Similarly, for op amp 2,

$$v_b = v_{n_2} = v_2.$$

Since $i_{n_1} = i_{n_2} = 0$ (op amp current constraint),

$$i_2 = \frac{v_b - v_a}{R_2} = \frac{v_2 - v_1}{R_2},$$

and

$$\begin{aligned} v_{o_2} - v_{o_1} &= i_2(R_1 + R_2 + R_3) \\ &= \left(\frac{R_1 + R_2 + R_3}{R_2}\right)(v_2 - v_1). \end{aligned} \tag{4.50}$$

For op amp 3,

$$v'_{o_2} = -v_{o_2},$$

and for op amp 4,

$$\begin{aligned} v_o &= -\frac{R_5}{R_6}(v_{o_1} + v'_{o_2}) \\ &= -\frac{R_5}{R_6}(v_{o_1} - v_{o_2}) \\ &= \frac{R_5}{R_6}(v_{o_2} - v_{o_1}) = R_5\left(\frac{R_1 + R_2 + R_3}{R_6 R_2}\right)(v_2 - v_1). \end{aligned} \tag{4.51}$$

Example 4-7: Block-Diagram Representation

Generate a block-diagram representation for the circuit shown in Fig. 4-19(a).

Solution: The first op amp is an inverting amplifier with a dc input voltage $v_1 = 0.42$ V. Its circuit gain G_i (with the subscript added to denote "inverting amp") is

$$\begin{aligned} G_i &= -\frac{30K}{10K} \\ &= -3, \end{aligned}$$

and its output is

$$\begin{aligned} v_{o_1} &= G_i v_1 \\ &= -3(0.42) \\ &= -1.26 \text{ V}. \end{aligned}$$

The second op amp is a difference amplifier. Using Table 4-3, the gains of its positive and negative channels are

$$\begin{aligned} G_2 &= \left(\frac{R_4}{R_3 + R_4}\right)\left(\frac{R_1 + R_2}{R_1}\right) \\ &= \left(\frac{2K}{1K + 2K}\right)\left(\frac{10K + 20K}{10K}\right) \\ &= 2 \end{aligned}$$

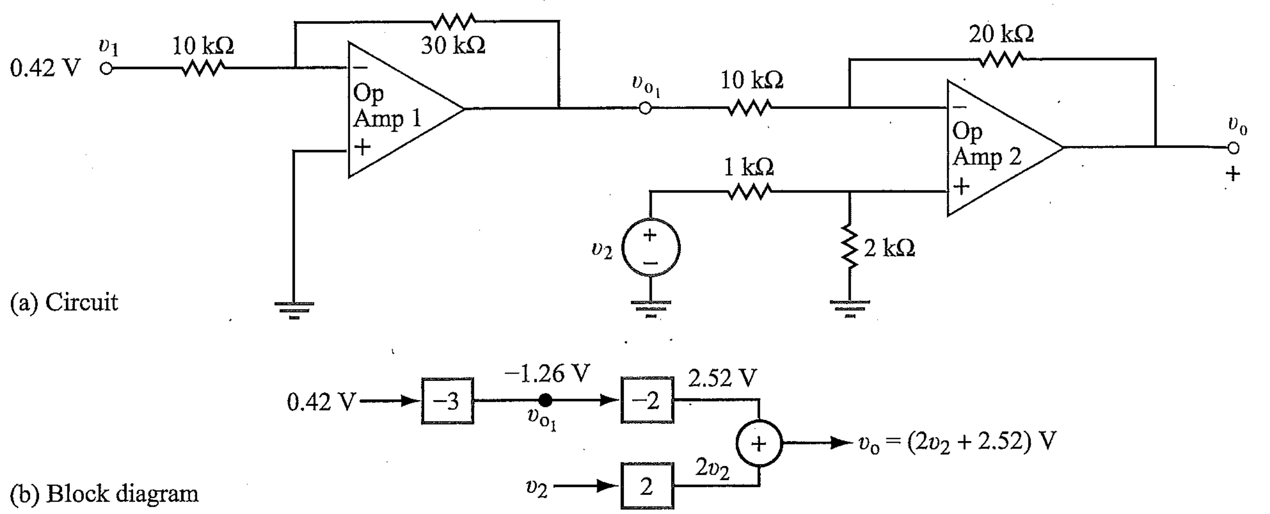


Figure 4-19: Block-diagram representation (Example 4-7).

and

$$\begin{aligned} G_1 &= -\frac{R_2}{R_1} \\ &= -\frac{20K}{10K} \\ &= -2. \end{aligned}$$

Hence,

$$\begin{aligned} v_o &= G_2 v_2 + G_1 v_{o_1} \\ &= 2v_2 - 2(-1.26) \\ &= (2v_2 + 2.52) \text{ V}. \end{aligned}$$

4-9 Instrumentation Amplifier

An electric *sensor* is a circuit used to measure a physical quantity, such as distance, motion, temperature, pressure, or humidity. *In some applications, the intent is not to measure the magnitude of a certain quantity, but rather to sense small deviations from a nominal value.* For example, if the temperature in a room is to be maintained at 20°C, the functional goal of the temperature sensor is to measure the difference between the room temperature T and the reference temperature $T_0 = 20$°C and then to activate an air conditioning or heating unit if the deviation exceeds a certain prespecified threshold. Let us assume the threshold is 0.1°C. Instead of requiring the sensor to be able to measure T with an absolute accuracy of no less than 0.1°C, an alternative approach would be to design the sensor to measure $\Delta v = v_2 - v_1$, where v_2 is the voltage output of a thermocouple circuit responding to the room temperature T and v_1 is the voltage corresponding to what a calibrated thermocouple would measure when $T_0 = 20$°C. Thus, the sensor is designed to measure the deviation of T from T_0, rather than T itself, with an absolute accuracy of no less than 0.1°C. The advantage of such an approach is that the signal is now Δv, which is more than two orders of magnitude smaller than v_2. A circuit with a precision of 10 percent is not good enough for measuring v_2, but it is plenty good for measuring Δv.

► The instrumentation amplifier is suited perfectly for detecting and amplifying a small signal deviation when superimposed on one or the other of two much larger (and otherwise identical) signals. ◄

An instrumentation amplifier consists of three op amps, as shown in Fig. 4-20. The circuit configuration for the first two is the same as the one we examined earlier in connection with Example 4-6. According to Eq. (4.50), the voltage difference between the outputs of op amps 1 and 2 is

$$\begin{aligned} v_{o_2} - v_{o_1} &= \left(\frac{R_1 + R_2 + R_3}{R_2}\right)(v_2 - v_1) \\ &= G_1(v_2 - v_1), \end{aligned} \tag{4.52}$$

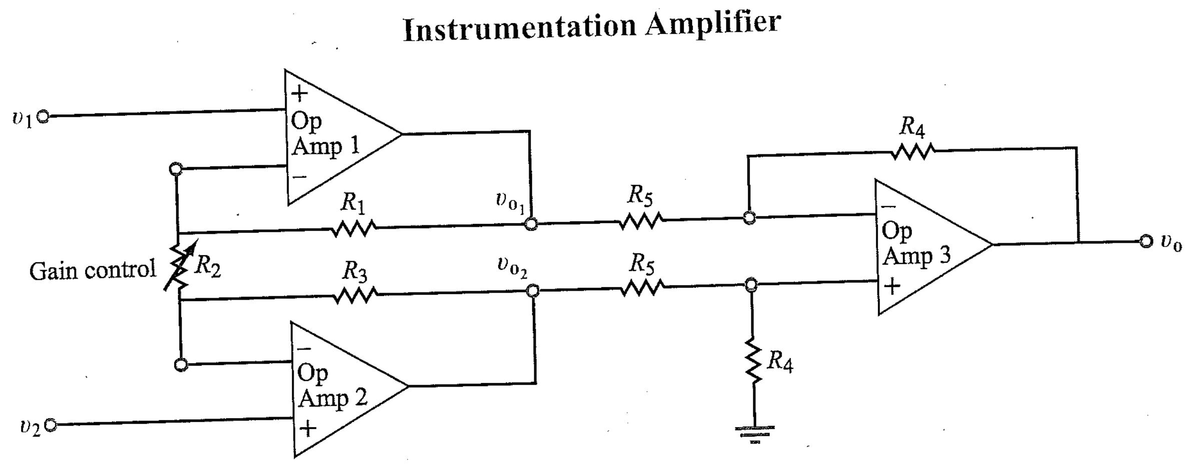


Figure 4-20: Instrumentation-amplifier circuit.

where G_1 is the circuit gain of the first stage (which includes op amps 1 and 2) and is given by

$$G_1 = \frac{R_1 + R_2 + R_3}{R_2}. \tag{4.53}$$

The third op amp is a difference amplifier that amplifies $(v_{o_2} - v_{o_1})$ by a gain factor G_2 given by

$$G_2 = \frac{R_4}{R_5}. \tag{4.54}$$

Hence,

$$\begin{aligned} v_o &= G_2 G_1 (v_2 - v_1) \\ &= \left(\frac{R_4}{R_5}\right)\left(\frac{R_1 + R_2 + R_3}{R_2}\right)(v_2 - v_1). \end{aligned} \tag{4.55}$$

To simplify the circuit—and improve precision—all resistors—with the exception of R_2—often are chosen to be identical in design and construction, thereby minimizing deviations between their resistances. If we set $R_1 = R_3 = R_4 = R_5 = R$ in Eq. (4.55), the expression for v_o reduces to

$$v_o = \left(1 + \frac{2R}{R_2}\right)(v_2 - v_1). \tag{4.56}$$

In that case, R_2 becomes the *gain-control resistance* of the circuit; its value (relative to R) sets the gain. If the expected signal deviation $(v_2 - v_1)$ is on the order of microvolts to millivolts, the instrumentation amplifier is designed to have an overall gain that would amplify the signal to the order of volts.

▶ *The instrumentation amplifier is a high-sensitivity, high-gain, deviation sensor.* Several semiconductor manufacturers offer instrumentation-amplifier circuits in the form of integrated packages. ◀

Concept Question 4-15: When designing a multistage op-amp circuit, what should the design engineer do to insure that none of the op amps is driven into saturation?

Concept Question 4-16: If the goal is to measure small deviations between a pair of input signals, what is the advantage of using an instrumentation amplifier over using a difference amplifier?

Exercise 4-8: To monitor brain activity, an instrumentation-amplifier sensor uses a pair of needle-like probes inserted at different locations in the brain to measure the voltage difference between them. If the circuit is of the type shown in Fig. 4-20 with $R_1 = R_3 = R_4 = R_5 = R = 50\ \text{k}\Omega$, $V_{cc} = 12$ V, and the maximum magnitude of the voltage difference that the brain is likely to exhibit is 3 mV, what should R_2 be to maximize the sensitivity of the brain sensor?

Answer: $R_2 = 25\ \Omega$. (See)