wb_gpio Specification

Introduction

The `wb_gpio` module is a simple General Purpose Input/Output (GPIO) interface designed to work with a Wishbone bus. It provides configurable bus width support, allowing for a range of 1 to 32 bits. The module facilitates basic GPIO operations, including setting data and direction registers. The first 32-bit word is used for GPIO data, while the second 32-bit word is for the direction register. The module adheres to the Wishbone bus protocol, a standard for interfacing between IP cores in a system-on-chip (SoC) design.

Architecture

The `wb_gpio` module consists of a single top-level module with the following key components: - **GPIO Direction Register**: Controls the direction of each GPIO pin. A '1' in the direction register sets the corresponding GPIO pin as an output. - **GPIO Data Register**: Holds the data to be output on the GPIO pins when they are configured as outputs. - **Wishbone Interface**: Handles communication with the Wishbone bus, including address decoding, data transfer, and acknowledgment signaling.

The module operates synchronously with the `wb_clk` clock signal and is reset using the `wb_rst` signal. The design includes logic for synchronizing input signals and generating acknowledgment signals for the Wishbone bus.

Interface

Signal	Width	In/Out	Description
wb_clk	1	In	Clock signal for synchronous operations.
wb_rst	1	In	Active-high reset signal. Resets internal registers.
wb_adr_i	1	In	Address input for selecting data or direction register.
wb_dat_i	n_bits	In	Data input for writing to GPIO registers.
wb_we_i	1	In	Write enable signal.
wb_cyc_i	1	In	Cycle valid input. Indicates a valid bus cycle.
wb_stb_i	1	In	Strobe signal. Indicates a valid data transfer cycle.
wb_cti_i	3	In	Cycle type identifier (unused in this module).
wb_bte_i	2	In	Burst type extension (unused in this module).
gpio_i	n_bits	In	Input data from GPIO pins.
wb_dat_o	n_bits	Out	Data output to the Wishbone bus. Reflects GPIO input or direction register.
wb_ack_o	1	Out	Acknowledgment signal for Wishbone bus transactions.

Signal	Width	In/Out	Description
wb_err_o	1	Out	Error signal for Wishbone bus (always 0 in this module).
wb_rty_o	1	Out	Retry signal for Wishbone bus (always 0 in this module).
gpio_o	n_bits	Out	Output data to GPIO pins.
gpio_dir_o	n_bits	Out	Direction control for GPIO pins.

Timing

The `wb_gpio` module operates synchronously with the `wb_clk` signal. The following timing characteristics are notable: - **Latency**: The module provides a single-cycle latency for read and write operations. The acknowledgment signal (`wb_ack_o`) is asserted in the cycle following a valid transaction. - **Signal Sampling**: Input signals are sampled on the rising edge of `wb_clk`. Outputs are updated on the same edge, ensuring synchronous operation.

Usage

To use the `wb_gpio` module, follow these steps: 1. **Initialization**: Ensure the module is reset by asserting `wb_rst` high. This sets all GPIO directions to input. 2. **Configuration**: Write to the direction register by setting `wb_adr_i` to 1 and providing the desired direction bits on `wb_dat_i`. Assert `wb_we_i`, `wb_cyc_i`, and `wb_stb_i` to initiate the write. 3. **Data Output**: To output data on GPIO pins, set `wb_adr_i` to 0 and provide the data on `wb_dat_i`. Assert the control signals as in the configuration step. 4. **Data Input**: Read the current state of GPIO inputs by setting `wb_adr_i` to 0 and observing `wb_dat_o` after the acknowledgment signal is asserted.

The module is designed for straightforward integration into systems using the Wishbone bus protocol, providing flexible GPIO control with minimal configuration overhead.

Functional Description (Generated by funcgen)

Verilog Design Module Description

Module: wb_gpio (Source File: wb_gpio.v)

Purpose

The `wb_gpio` module is a simple configurable GPIO (General Purpose Input/Output) interface that follows the Wishbone bus protocol. It supports various bus widths and allows GPIO data and direction control via register-accessible interfaces.

Parameters

- **n_bits**: Default value = 32. This parameter specifies the width of the GPIO bus, ranging from 1 to 32 bits, allowing for flexibility in design according to specific requirements.

Ports

- **wb_clk** (input, 1-bit): The clock input signal for synchronizing all operations within the module.
- **wb_rst** (input, 1-bit): Active-high reset signal used to initialize registers to their default states.
- **wb_adr_i** (input, 1-bit, specifically bit 2): Wishbone address input, used to select between the GPIO data register and direction register.
- **wb_dat_i** (input, [n_bits-1:0]): Wishbone data input bus used for writing data to the internal registers.
- **wb_we_i** (input, 1-bit): Write-enable signal indicating a write operation.
- **wb_cyc_i** (input, 1-bit): Cycle indicator for valid bus transactions.
- **wb_stb_i** (input, 1-bit): Strobe signal for signaling valid operations.
- **wb_cti_i** (input, 3-bit): Cycle type identifier, not used in the module's logic.
- **wb_bte_i** (input, 2-bit): Burst type extension, not used in the module's logic.
- **wb_dat_o** (output reg, [n_bits-1:0]): Wishbone data output bus used for reading data from the internal registers.
- **wb_ack_o** (output reg, 1-bit): Acknowledge signal indicating the completion of a bus transaction.
- **wb_err_o** (output, 1-bit): Error signal, always low, indicating no error condition is present.
- **wb_rty_o** (output, 1-bit): Retry signal, always low, indicating no need for transaction retrying.
- **gpio_i** (input, [n_bits-1:0]): Input bus for external GPIO signals.
- **gpio_o** (output reg, [n_bits-1:0]): Output bus for driving external GPIO signals.
- **gpio_dir_o** (output reg, [n_bits-1:0]): Output bus to control the direction of each GPIO pin, with '1' indicating an output and '0' indicating an input.

Internal Signals

- **gpio_i_ff** (reg, [n_bits-1:0]): An internal register used to store the synchronized input data from `gpio_i`.

Functionality

Sequential Logic

- **GPIO Direction Register**: On reset (wb_rst), all direction bits in gpio_dir_o are set to zero, indicating input by default. When a valid bus transaction occurs (wb_cyc_i & wb_stb_i & wb_we_i), if the address bit wb_adr_i[2] is high, the module updates the direction register gpio_dir_o with wb_dat_i.
- **GPIO Data Out Register**: On reset, gpio_o is set to zero. It updates with the incoming data wb_dat_i whenever a write transaction occurs targeting the data register (wb_adr_i[2] is low).
- **GPIO Input Synchronization**: The gpio_i input is synchronized to the system clock and stored in gpio_i_ff.
- **Bus Readback Logic**: On every clock cycle, the module updates the wb_dat_o register with the contents of gpio_i_ff (when reading the data register) or gpio_dir_o (when reading the direction register).
- **Acknowledge Signal Logic**: The wb_ack_o signal is asserted (set high) on the first cycle of a valid transaction (wb_cyc_i & wb_stb_i) and is de-asserted (set low) on the subsequent cycle, providing feedback for transaction completion.

Combinational Logic

- The modules have dedicated outputs wb_err_o and wb_rty_o which are fixed at logic low, indicating no support for error handling and retry requests.

Instantiations

- There are no sub-module instantiations within wb_gpio.

Inter-Module Connections

- Given there is only one module description provided, no inter-module connections are present. The wb_gpio module exists as a standalone block within a larger system, interfacing other components via its ports to the Wishbone bus and external GPIO connections.