Experiment No: 01

Name of the experiment: Studing different digital logic gates and designing of basic logic gates Using Universal gates.

GITTOUP numbers: 03

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Course Title: Digital Logic and circuits Lab

section: M

Date of experiment: 26/05/2022

Date of Submission: 13/06/2022

Objective of the experiment:

To understand the behaviour of the logic circuits using some ancul Integrated, Chips (Ic) and understanding the conversion of different digital logic function Using Universal gates.

List of Components:

3. Power Supply

4. Willes.

IC List:

+ 7408 : 1 Pcs

7404: 1 Pcs

7402: 1 Pes

1 Pcs

7432: 7400: 1 Pes

7486: 1 Pes

^{1.} Digital trainer board

^{2.} IC

3. Symbols, black diagram and figures:



Fig: AND Gate

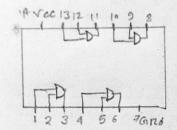


Fig: TC 7408

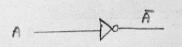
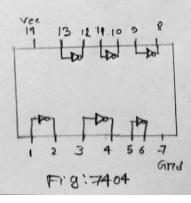


Fig: Not Bate



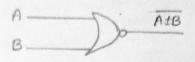
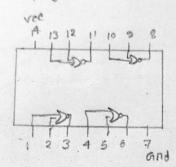


Fig: NOR Gale



F18: 7402

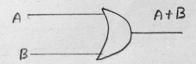
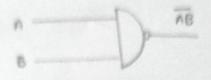


Fig: DR Gate.

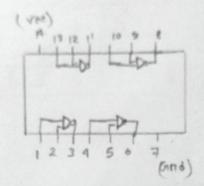
(Yee) 131211 10 2 2

1 2 3 4 5 6 7

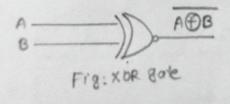
Fig: 7432

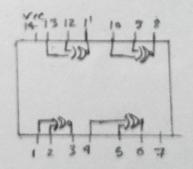


FIS! NAND gale



F18: 7400





F18: Te 7486

Data table a calculation:

1. FOR AND gate:

AB		output		
0	0	0		
0 1		ව		
1	0	0		
1 1		1		

2. FOR NOT gate:

A	output	
Ø	ı	
1	0	

3. Nor gale:

A	В	output
0	0	
0	1	0
(0	0
(1	0

4. OR gate:

A	В	output
0	0	0
0	1	1
1	0	1. 1
1	1	1

5. NAND gate:

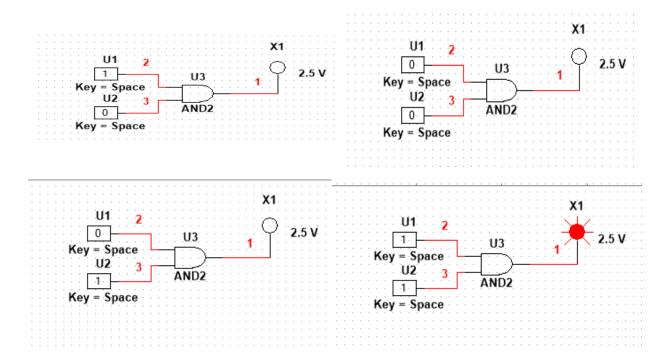
В	A	outpul		
0	0	1		
1	0	1		
0	1			
1	1	0		

6. XOR :

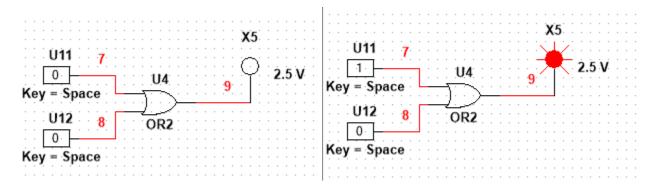
AB		output		
0	0	0		
0	1	1		
1	0	1		
1		0		

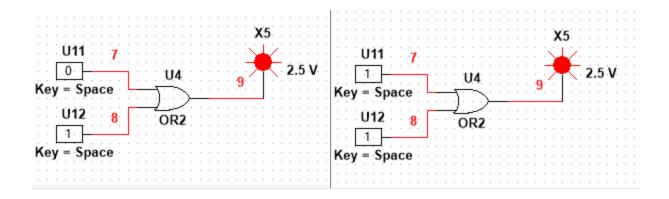
Simulation

AND Gate:

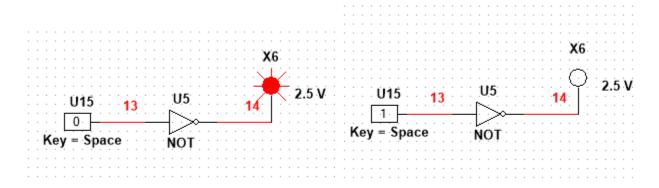


OR Gate

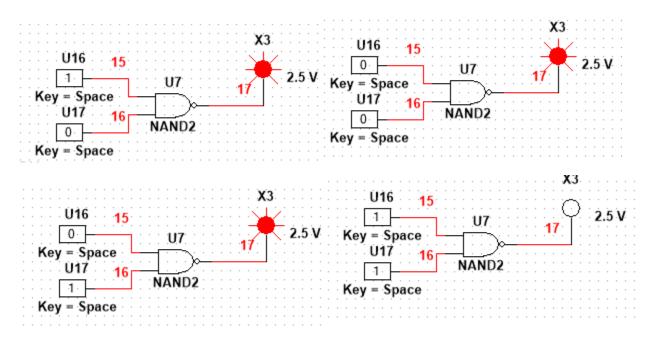




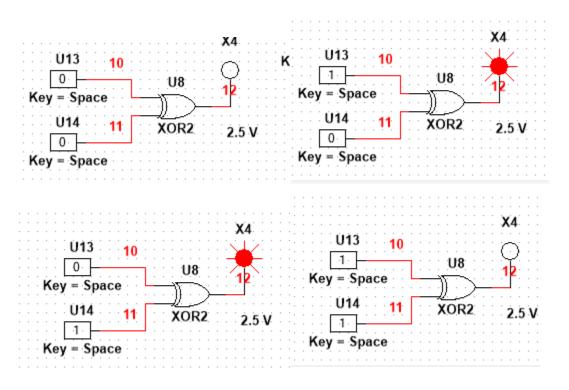
NOT Gate



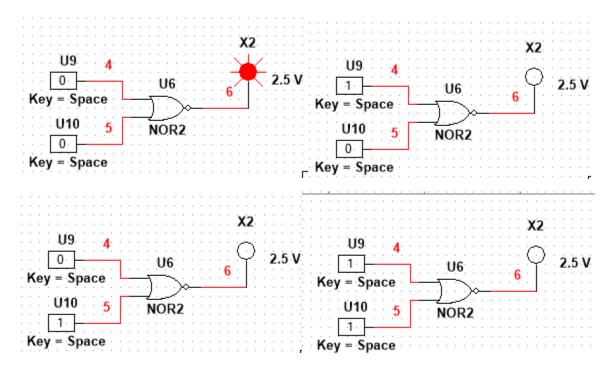
NAND



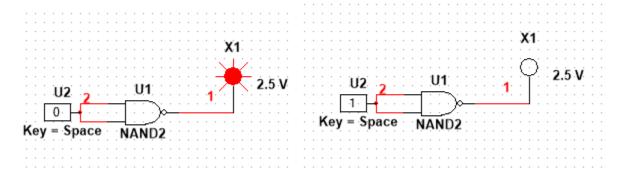
XOR



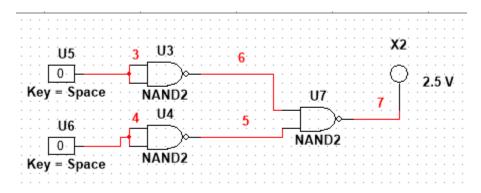
NOR



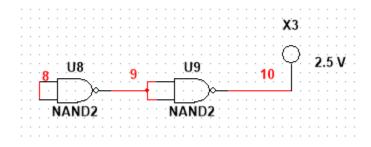
NOT gate Using NAND



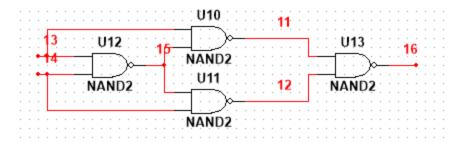
OR gate Using NAND



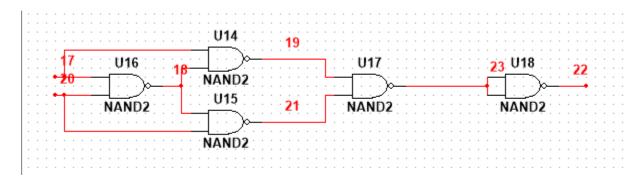
AND gate Using NAND



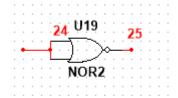
XOR gate Using NAND



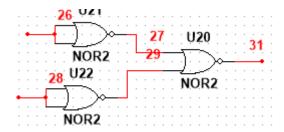
XNOR gate Using NAND



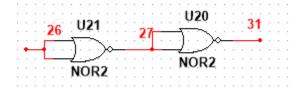
NOT gate Using XOR



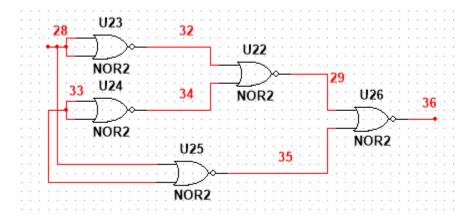
AND gate Using XOR



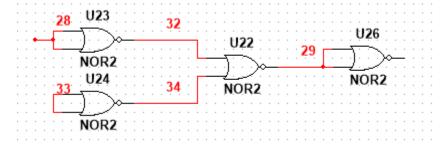
OR gate Using NOR



XNOR gate Using NOR



XOR gate using NOR



Discussion: The term logic referes to a human reasoning. That enables to us to make various conditional Proposition such as "This statement is thue" "I various digital logic gates act on various valtage level. 3 fundamental gates are AND. OR and NOT and NAND and NOR are universal gates. XOR and XNOR are exclusive gate.

In this experiment, we have seen various Ic acts according to its logical input. It acts according to its logical input. It acts according to its logic gates. In a Ic, there are various logic gates. In AND, OR, NET XOR, XNOR, NANDER gates are assigned into it. For them, Pin Mo. are input and 3, 6 11 are output. Not gate input and 3, 6 11 are output. Not gate input is 1,3,5,9,11,13 and output lines in put is 1,3,5,9,11,13 and output lines are 2,4,6,48,10,12. It is consider as are 2,4,6,48,10,12. It is consider as are ground and 14 is consider as are power input. Anside digital board, we have connected the wines and pins according to it and to see the output we have connected the into the digital board. The

board switch. The Combination of inputs depend only on the Present input "[2]. During experiment, the Pin Configuration understanding is very much important as the input outputs are very much likely related to this. During experiment, some facinable were not functioning experiment, some facinable of excessive use Properly due to pin damage or excessive use of circuits during its diffetime. The Fren digital of circuits during its diffetime. The Fren digital of contract board output side may not show the contract board output side may not show the contract answer. To get raid of this, P Ta chips answer. To get raid of this, P Ta chips answer to be update regularly, new Pins need to be added and use of low voltage should be added and use of low voltage and to be ensured.

The experiment, however was a success, the still the tresult may not be loo percent contrect due to some fault. But it can be consider as minor fault and the enror percentage maybe 0.03% which is negrable.

Condusion:

To verify various logic circuits using digital board. In the theorytical truth table, and experimental truth table shows the same tresult. So, we can say that we have achived the goal and digital gates are verified.

I Remarcks:

- (i) Digital gates acts differently in various
- the way they are amounted in PCB
- (iii) Ic fin numbers are assigned into articlock wise motorion.
- M OR gate acts like Panauer scincuit
- (vi) AND gate acts like series cincuit
- (vii) Not gate is a complement gate.

 (viii) I cis designed with multiple logic circuits.

List of the femence:

[1] Digital Logie and Computer design

[M. Zafrul Mulk] [Poseg, 19,21] [Ist edition]

2. Digital Fundamentals [James Floyed].