Experiment:03:

Name of the experiment: Design of Adder, subtractor and comparator circuit.

Group no:03

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Student id: 20-42119-1

Course title: Digital Logic and Circuit Lab

Section: M

Date of experiment: 09/06/2022

Date of Submission: 15/06/2022

Objective of the experiment:

(i) To see how adder, subtractor and comparator works and verify the truth table
(ii) Observing the application of integral circuit
(iii) To make complex circuit from bodean expression

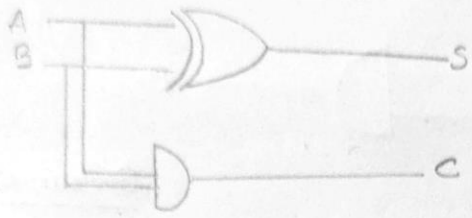
List of components:

(i) Trainer board
(ii) IC
(iii) Wires

IC:

IC 7408
IC 7432
IC 7404
IC 7486
IC 74

Symbol, block diagram and figures:

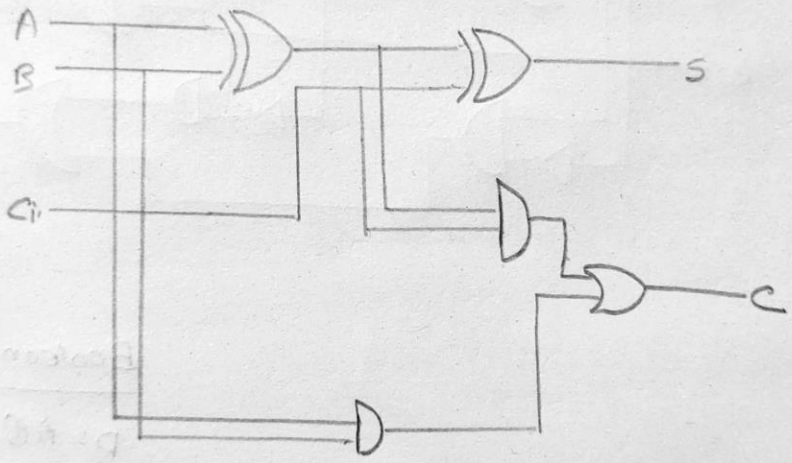


Half adder

Boolean expression

$S = A \oplus B$

$C = AB$

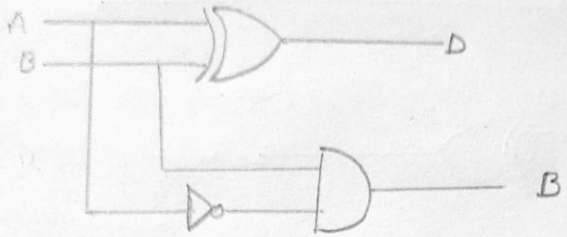


Boolean -

$S = A \oplus B \oplus Cin$

$C = Cin(A \oplus B) + AB$

Fun adder

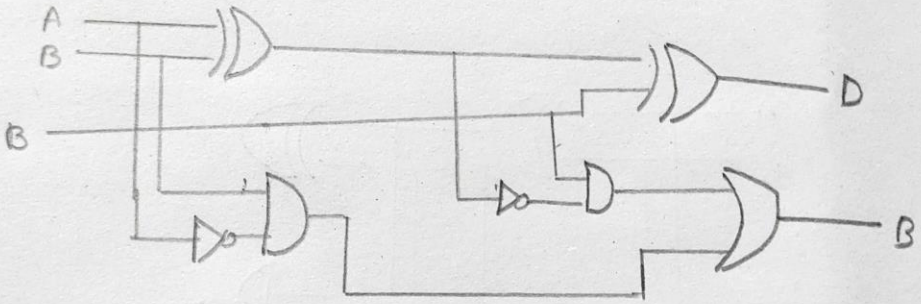


Boolean expression:

$D = A \oplus B$

$B = \bar{A}B$

Half Substraction

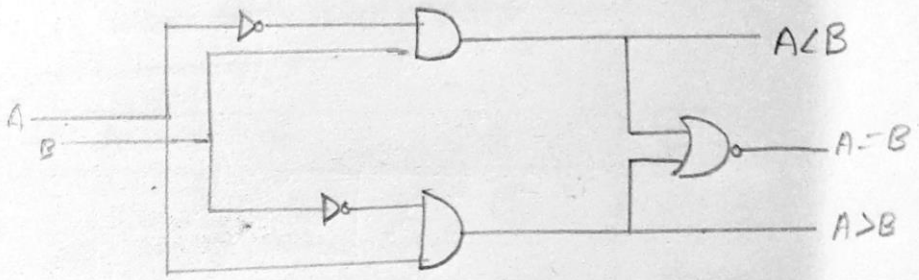


Boolean Expression

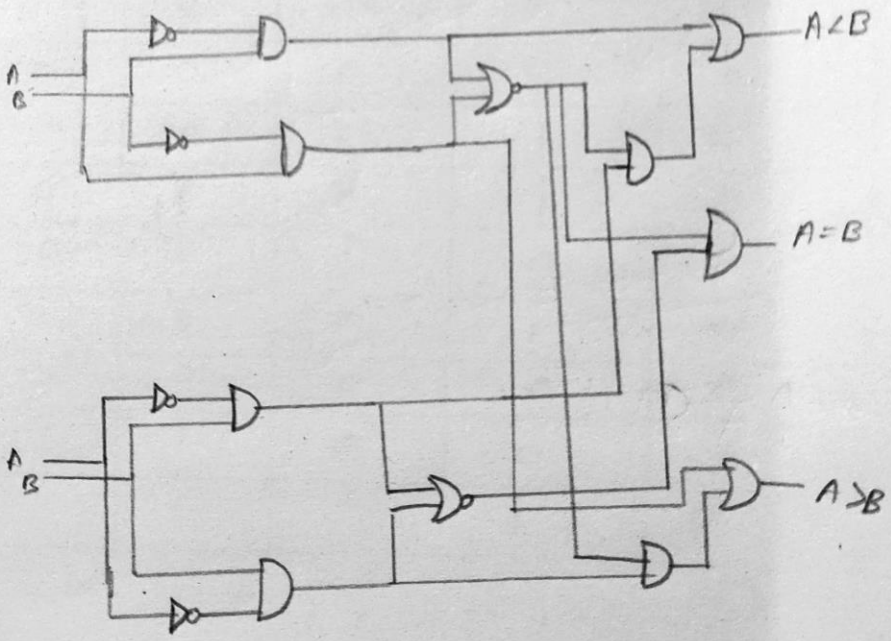
$D = A \oplus B \oplus C$

$B_{out} = \bar{A}B + \bar{A}B_{in} + BB_{in}$

Fum Substraction.



1 Bit comparator.



2 bit comparator

Data table:

Truth table for Half adder:

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Truth table for Full adder:

A	B	Cin	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	0
1	0	0	1	0
1	0	1	0	0
1	1	0	0	1
1	1	1	1	0

Half substraction:

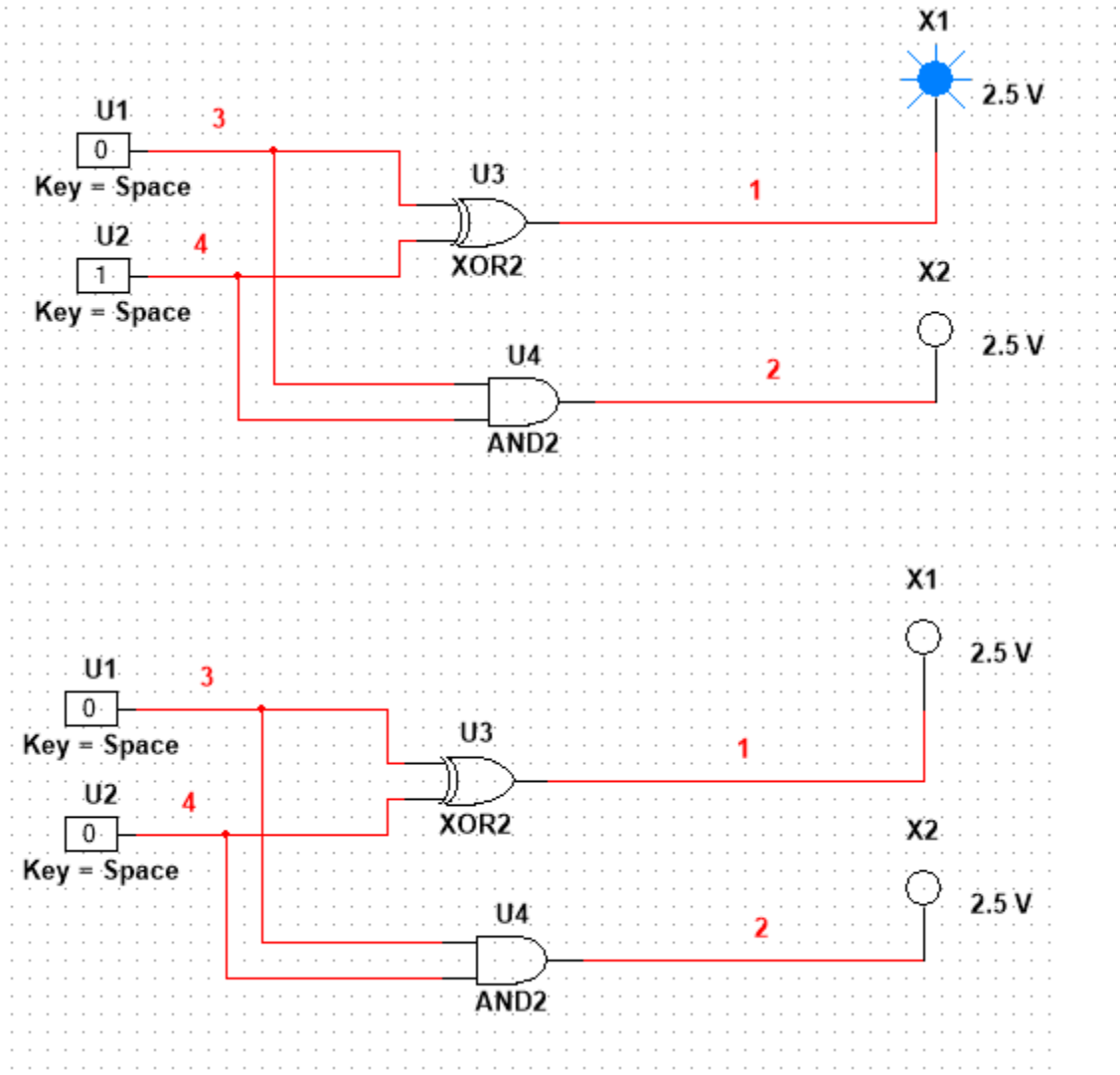
A	B	D	B
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

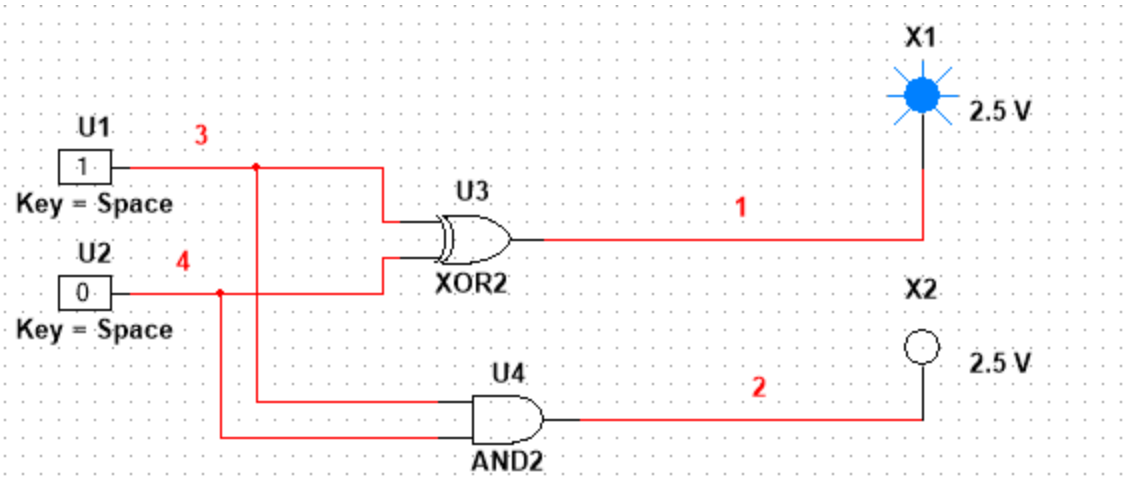
Full Substraction:

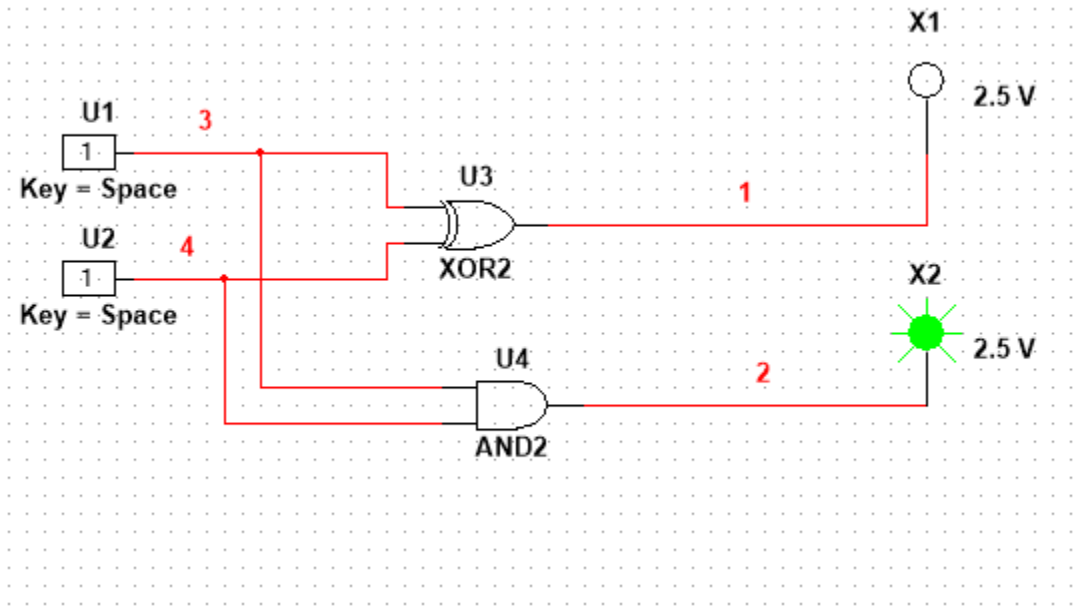
A	B	Bin	D	Bout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	0

Simulation

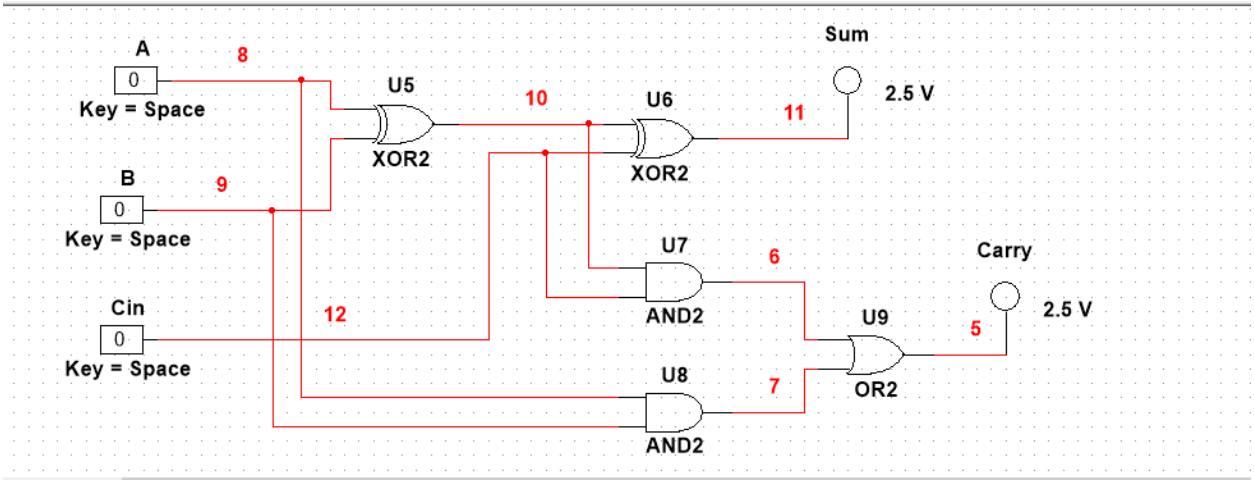
Half Adder Simulation:

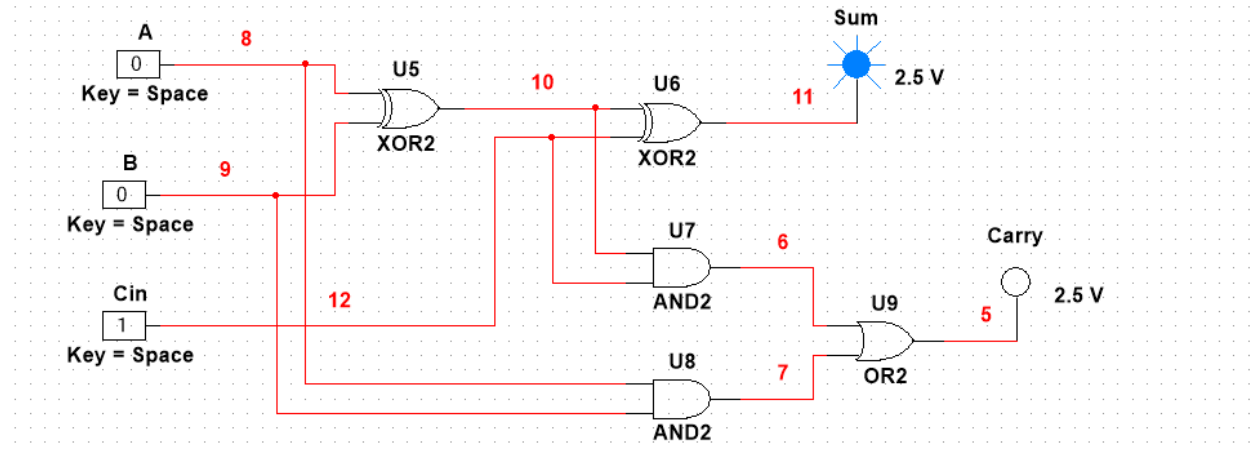


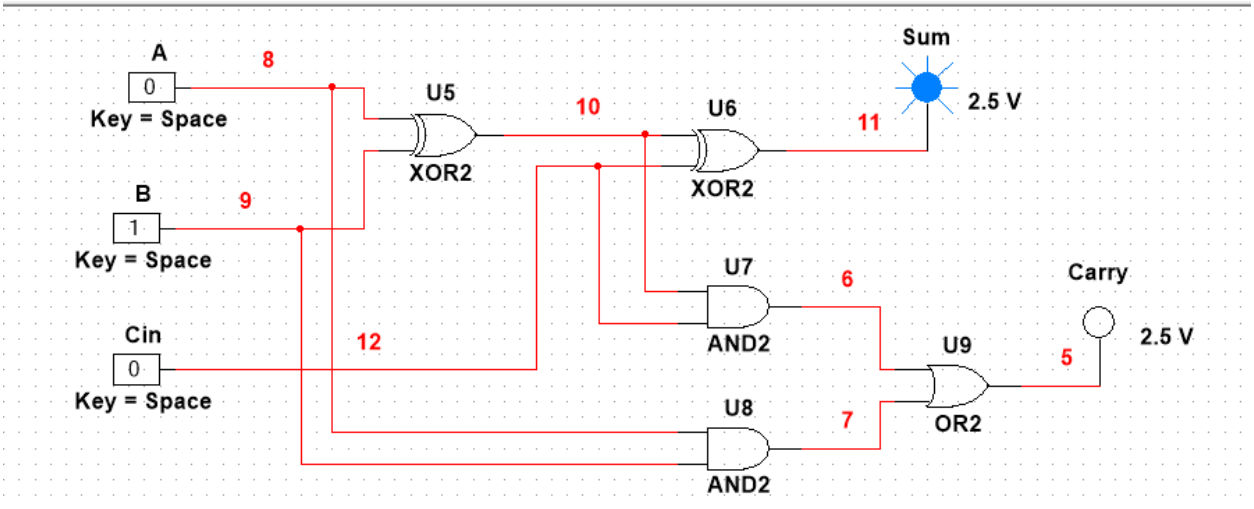

X1
2.5 V
U1
3
1
Key = Space
U3
1
U2
4
0
Key = Space
XOR2
X2
2.5 V
U4
2
AND2

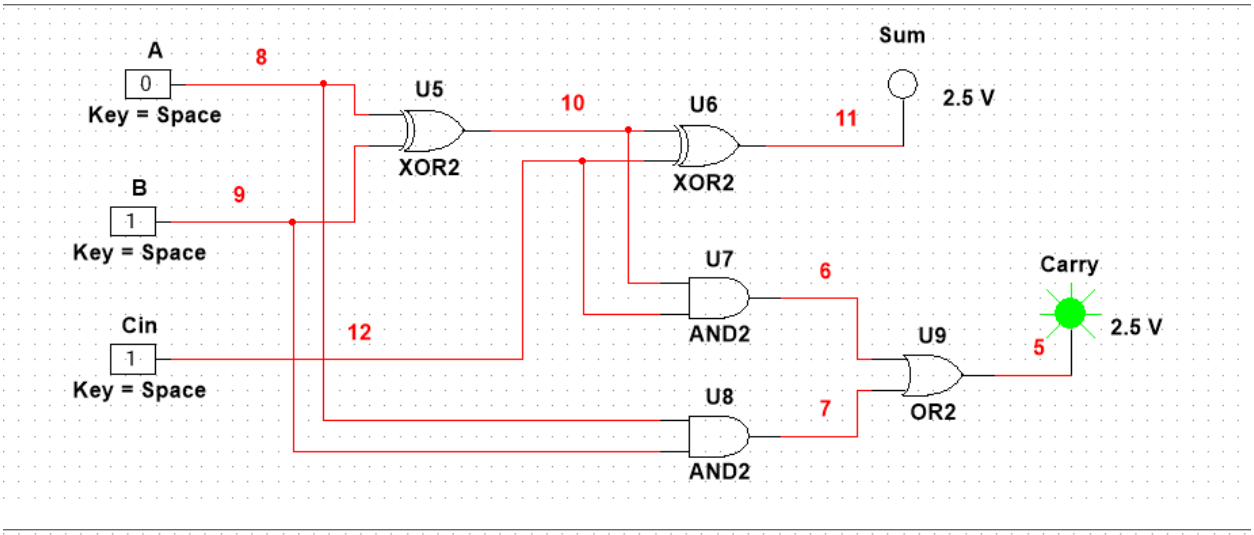

X1
2.5 V
U1
3
1
Key = Space
U3
1
U2
4
1
Key = Space
XOR2
X2
2.5 V
U4
2
AND2

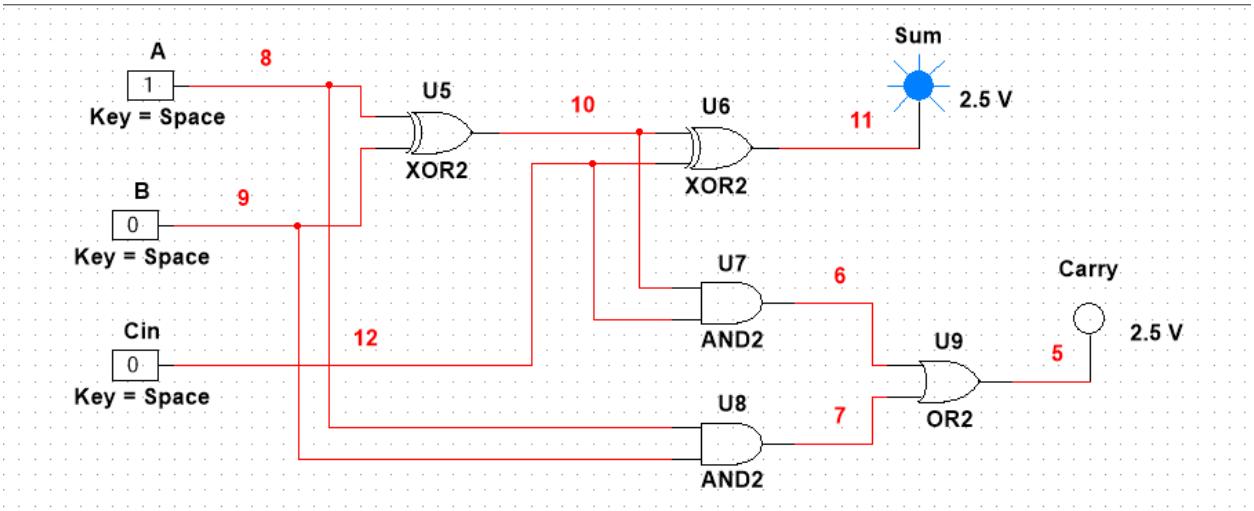
Full Adder Simulation:








A
0
Key = Space
8
B
1
Key = Space
9
Cin
1
Key = Space
12
U5
XOR2
10
U6
XOR2
11
Sum
2.5 V
U7
AND2
6
U8
AND2
7
U9
OR2
5
Carry
2.5 V


A
1
Key = Space
8
B
0
Key = Space
9
Cin
0
Key = Space
12
U5
XOR2
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XOR2
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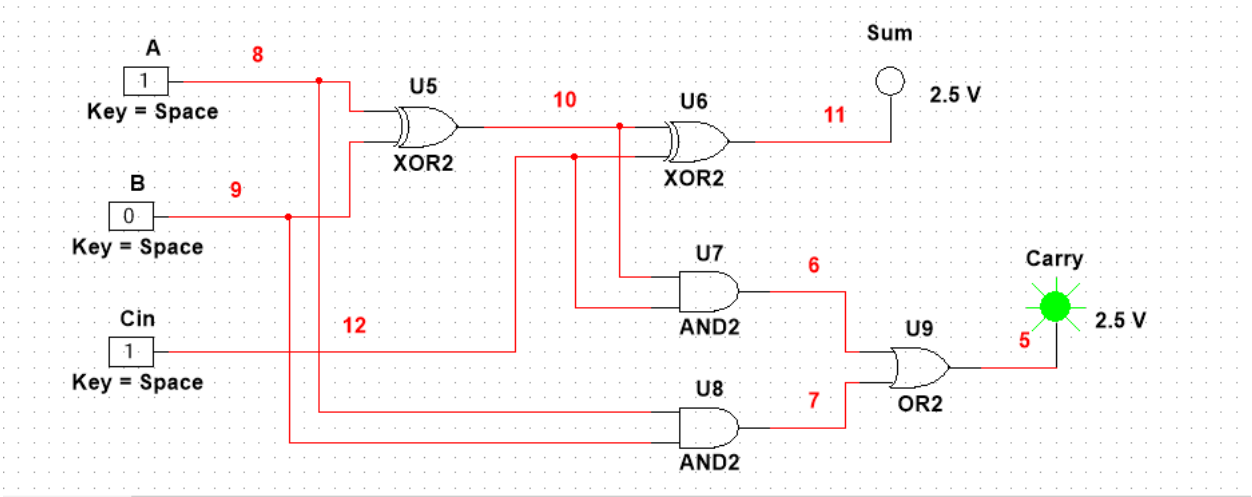
U8
AND2
7
U9
OR2
5
Carry
2.5 V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Key = Space
B
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Key = Space
Cin
1
Key = Space
8
9
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U5
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XOR2
11
Sum
2.5 V
U7
AND2
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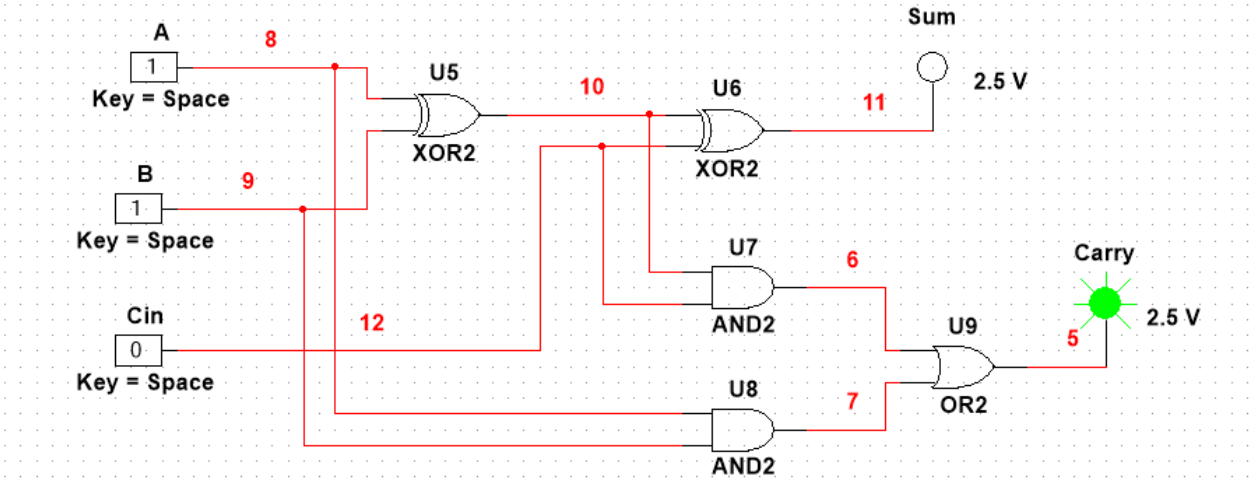
U8
AND2
7
U9
OR2
5
Carry
2.5 V


A
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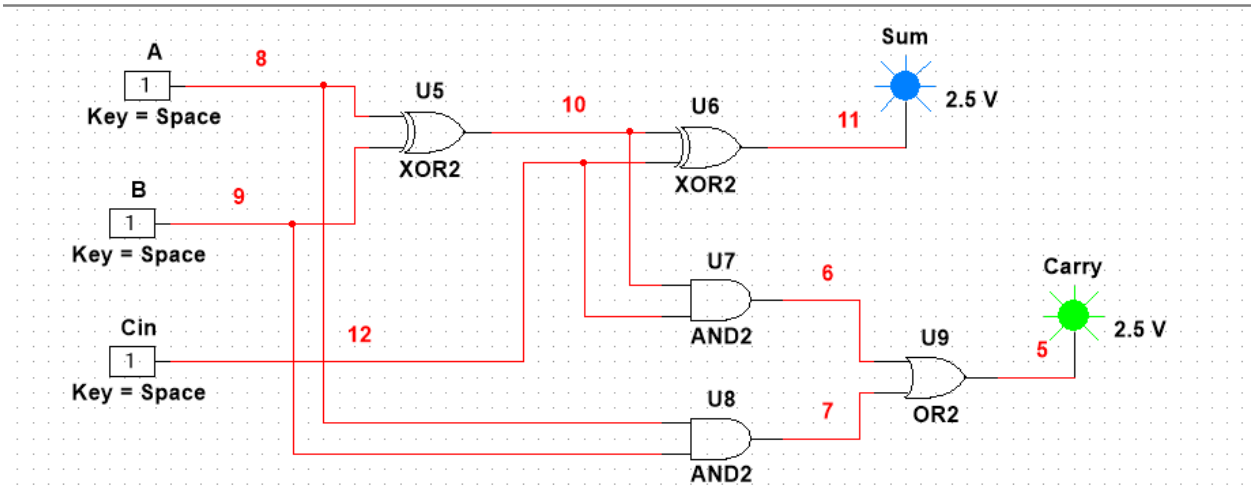
Key = Space
B
1
Key = Space
Cin
0
Key = Space
8
9
12
U5
XOR2
10
U6
XOR2
11
Sum
2.5 V
U7
AND2
6
U8
AND2
7
U9
OR2
5
Carry
2.5 V


A
1
Key = Space
B
1
Key = Space
Cin
1
Key = Space
8
9
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U5
XOR2
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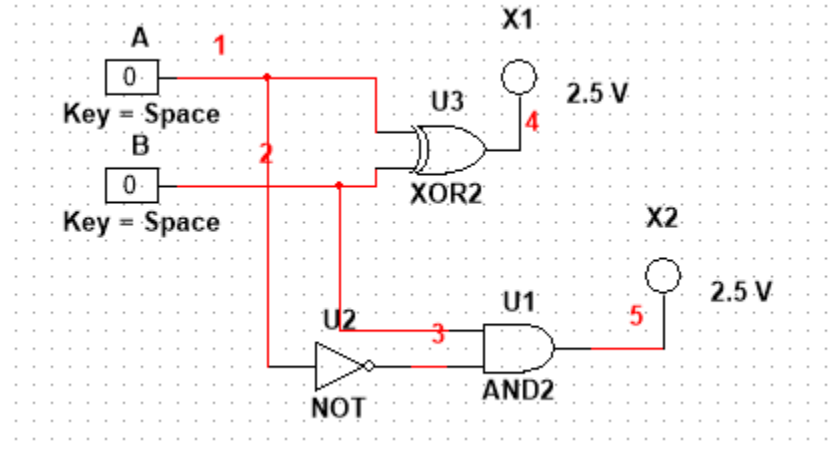
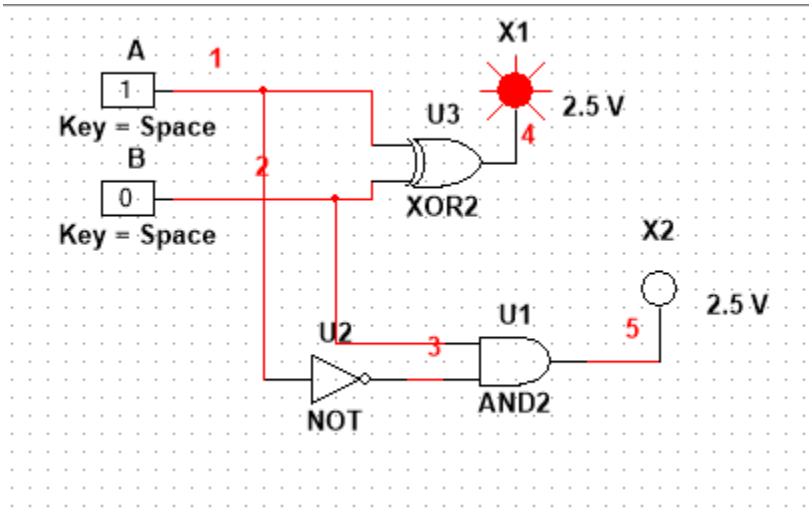
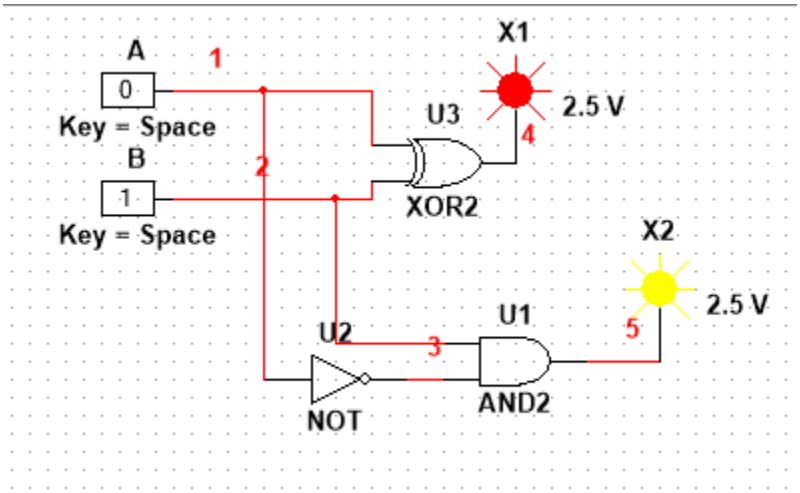
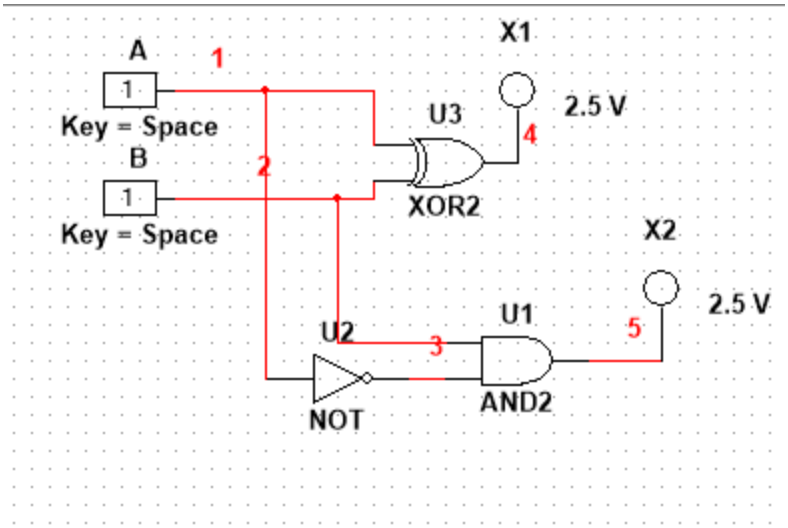
U6
XOR2
11
Sum
2.5 V
U7
AND2
6
U8
AND2
7
U9
OR2
5
Carry
2.5 V

Half Subtractor:

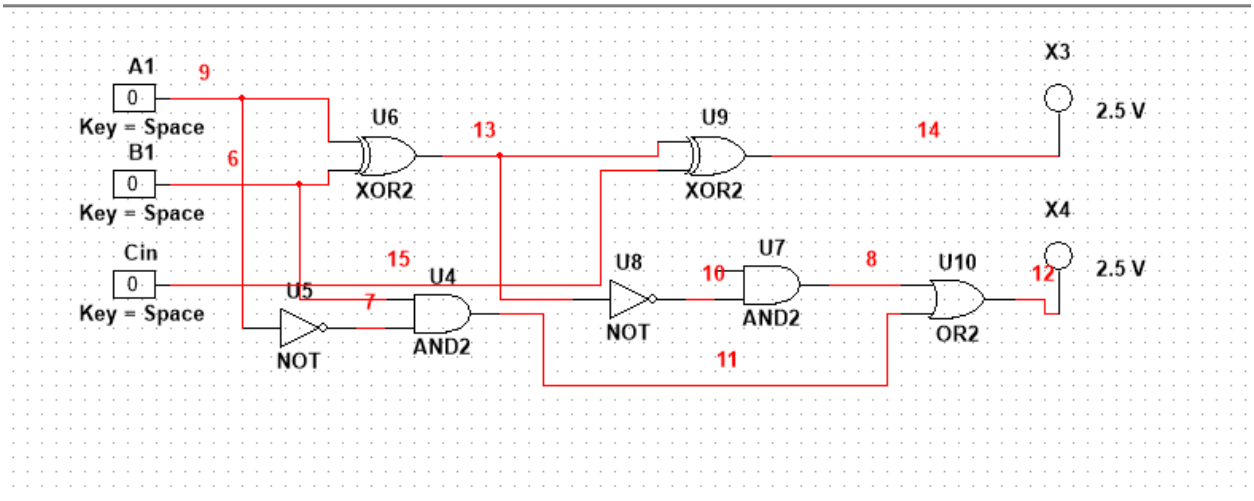


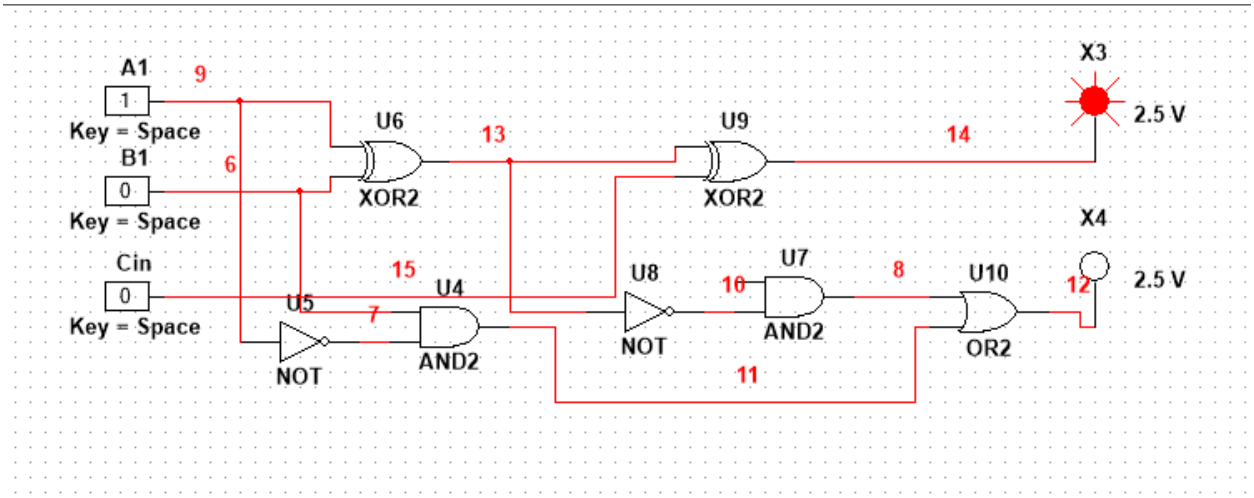


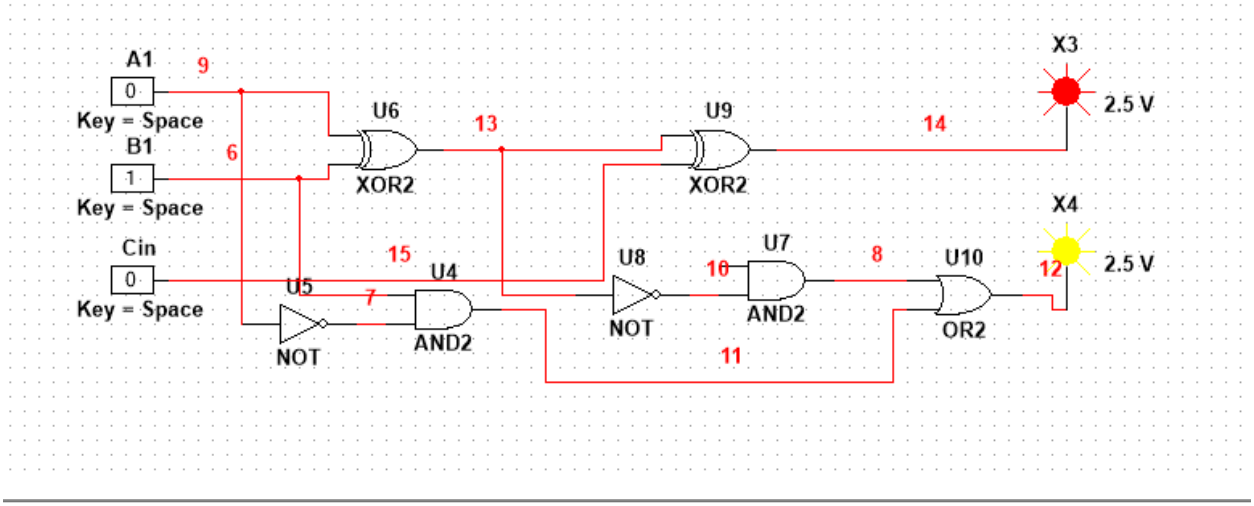


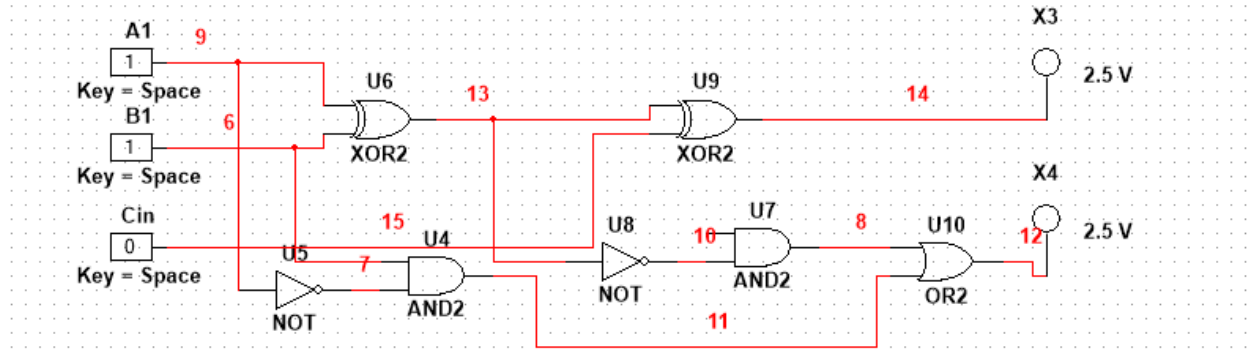


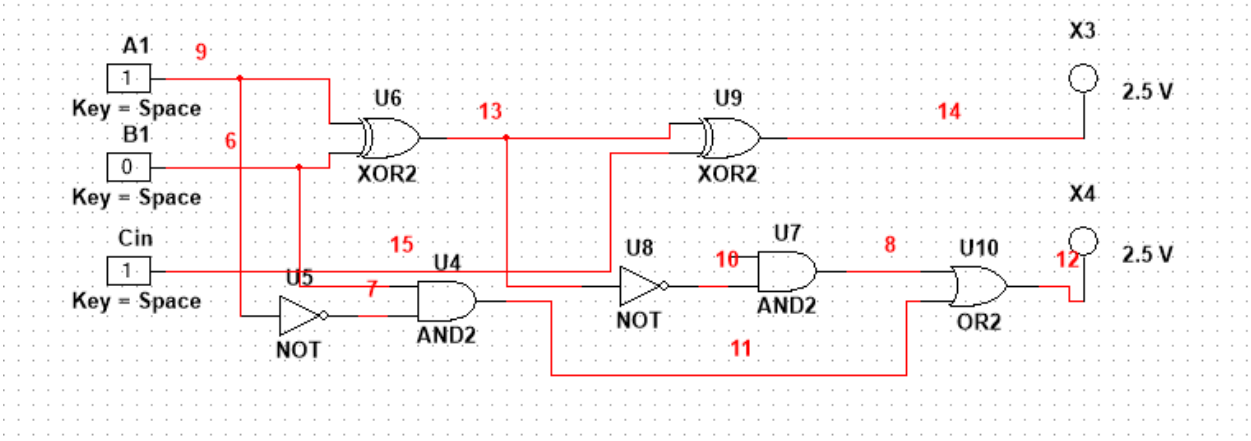
Full Subtractor:






A1
0
Key = Space
B1
1
Key = Space
Cin
0
Key = Space
9
6
15
7
13
14
11
8
10
12
U6
XOR2
U9
XOR2
U5
NOT
U4
AND2
U8
NOT
U7
AND2
U10
OR2
X3
2.5 V
X4
2.5 V


A1
1
Key = Space
B1
1
Key = Space
Cin
0
Key = Space
9
6
15
7
13
14
11
8
10
12
U6
XOR2
U9
XOR2
U5
NOT
U4
AND2
U8
NOT
U7
AND2
U10
OR2
X3
2.5 V
X4
2.5 V


A1
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B1
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Cin
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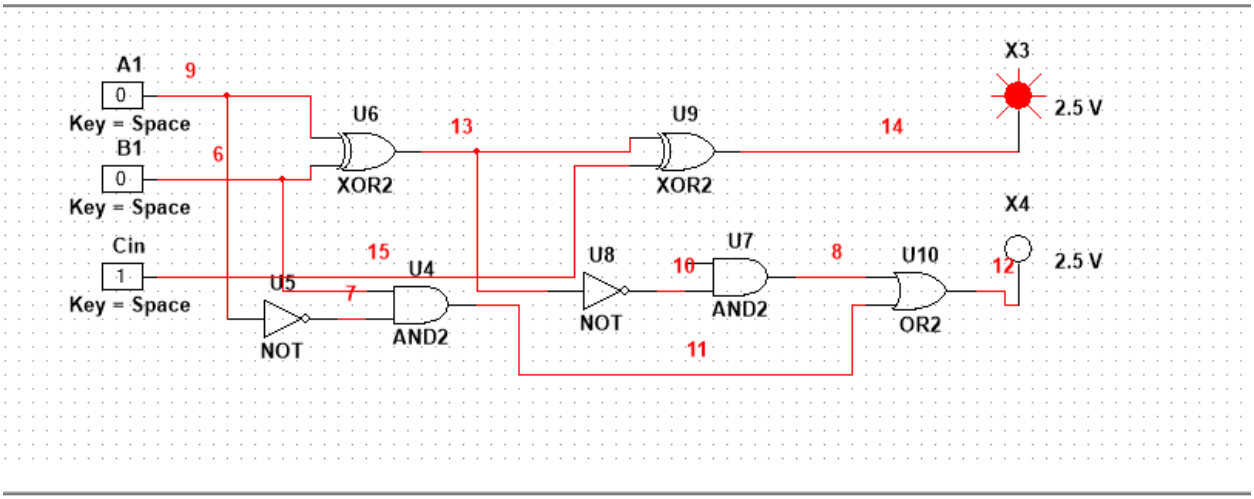
11
8
10
12
U6
XOR2
U9
XOR2
U5
NOT
U4
AND2
U8
NOT
U7
AND2
U10
OR2
X3
2.5 V
X4
2.5 V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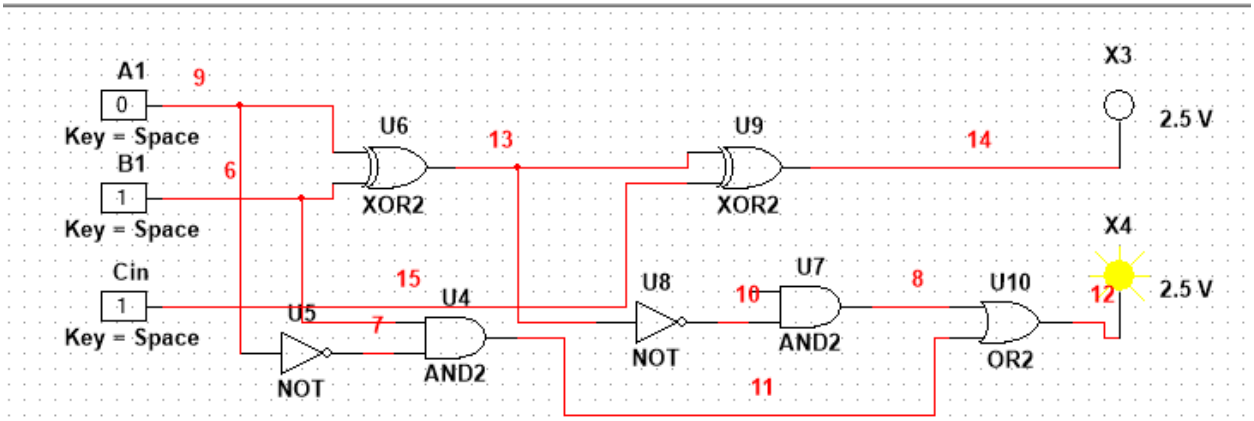
Key = Space
B1
0
Key = Space
Cin
1
Key = Space
9
6
15
7
13
11
14
8
16
12
U6
XOR2
U9
XOR2
U5
NOT
U4
AND2
U8
NOT
U7
AND2
U10
OR2
X3
2.5 V
X4
2.5 V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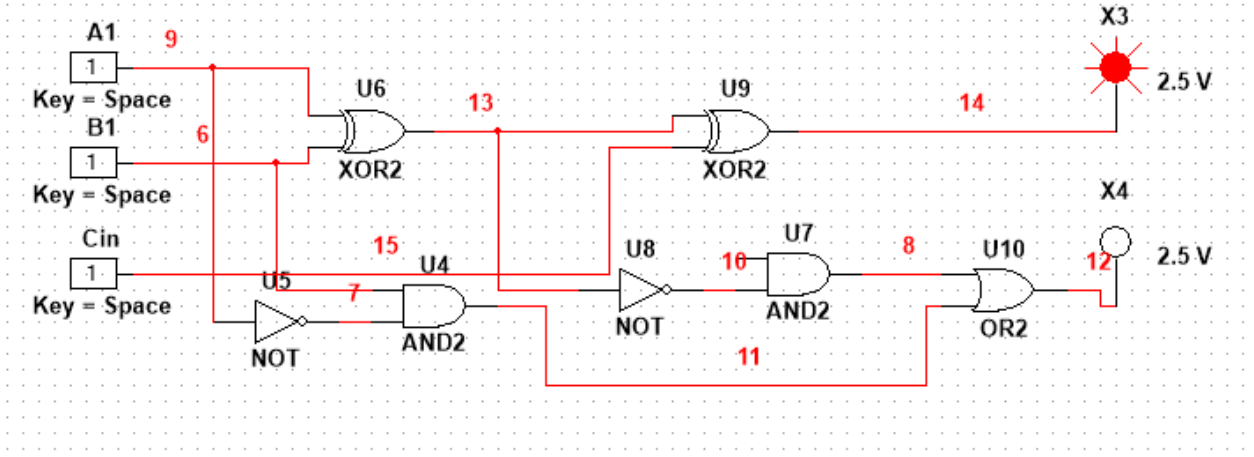
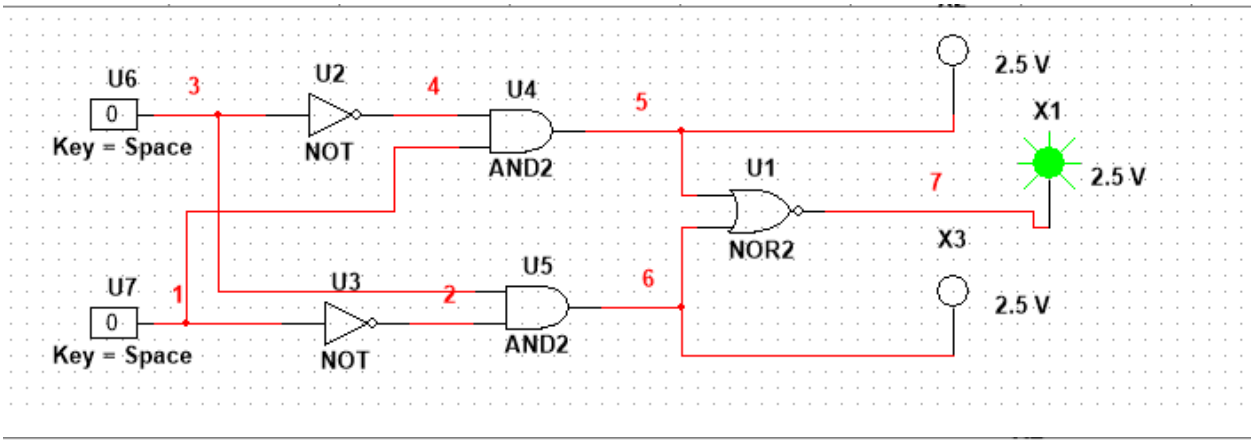
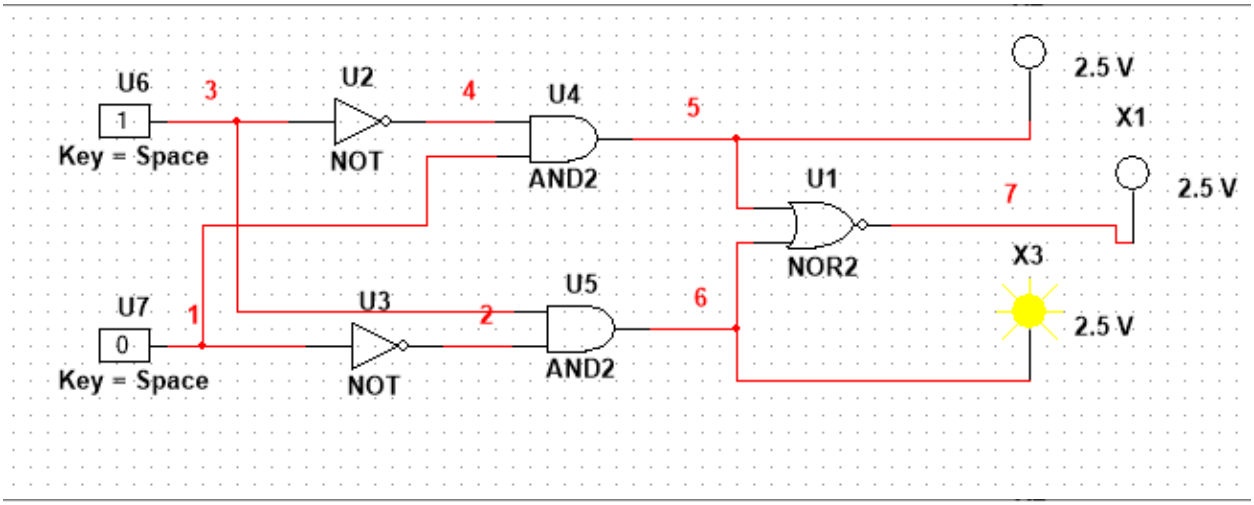
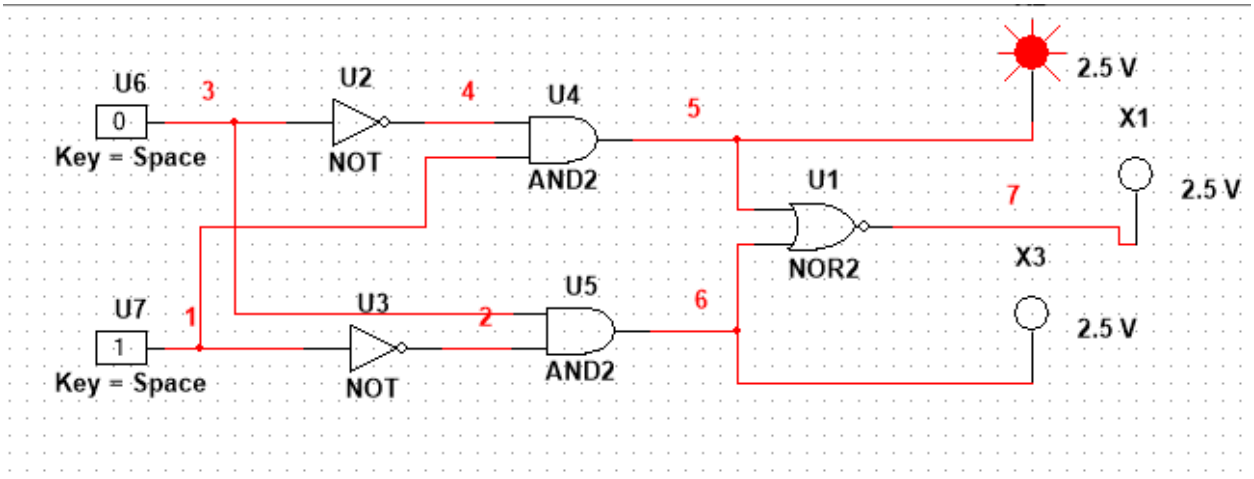
0
Key = Space
B1
1
Key = Space
Cin
1
Key = Space
9
6
15
7
13
11
14
8
16
12
U6
XOR2
U9
XOR2
U5
NOT
U4
AND2
U8
NOT
U7
AND2
U10
OR2
X3
2.5 V
X4
2.5 V

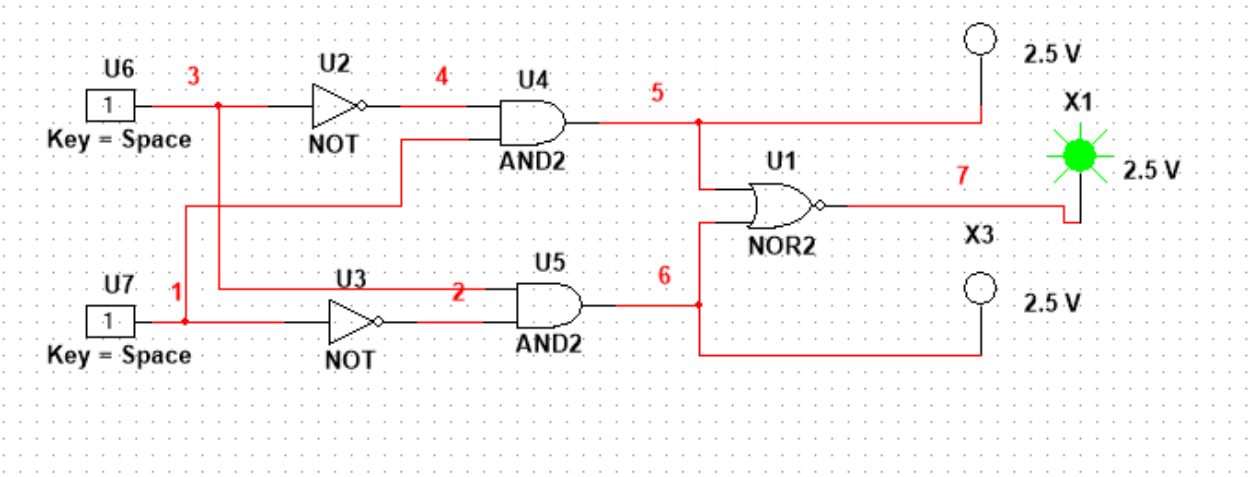

A1
1
Key = Space
B1
1
Key = Space
Cin
1
Key = Space
9
6
15
7
13
11
14
8
16
12
U6
XOR2
U9
XOR2
U5
NOT
U4
AND2
U8
NOT
U7
AND2
U10
OR2
X3
2.5 V
X4
2.5 V

1 bit Comparator:

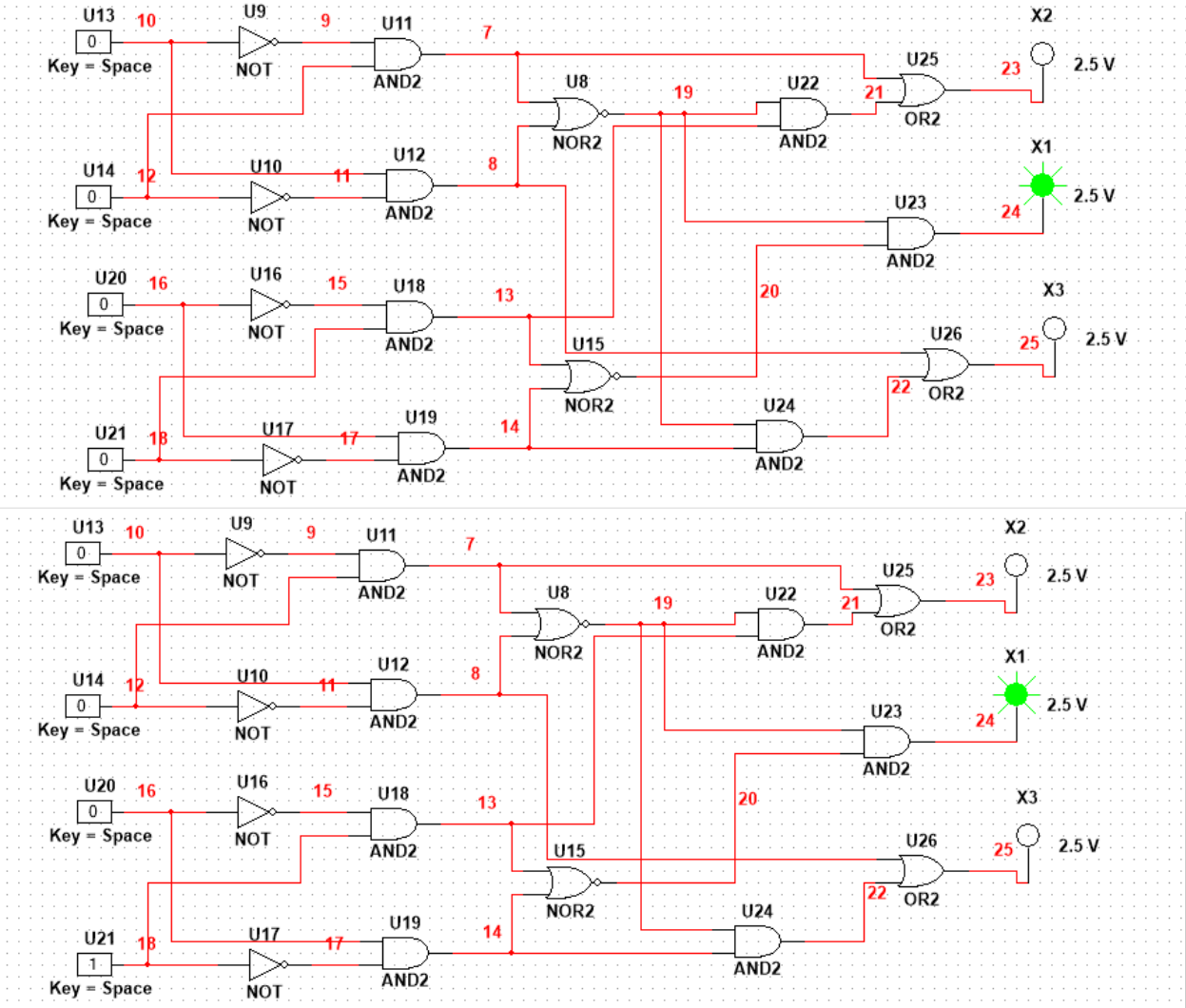


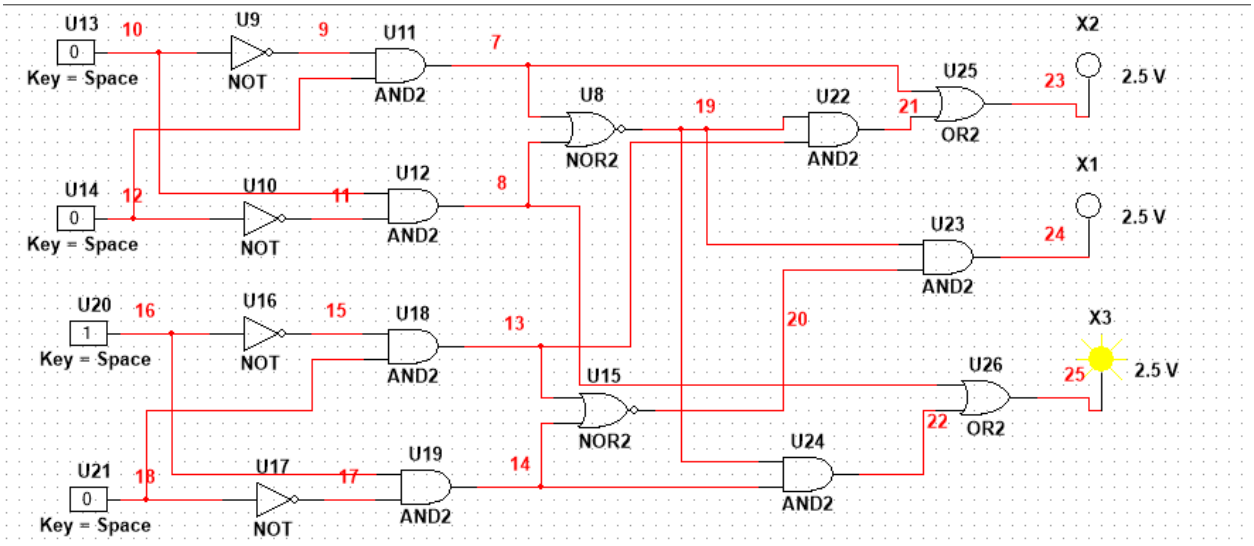


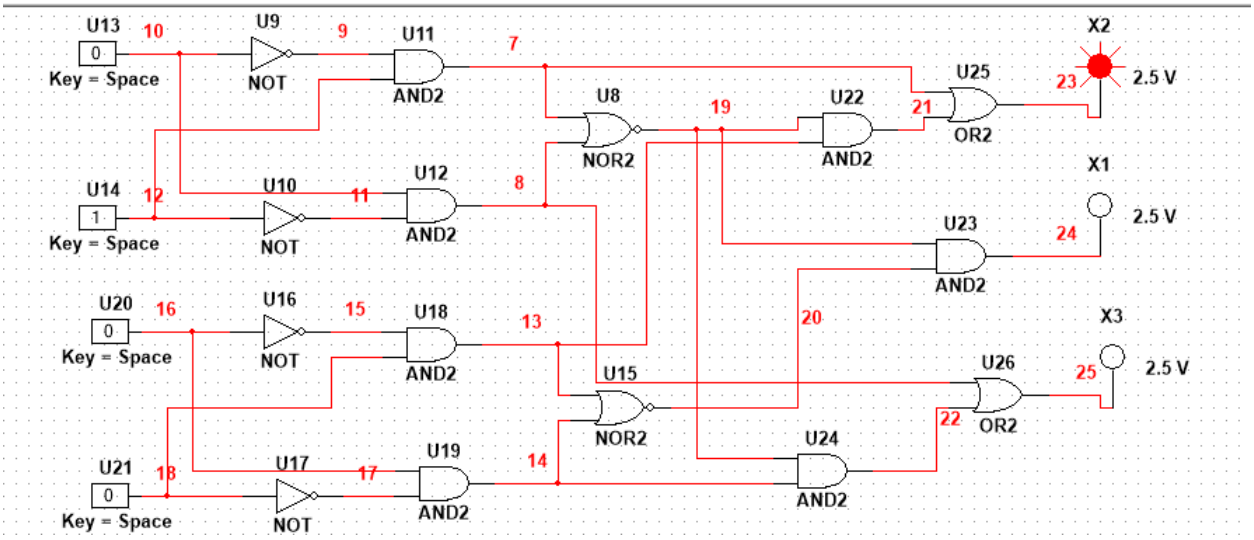


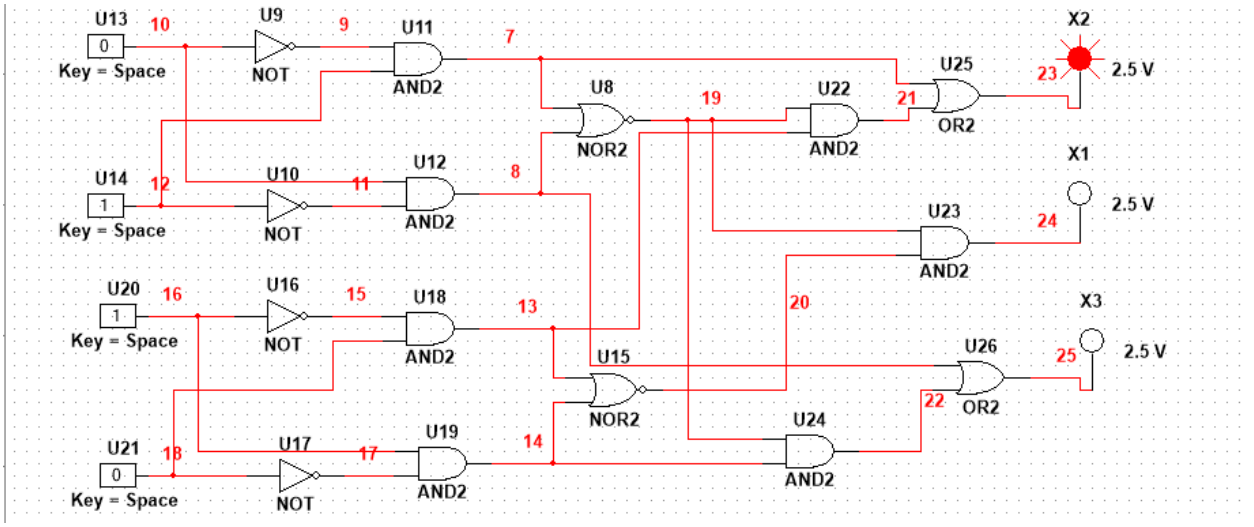


2-bit Comparator:




U13
0
Key = Space
10
U9
NOT
9
U11
AND2
7
U8
NOR2
19
U22
AND2
21
U25
OR2
23
X2
2.5 V
U14
0
Key = Space
12
U10
NOT
11
U12
AND2
8
X1
2.5 V
U23
AND2
24
U20
1
Key = Space
16
U16
NOT
15
U18
AND2
13
20
X3
2.5 V
U15
NOR2
U26
OR2
25
22
U21
0
Key = Space
18
U17
NOT
17
U19
AND2
14
U24
AND2


U13
0
Key = Space
10
U9
NOT
9
U11
AND2
7
U8
NOR2
19
U22
AND2
21
U25
OR2
23
X2
2.5 V
U14
1
Key = Space
12
U10
NOT
11
U12
AND2
8
X1
2.5 V
U23
AND2
24
U20
0
Key = Space
16
U16
NOT
15
U18
AND2
13
20
X3
2.5 V
U15
NOR2
U26
OR2
25
22
U21
0
Key = Space
18
U17
NOT
17
U19
AND2
14
U24
AND2


U13
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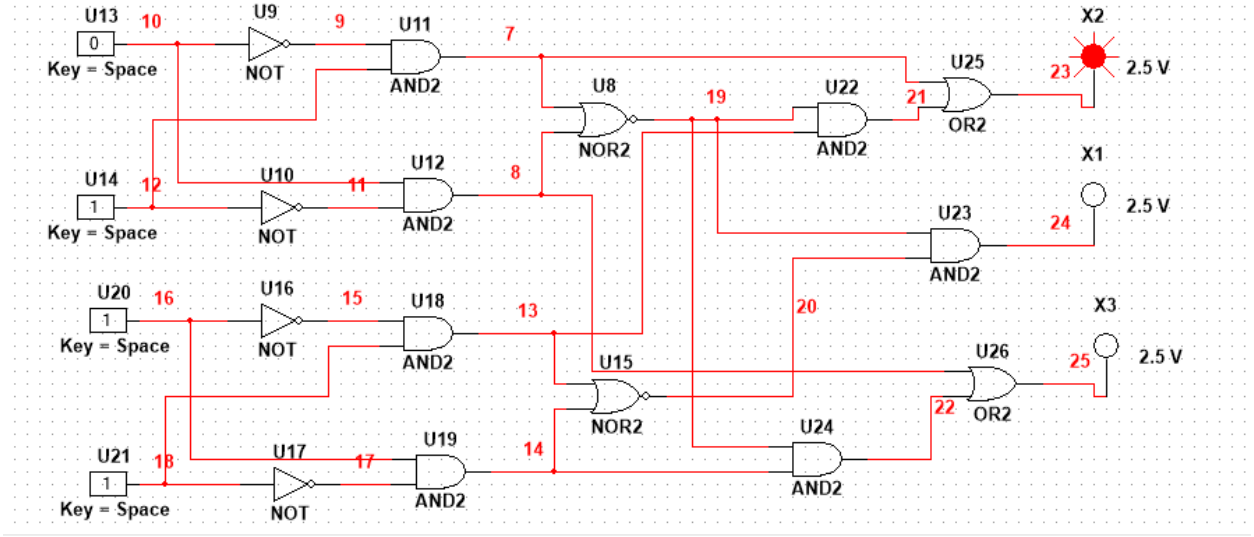
9
U11
AND2
7
U8
NOR2
19
U22
AND2
21
U25
OR2
23
X2
2.5 V
U14
1
Key = Space
12
U10
NOT
11
U12
AND2
8
X1
2.5 V
U23
AND2
24
U20
1
Key = Space
16
U16
NOT
15
U18
AND2
13
20
X3
2.5 V
U15
NOR2
U26
OR2
25
22
U21
0
Key = Space
18
U17
NOT
17
U19
AND2
14
U24
AND2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OR2
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X2
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U12
AND2
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U23
AND2
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X1
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1
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U16
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U18
AND2
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U15
NOR2
U26
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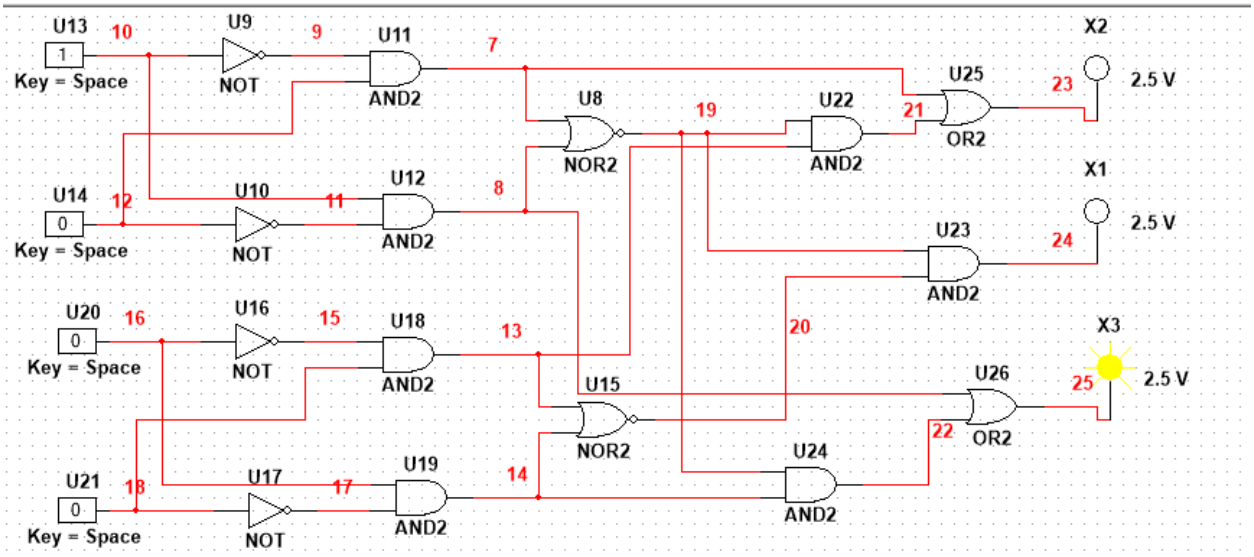
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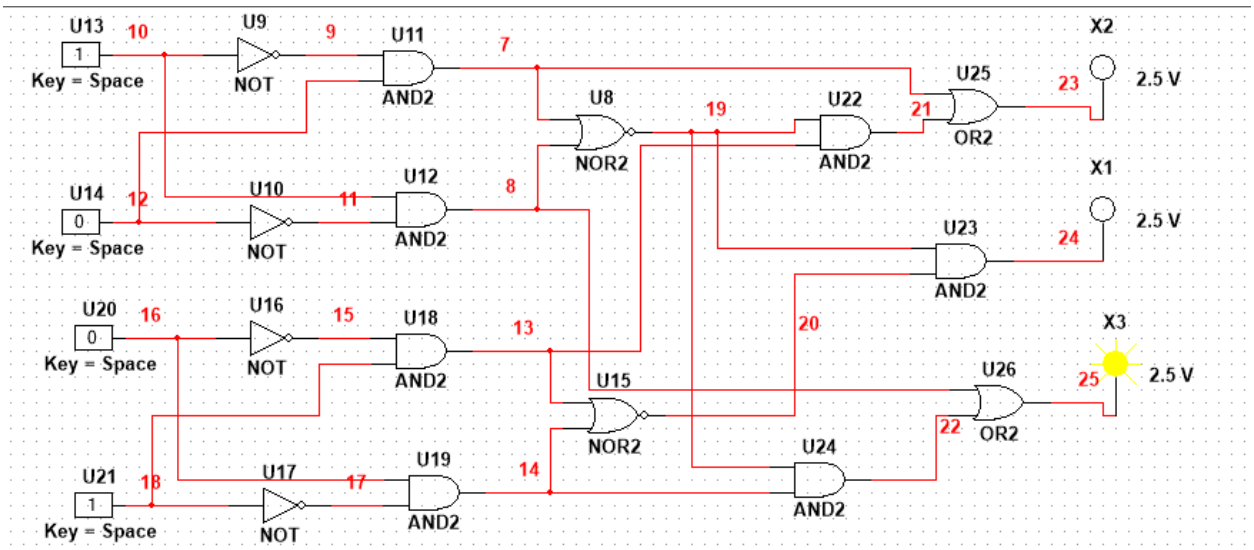
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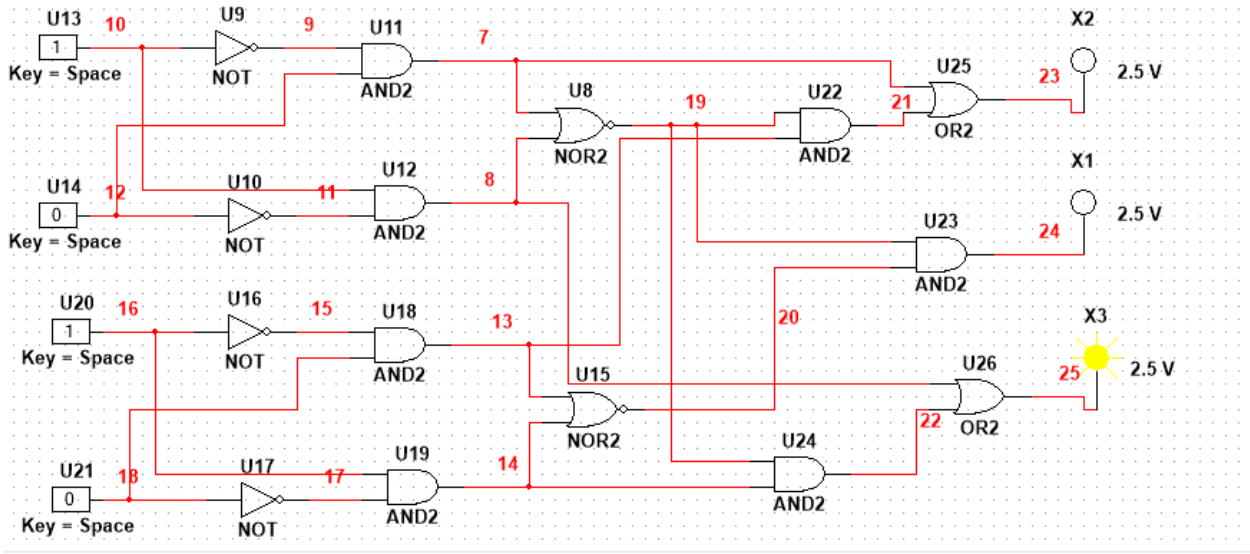
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Key = Space
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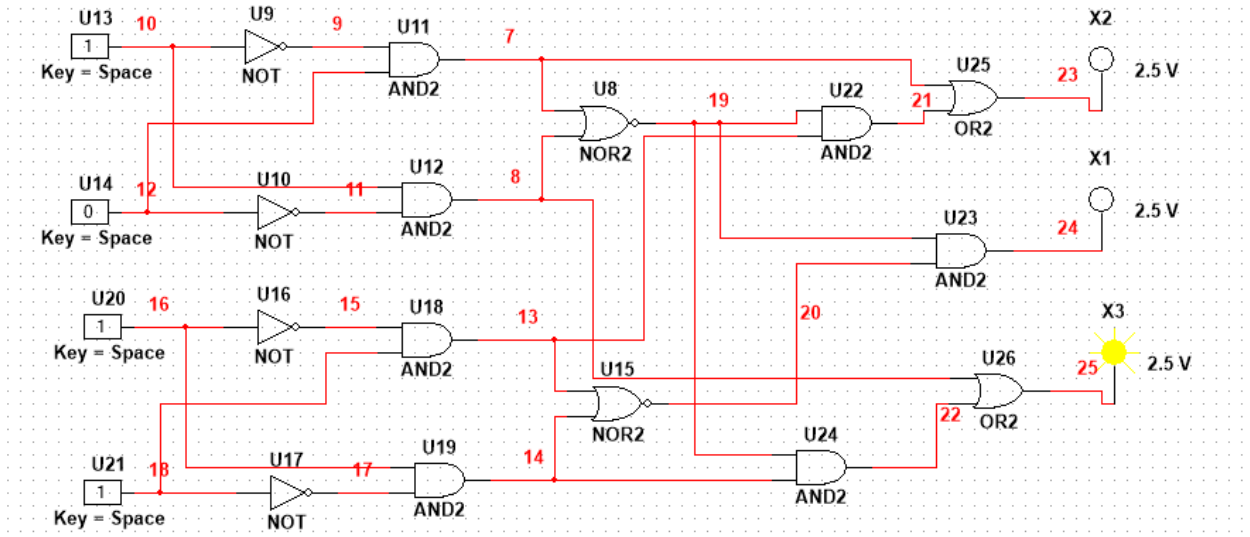
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X1
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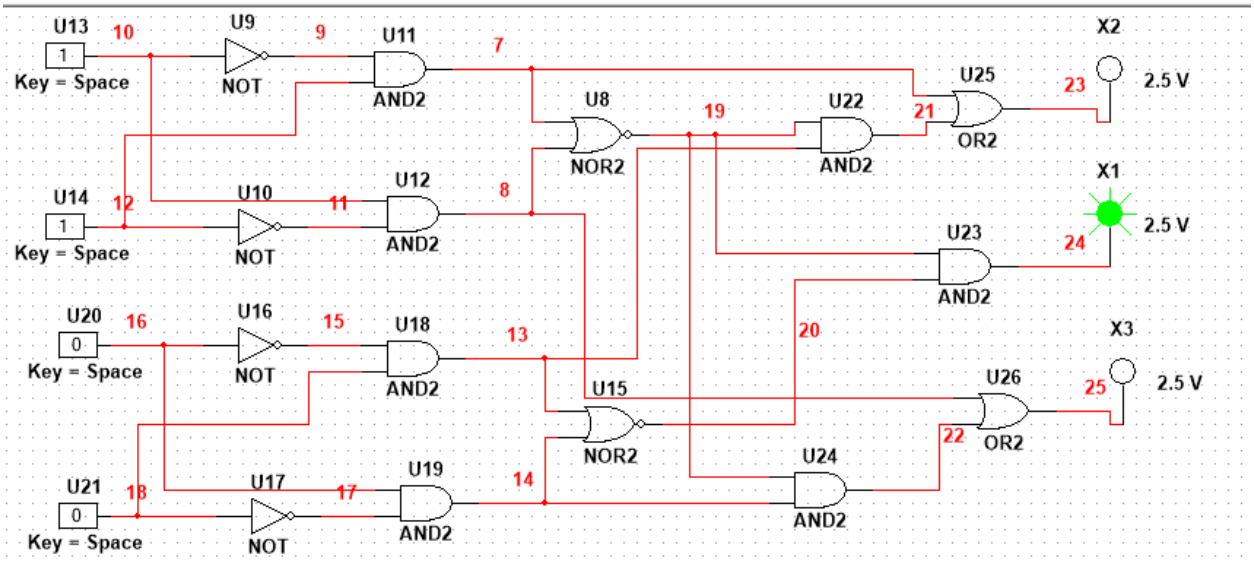
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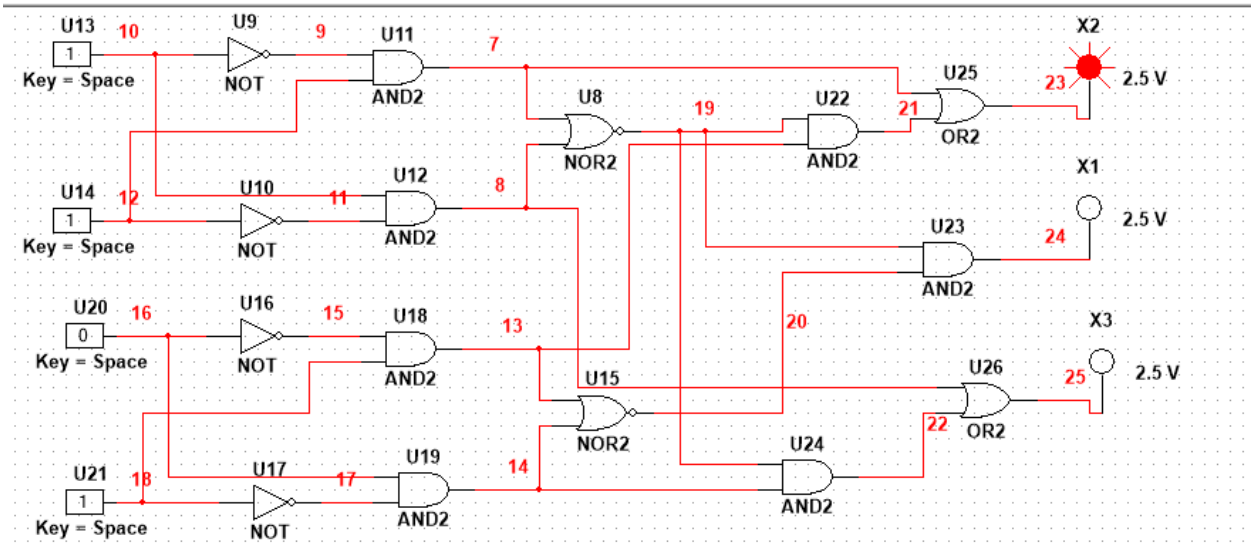
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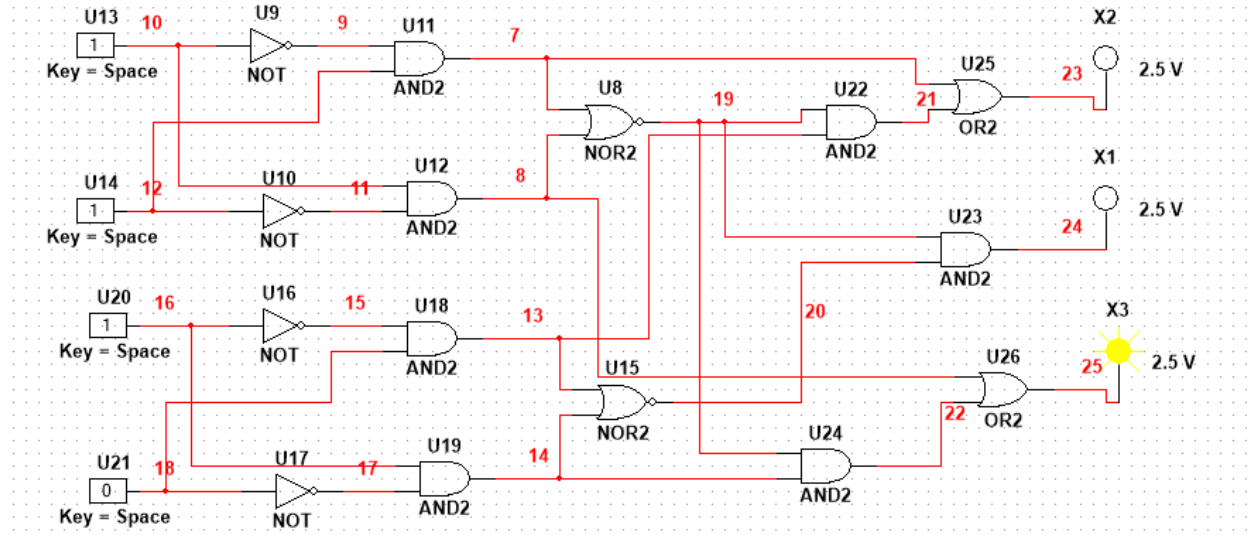
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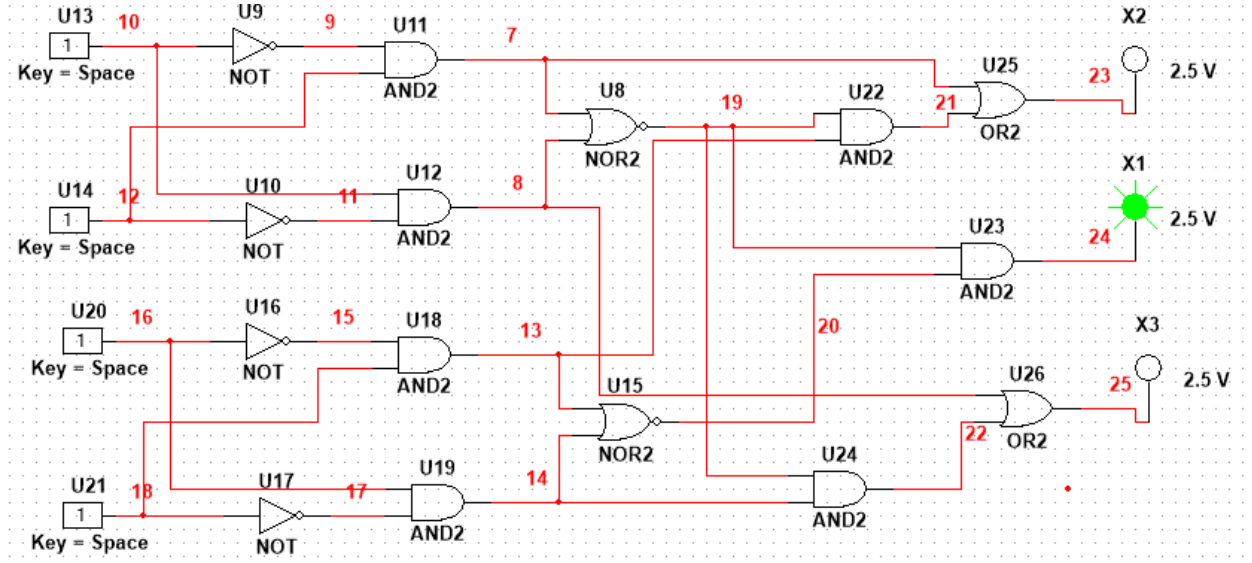
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Key = Space
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Discussion:

The experiment is about adder, subtractor and comparator. Adder is used for summing up various kind of digital logic and subtractor is used for various kind of subtraction. Comparator mainly compares the largest voltage among others. In this experiment, we mainly first build a truth table and follows the circuit. output from trainer board from various kinds of input. We mainly built half adder, full adder, half subtractor full subtractor and comparators

While building the circuit we find out that some IC pins were defected. Also. inside the ~~bread~~ breadboard, some alignment was not perfect.

But at the end, we find out the output which was matched with the truth tables. So, we can say that our goal of the experiment were successful.

Conclusion:

To verify the adder, subtractor and comparator, we have mainly used IC7408, IC7432 and IC7404. We solved a boolean function for developing the truth table. The output was verified.

Remarks:

(i) Adders are mainly use for adding some boolean logic and subtractor are used for substitution of boolean logic.

(ii) Comparator are used for comparing voltages

(iii) Adder and subtractor are mainly used for arithmatic operation and comparator is used for computer logic.

Reference:

[1] Tomas: L. Floyd "Digital Fundamentals" 11th edition, 2015.