Experiment NO: 07

Name: Implementation of Asynchronous and Synchronow Counters using flip flop

Group number. 03

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Course Title: Digital logic and circuit lab

Section: M

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Objective of the experiment: To understand the basic action of the J-K flip flop and D-flip flop and their truth table.

List of the components:

IC 7474 (D-flip flop)
IC 7476 (J-K flip flop)

Symbols, block diagram and figures:

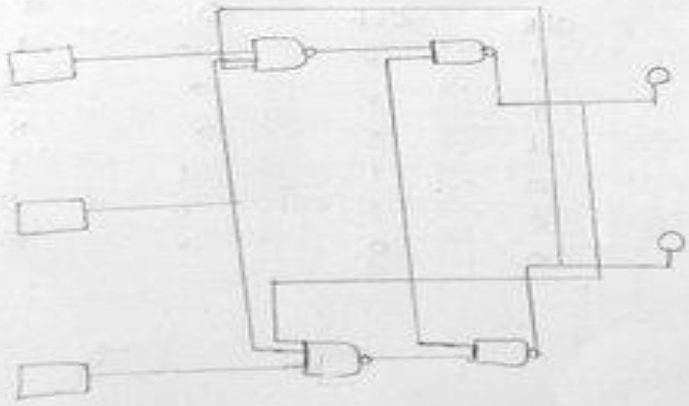


Fig: JK flip flop

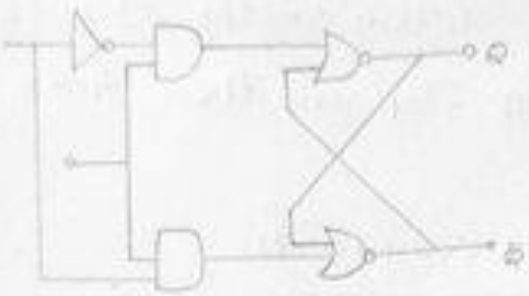
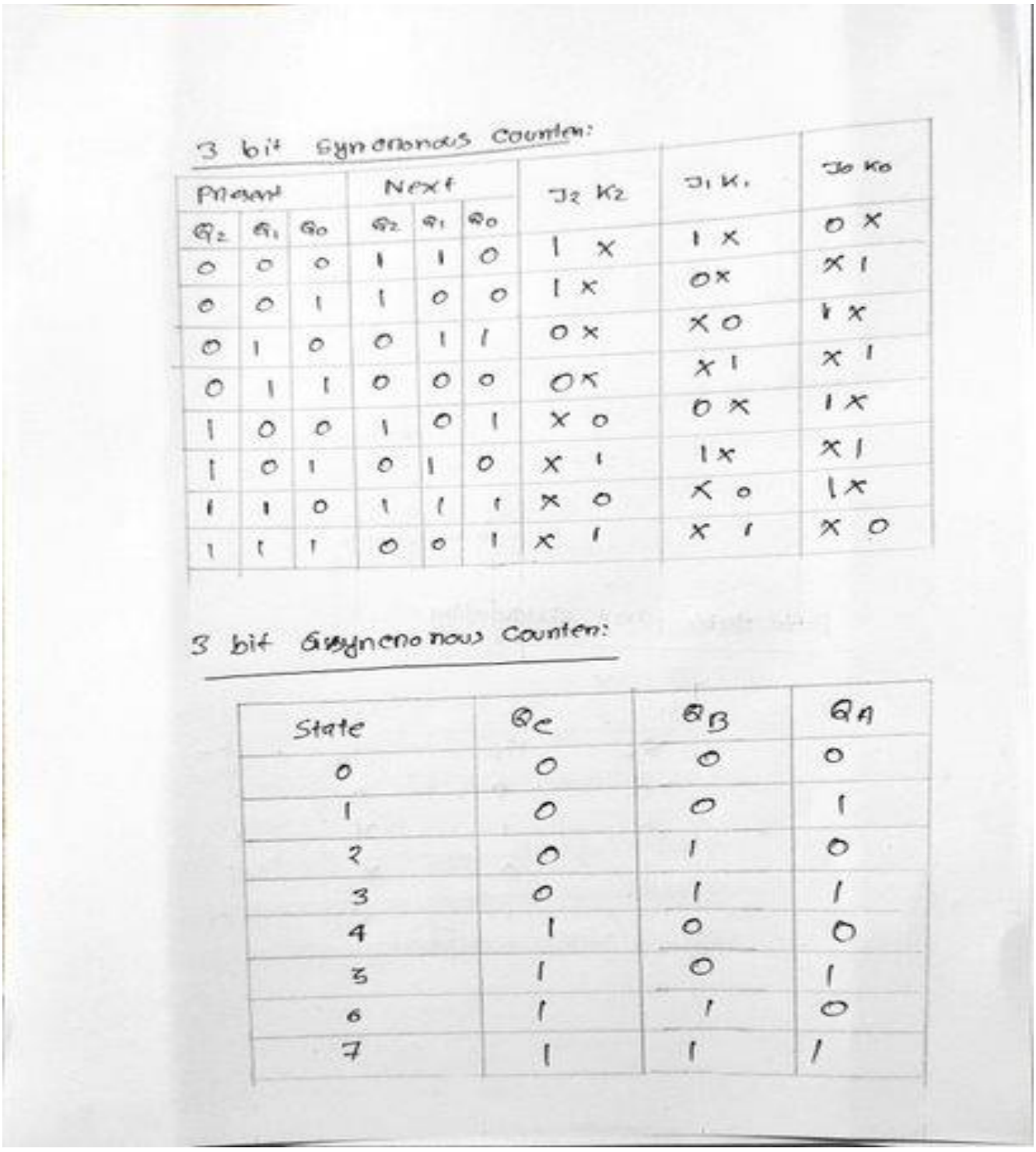


Fig: D flip flop

Data table and calculation:

For J-K flip flop:

PR	CLR	CLK	D	Q	Q̄
1	0	x	x	1	0
0	1	x	x	0	1
1	1	x	x	x	x
0	0	1	1	1	0
0	0	1	0	0	1
0	0	0	x	Q_0	$\bar{Q}_0$



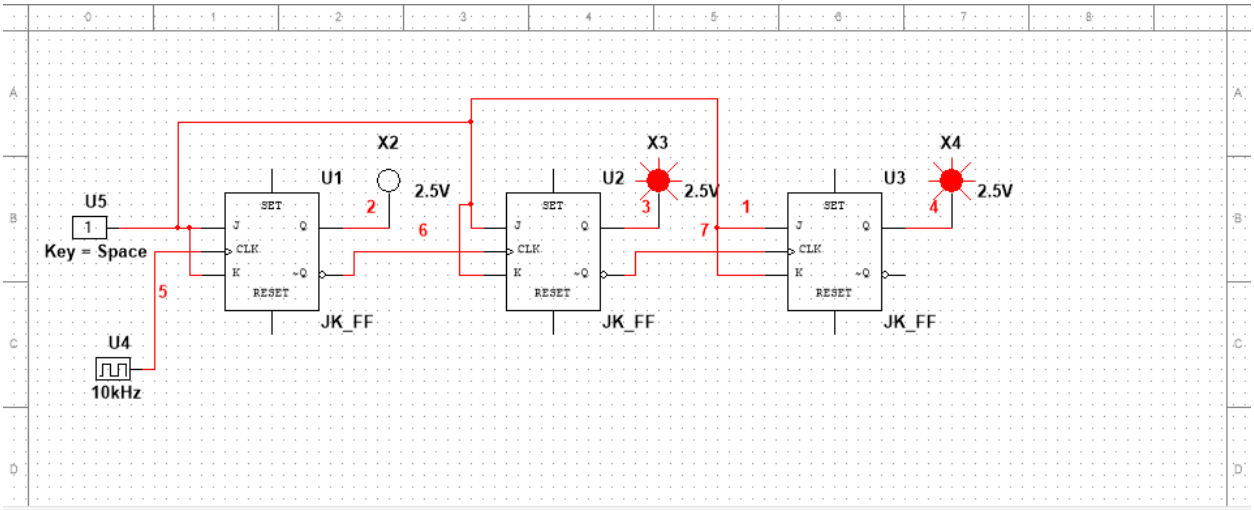
3 bit Synchronous Counter:

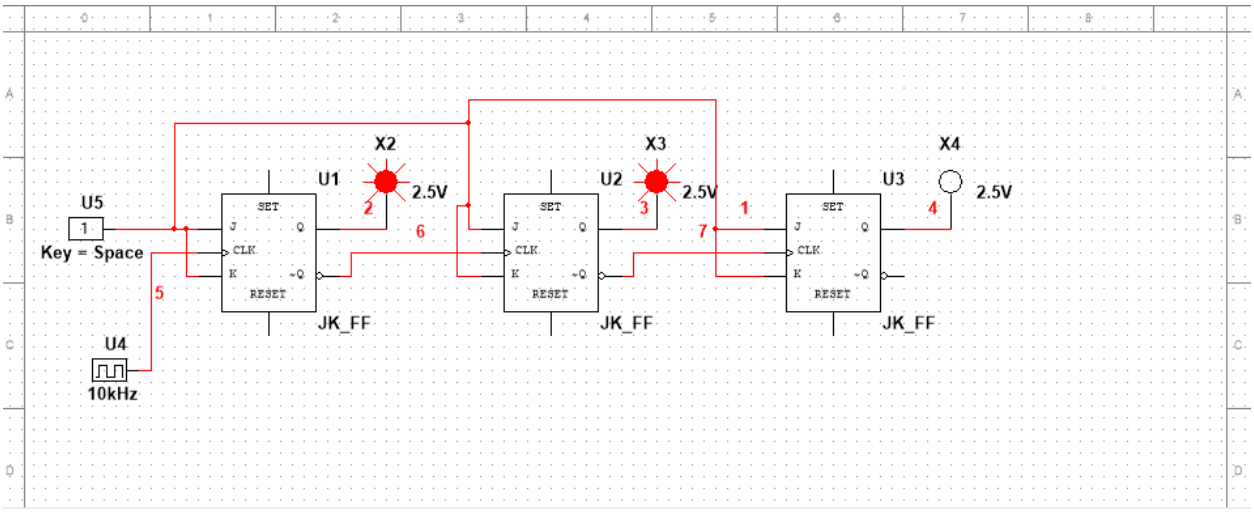
Present			Next			J_2 K_2	J_1 K_1	J_0 K_0
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0			
0	0	0	1	1	0	1 x	1 x	0 x
0	0	1	1	0	0	1 x	0 x	x 1
0	1	0	0	1	1	0 x	x 0	1 x
0	1	1	0	0	0	0 x	x 1	x 1
1	0	0	1	0	1	x 0	0 x	1 x
1	0	1	0	1	0	x 1	1 x	x 1
1	1	0	1	1	1	x 0	x 0	1 x
1	1	1	0	0	1	x 1	x 1	x 0

3 bit Asynchronous Counter:

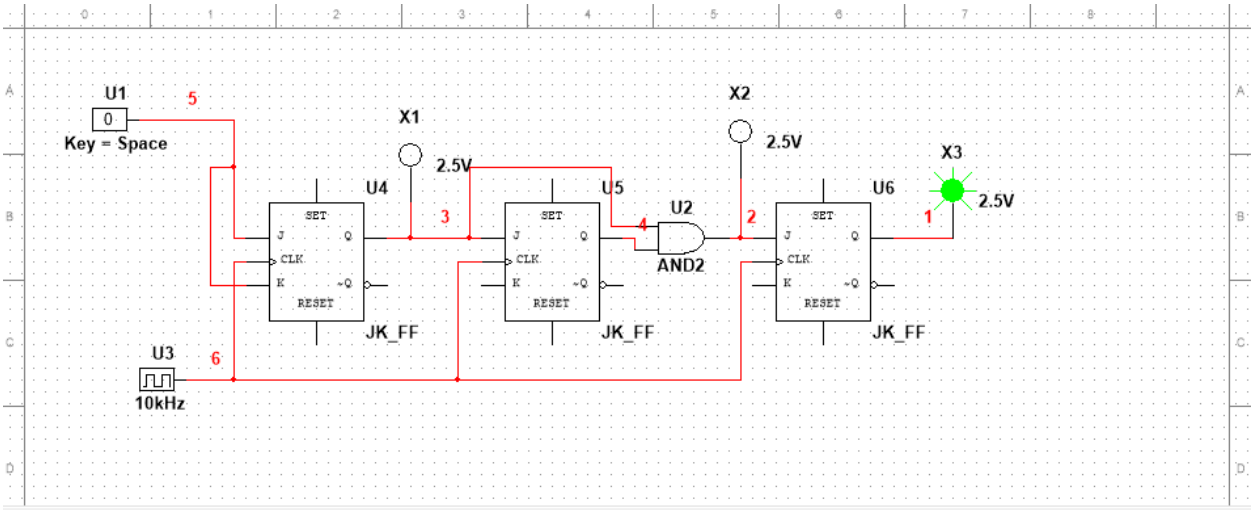
State	Q_C	Q_B	Q_A
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

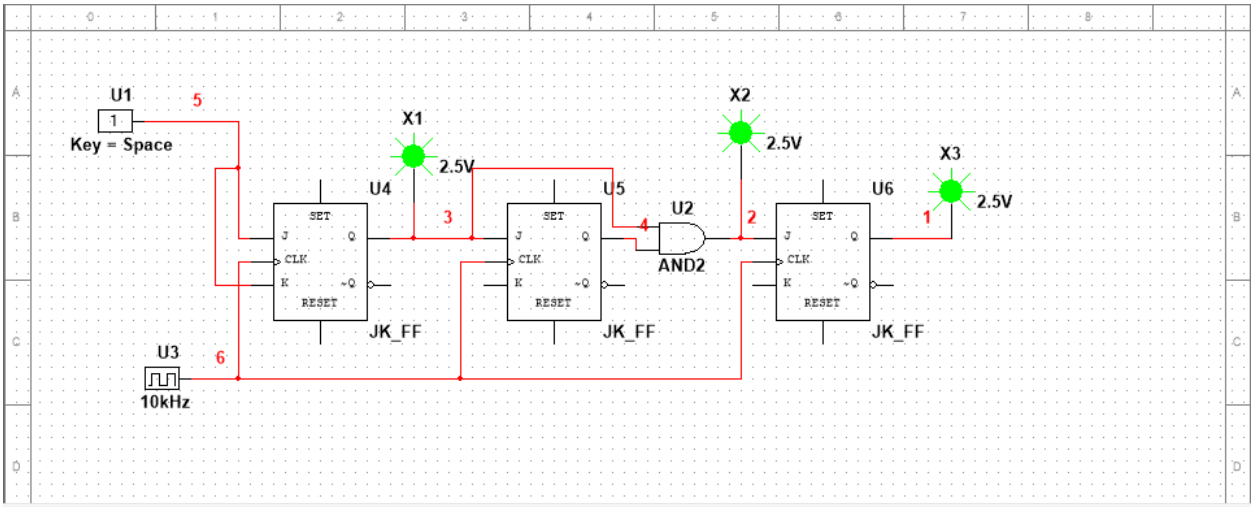
3 bit asynchronous counter:

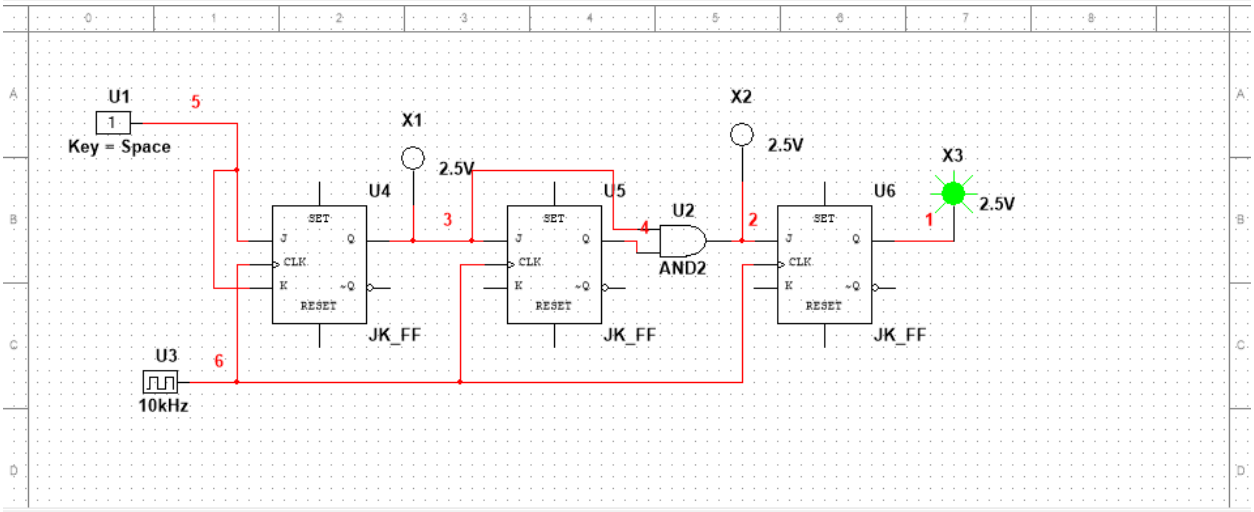




3 bit synchronous counter:


U1
0
Key = Space
5
X1
2.5V
U4
SET
J
Q
CLK
K
~Q
RESET
JK_FF
3
U5
4
U2
AND2
X2
2.5V
2
U6
X3
2.5V
1
U3
6
10kHz


U1
1
Key = Space
5
X1
2.5V
U4
SET
J
Q
CLK
K
~Q
RESET
JK_FF
3
U5
4
U2
AND2
X2
2.5V
2
U6
X3
2.5V
1
U3
6
10kHz


U1
1
Key = Space
5
X1
2.5V
U4
SET
J
Q
CLK
K
~Q
RESET
JK_FF
3
U5
4
U2
AND2
X2
2.5V
2
U6
X3
2.5V
1
U3
6
10kHz

Discussion: Counters are the digital device which are used to count. Counters are mainly 2 types Asynchronous counter and Synchronous counter.

An 3 bit Asynchronous counter contains of 3 T Flip flop and T inputs of all flip flops which are connected to the I. If a flip flop doesn't receive the same clock signal then the counter is called Asynchronous counter. If all the flip flop receive the same clock signal, then that counter is called Synchronous counter. In the asynchronous counter, clock signal is directly applied to the first T flip flop. The first output T flip flop toggles every negative edge of clock signal. Meanwhile Synchronous counter toggles every negative edge of the clock signal.

By connecting IC pins with correct order, we can get an output of the

desire counter output.

Conclusion: In the truth tables of both counters, we can see that the counters are behaving same as theoritical. Though there were some pulse bit issues inside the counter, but although all the outputs are as desired. So, we can say our experiment is a success.

Remarks:

1. Asyncronous counter sometimes give wrong output due to counters maximum use
2. Some IC pins were damaged. So, we have to use pin of different ports

Reference:

Digital Fundamentals Tomas L Floyed.