



CSE 460

VLSI LAB

ASSIGNMENT 01

Submitted by

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CSE-460 Summer-2022

Submission Date: 17th August 2022

Lab Assignment 01

Problem statement

Write a Verilog code to implement the AOI-32 gate and verify it with the timing diagram in Quartus.

Code

```
//verilog code for AND-OR-INVERT(AOI) gate
```

```
module AOI32 (input a,b,c,d,e, output y);
```

```
    assign y = ~((a & b & c) | (d & e)) ;
```

```
endmodule
```

```
//end of verilog code
```

Compilation Report

Quartus II - E:/Fall 22/CSE 460/Labs/AOI32 - AOI32.v [Compilation Report - Flow Summary]

File Edit View Project Assignments Processing Tools Window Help

Project Navigator

Entity	Logic Cells	LC Registers	Memory Bits
FLEX10KE AUTO	2 (2)	0	0

Tasks

Flow: Compilation

Task	Time
Compile Design	00:00:10
Analysis & Synthesis	00:00:02
Fitter (Place & Route)	00:00:03
Assembler (Generate programming files)	00:00:03
Classic Timing Analysis	00:00:01
EDA Netlist Writer	00:00:01
Program Device (Open Programmer)	

Compilation Report - Flow Summary

Flow Status: Successful - Mon Oct 17 18:26:38 2022

Quartus II Version: 8.1 Build 163 10/28/2008 SJ Web Edition

Revision Name: AOI32

Top-level Entity Name: FLEX10KE

Family: FLEX10KE

Met timing requirements: Yes

Total logic elements: 2 / 1,728 (< 1 %)

Total pins: 6 / 102 (6 %)

Total memory bits: 0 / 24,576 (0 %)

Total PLLs: 0

Device: EPF10K30ETC144-1

Timing Models: Final

Message Window

Type: Message

Info: Delay annotation completed successfully

Info: Longest tpd from source pin "c" to destination pin "y" is 7.800 ns

Info: Quartus II Classic Timing Analyzer was successful. 0 errors, 0 warnings

Info: Running Quartus II EDA Netlist Writer

Info: Command: quartus_eda --read_settings_files=off --write_settings_files=off AOI32 -c AOI32

Warning: Can't generate output files. Specify command-line options to generate output files, or update EDA tool settings using GUI or Tcl scripts.

Info: Quartus II EDA Netlist Writer was successful. 0 errors, 1 warning

Info: Quartus II Full Compilation was successful. 0 errors, 4 warnings

System [2] Processing [43] Extra Info [39] Info [39] Warning [4] Critical Warning Error Suppressed Flag

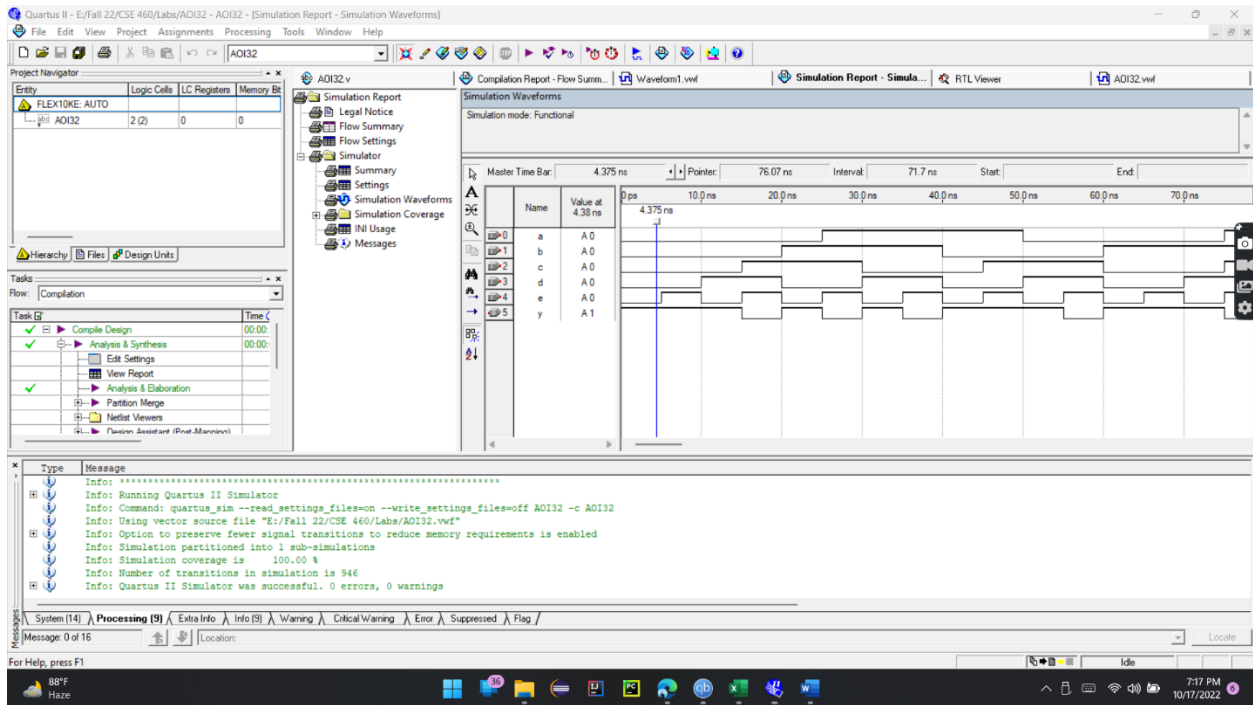
Message: 0 of 87

For Help, press F1

89°F
Haze

6:26 PM
10/17/2022

Simulation Report



Truth Table

A	B	C	D	E	$Y = \sim ((A.B.C) (D.E))$
0	0	0	0	0	1
0	0	0	0	1	1
0	0	0	1	0	1
0	0	0	1	1	0
0	0	1	0	0	1
0	0	1	0	1	1
0	0	1	1	0	1
0	0	1	1	1	0
0	1	0	0	0	1
0	1	0	0	1	1
0	1	0	1	0	1
0	1	0	1	1	0
0	1	1	0	0	1
0	1	1	0	1	1
0	1	1	1	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	0	0	1	1

1	0	0	1	0	1
1	0	0	1	1	0
1	0	1	0	0	1
1	0	1	0	1	1
1	0	1	1	0	1
1	0	1	1	1	0
1	1	0	0	0	1
1	1	0	0	1	1
1	1	0	1	0	1
1	1	1	0	0	0
1	1	1	0	1	0
1	1	1	1	0	0
1	1	1	0	1	0
1	1	1	1	0	0
1	1	1	1	1	0

RTL View

The screenshot displays the Quartus II RTL Viewer for the design AOI32.v. The interface includes a Project Navigator on the left showing the design hierarchy (Entity, Logic Cells, LC Registers, Memory Blocks) and a Tasks pane. The main area shows the RTL logic diagram with three 3-input AND gates (labeled y-1, y-2, y-3) and a 3-input OR gate (labeled y). The AND gates have inputs a, b, c and d, e, f respectively. The OR gate has inputs y-1, y-2, and y-3. The output is y. The bottom pane shows the Messages window with simulation results, including information about simulation coverage (100.00%) and the number of transitions (2490).

Explanation of how the timing diagram manifests the Truth Table

In this task, I've simulated an AOI32 [And Or Invert] gate, which is based on five inputs and provides one output. For input, A binary value changes faster, so I've given the least time to change the value in A. The binary value of input B changes slowly compared to input A. Accordingly, the value of input C changes slower than input B. Input D changes slower than input C. Input E changes slower than input D. In that case; I've assigned the values of these inputs depending on their changing rate, which is why I've taken 50ns time for input A, 40ns for input B, 30ns for input C, 20ns for input D, 10ns for input E. I've taken 10ns difference of time for each input.

Now, if we look at the timing simulation and analyze it, we will be able to see the truth table representation in the timing diagram. In the timing diagram, 0ps to 10ns, if we notice the output value $Y = 1$ for input $A=0, B=0, C=0, D=0$ and $E=0$, also output $Y=1$ when input $A=0, B=0, C=0, D=0$ and $E=1$. Similarly, output $Y=0$ when input $A=0, B=0, C=1, D=1, E=1$.

So, according to the simulations and what has been discussed, it represents that the timing diagram manifests the truth table.