

CSE 460

VLSI LAB

ASSIGNMENT 02

**Submitted by**

Md. Nasimuzzaman

Id: 19101051

CSE-460 Fall-2022

Submission Date: 1st November 2022

**Lab Assignment 01**

**Problem statement**

Design an 8 to 1 MUX using **case** statement in Verilog HDL

**Code**

module MUX(A,B,c);

input [7:0]A;

input [2:0]B;

output reg c;

always @(A,B)

case ({B})

0: c = A[0];

1: c = A[1];

2: c = A[2];

3: c = A[3];

4: c = A[4];

5: c = A[5];

6: c = A[6];

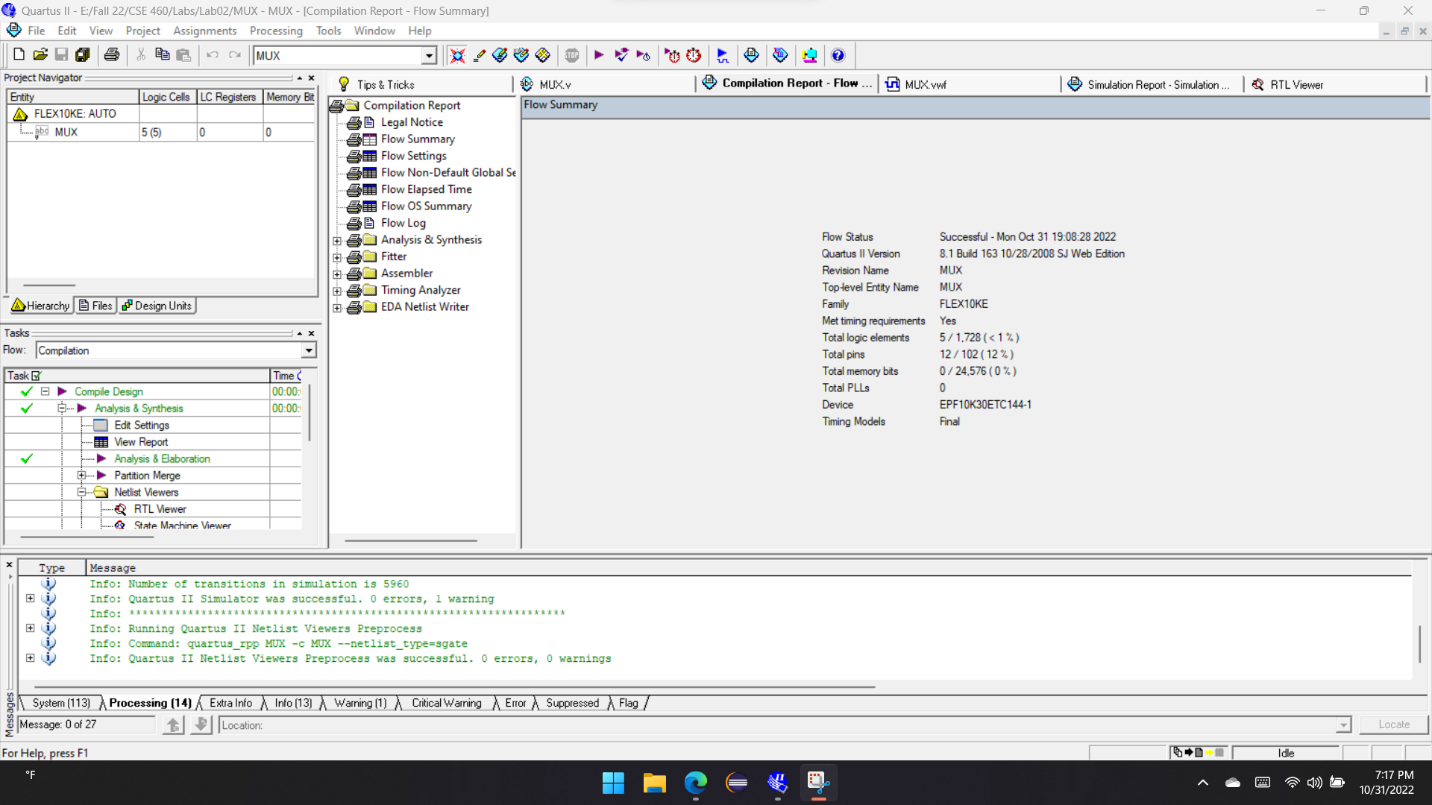
7: c = A[7];

default: c = 1'bx;

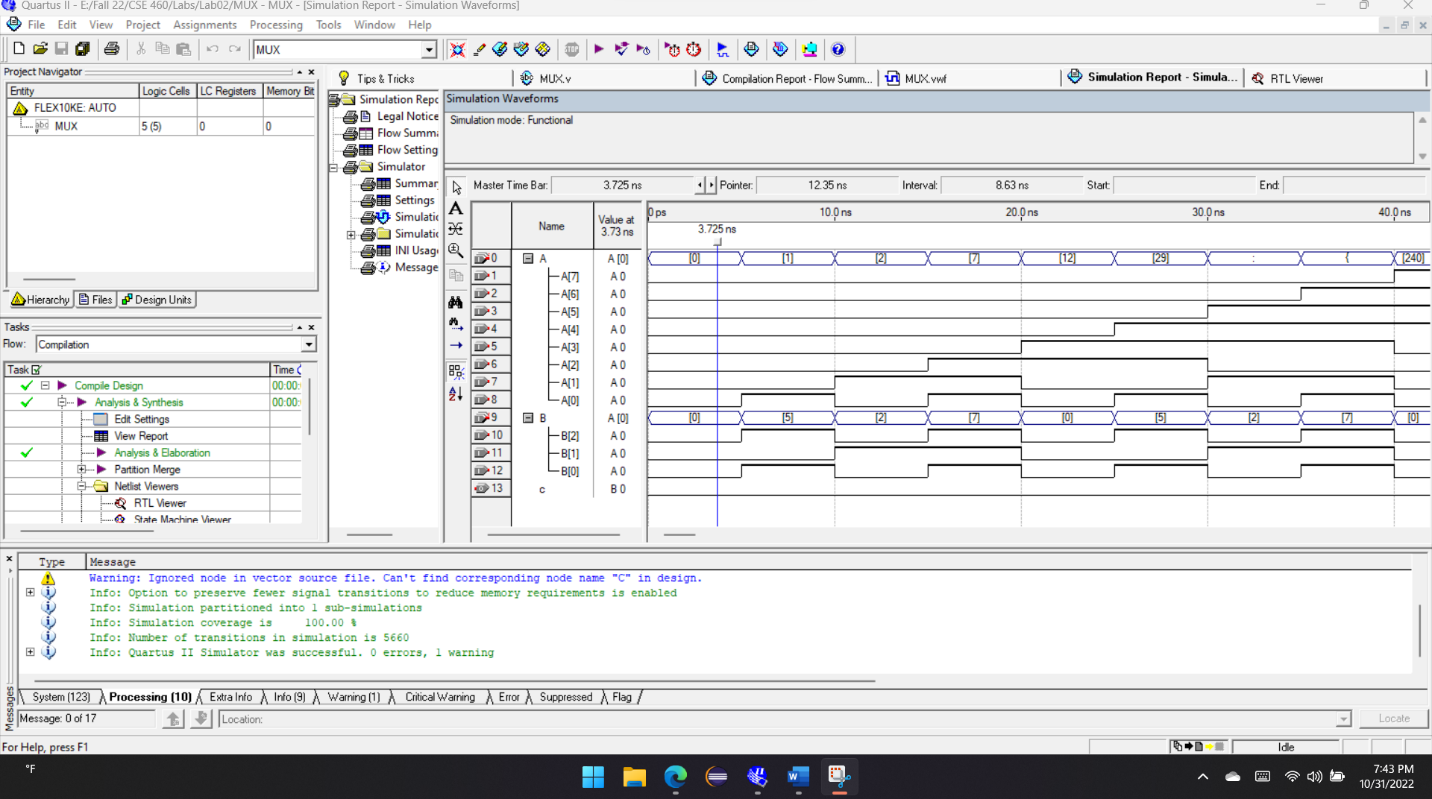
endcase

endmodule

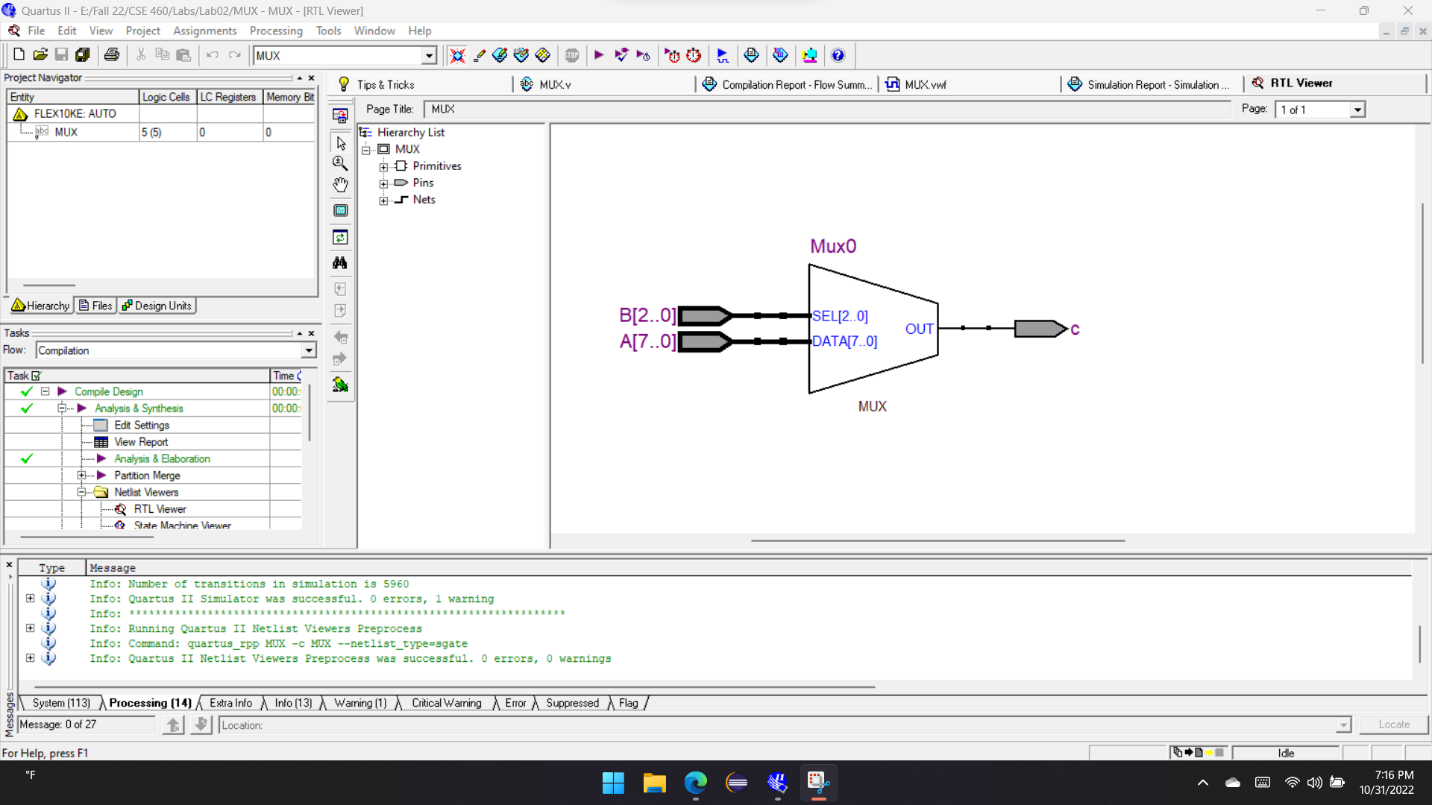
**Compilation Report**



**Simulation Report**



**RTL View**

****

**Explanation**

In this task, I’ve simulated an 8:1 Multiplexer, which is based on eight inputs and provides one output. An 8:1 MUX is a digital circuit that allows eight data inputs to be selected and routed to a single data output. The selection of which data input to route to the output is controlled by three select lines. The three select lines are used to control which data input is routed to the output. The select lines are typically active-low, meaning that when the select line is low, the corresponding data input is selected. For example, if select lines S0 and S2 are low and select line S1 is high, data input D0 will be routed to the output.

Now, look at the timing simulation and I’ve taken B as selection pin along with input pin A. The output is ‘c’ here. So, from the simulation when the selector pin B0 & B2 are low and B1 is high, the output is generating the input value of A0.