Variable Gain Amplifier (VGA)

An amplifier with continuously tuneable gain via the tail current MOSFET.

Features/Specifications

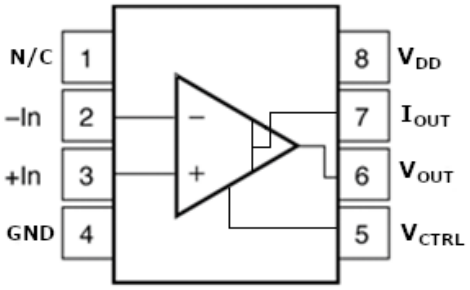
- Gain Range: 32dB - V_{OUT}, 10kΩ resistive load
- Bandwidth: from 1MHz up to 100MHz (load dependant)
- Power Consumption: 1.773mW with 1nF Load, V_{CTRL} = 0.7V; 502µW with 1kΩ Load, V_{CTRL} = 0.6V;
- 1.8v single supply

Recommended V_{CTRL} range: 0.6v to 2v

Applications

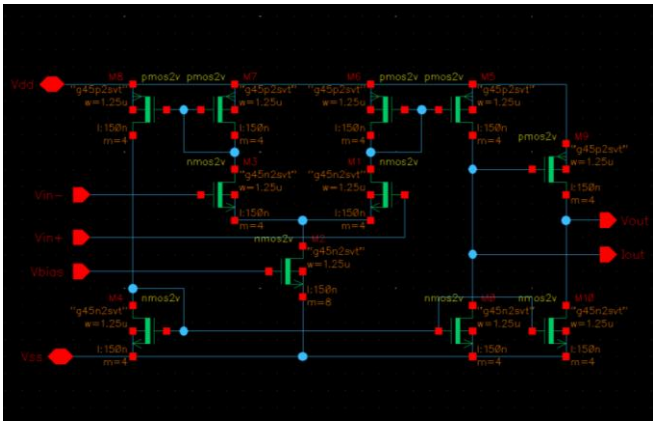
- Signal conditioning
- Instrumentation amplifier
- Medical and industrial ultrasound systems

Pinout



Functional Description

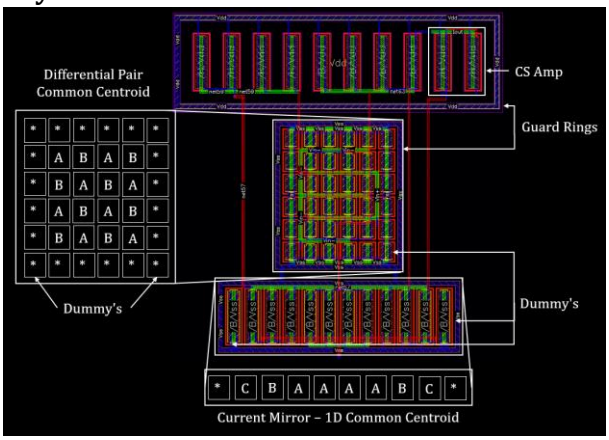
Schematic



Description

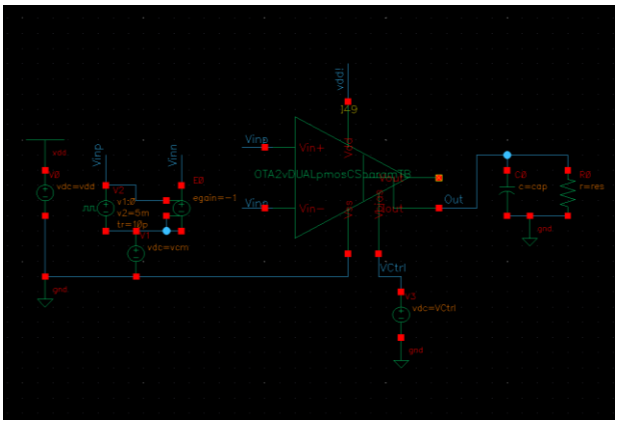
Based on a standard Operational Transconductance Amplifier (OTA) architecture with an added Common Source buffer to convert the current output to voltage. The current mode output (I_{OUT}) only supports purely capacitive loads (as resistive loads below 10k cripple the gain). The buffer allows for enhanced gain and the support of resistive loads instead of just purely capacitive loads.

Layout



The differential pair was organised in a tiled 2-dimensional common centroid arrangement. The NMOS current mirrors were arranged in a 1-dimensional common centroid fashion as the 3 MOSFETs do not have an optimum interdigitated pattern. Dummies were placed on the ends of the current mirror arrangement.

Testbench

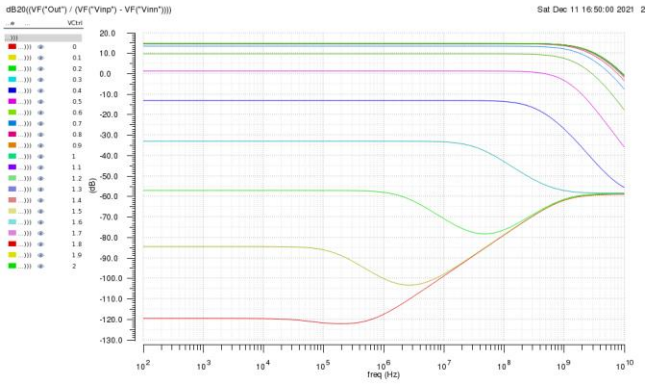


Typical Characteristics/Performance Metrics

OTA Output - I_{OUT}

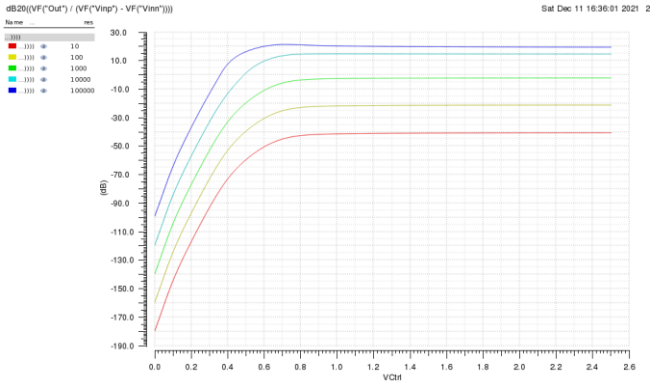
Resistive Loads

Freq. Response (vs V_{CTRL}) with 100kΩ Load



For the Current mode output of the OTA (I_{OUT}) resistive loads that aren't sufficiently high do not allow for positive gain.

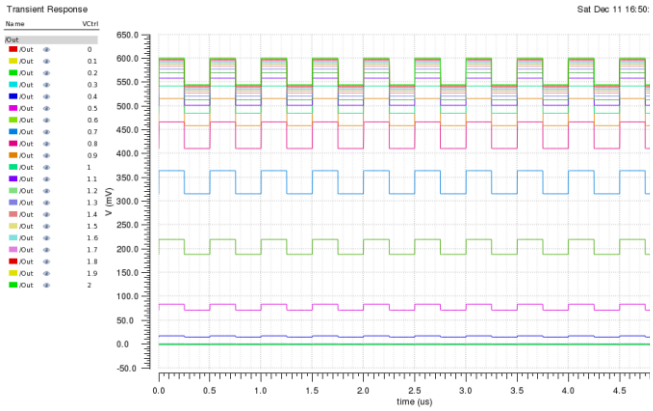
Gain vs V_{CTRL} @ 100Hz - Resistive Loads



With low resistances (5k-10k) gain range is limited to a few decibels requiring higher minimum control voltages to achieve positive gain. Resistive loads less than 5k do not provide positive gain.

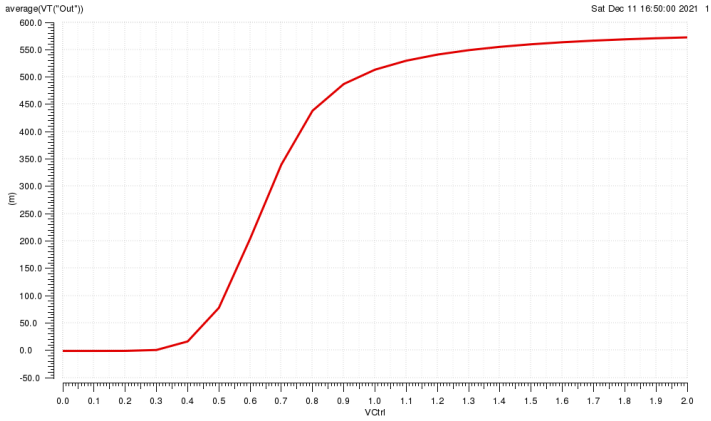
Resistance	Max G	Min G	Range
100k	21.4	19.34	2.06
10k	14.89	10.3	4.59
1k	-1.92	-10.3	8.38

Transient Response (vs V_{CTRL}) with Load = 100kΩ



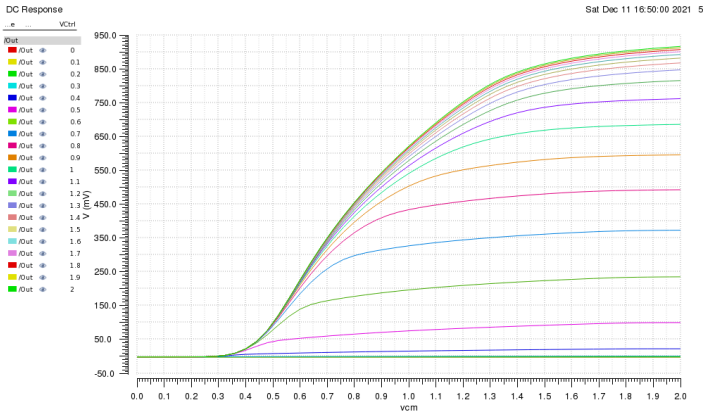
Common mode voltage is seen on output and is dependent on V_{CTRL}.

Avg. Tran. Response vs V_{CTRL} with V_{CM} = 0.9v



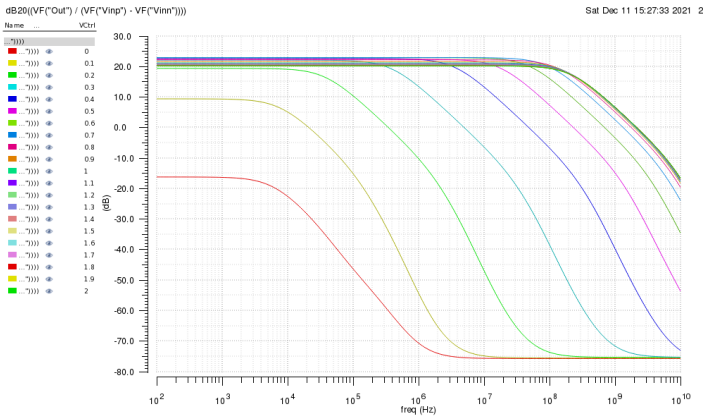
Offset seen at output varies with control voltage and is seen to be attenuated compared to the 0.9v common to the inputs.

I_{OUT} vs V_{CM} (vs V_{CTRL})



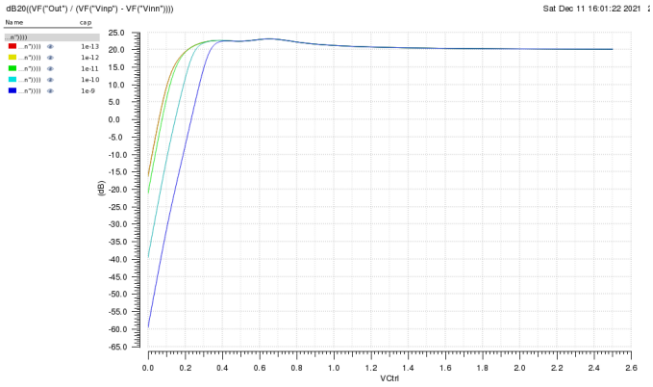
Capacitive Loads

Freq. Response (vs V_{CTRL}) with Load = 100fF



Minimum achievable bandwidth of 20MHz with control voltage floor of 0.6v and capacitive loads below 100pF.

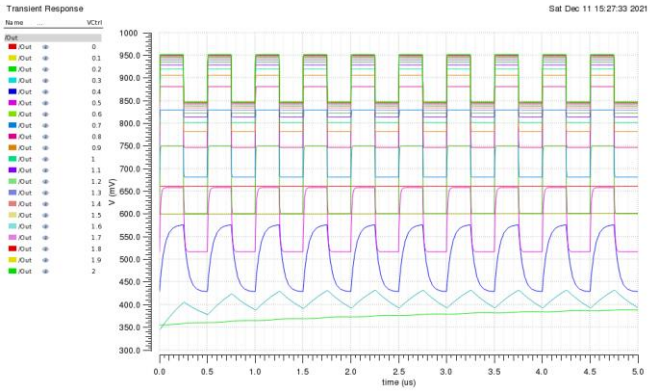
Gain vs V_{CTRL} @ 100Hz – Capacitive Loads



Consistent Gain range of approximately 3.5dB (approx. min 20dB, max 23.5dB) for various capacitive loads.

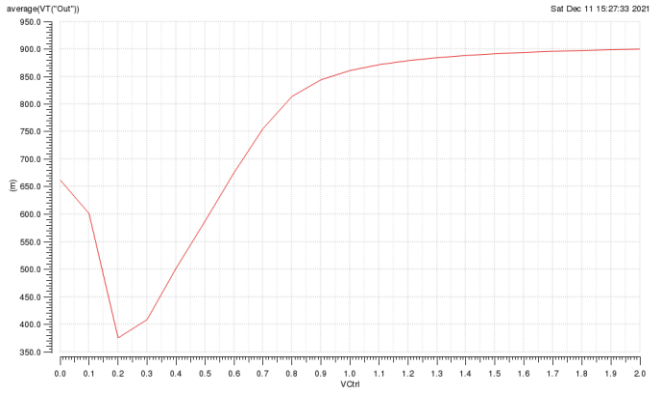
Max G	Min G	Gain Range
23.1	19.97	3.13dB

Transient Response (vs V_{CTRL}) with Load = 100fF

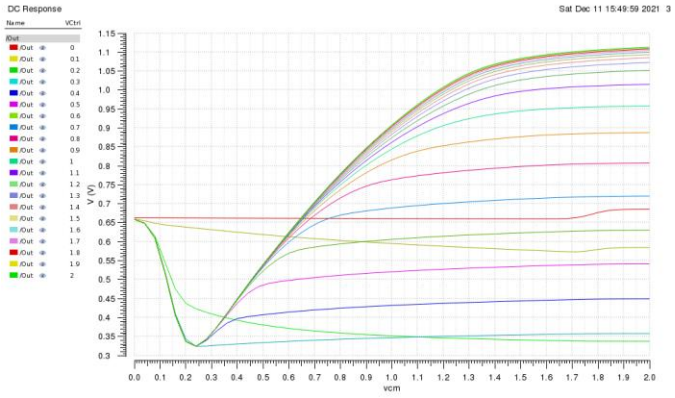


To ensure good slew rate for capacitive loads the lower limit on control voltage should be 0.5v. also capacitive loads greater than 10pF cause the slew rate to drop significantly

Avg. of Tran. Response vs V_{CTRL} with V_{CM} = 0.9v



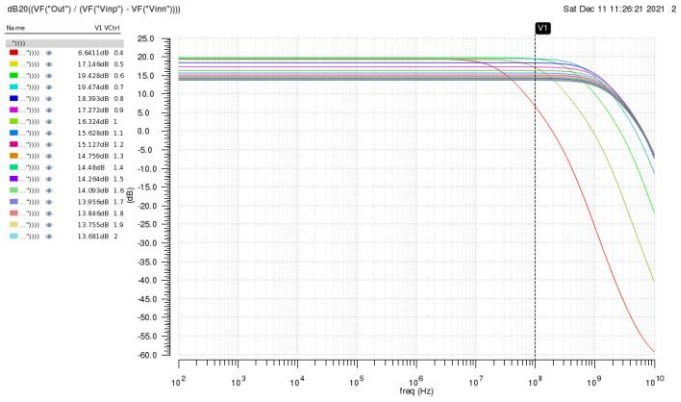
I_{OUT} vs V_{CM} (vs V_{CTRL})



Buffer Output - V_{OUT}

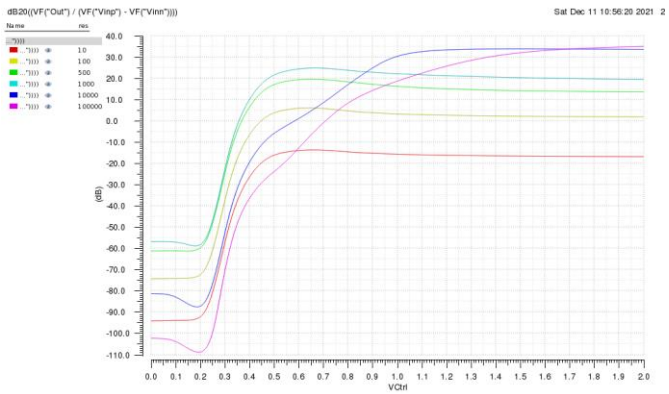
Resistive Loads

Freq. Response (vs V_{CTRL}) with Load = 500Ω



100MHz bandwidth at max gain of 19.47dB at 0.7v V_{CTRL}. V_{CTRL} of 2v gain is reduced with bandwidth increased to 1GHz. Positive gain is achievable at higher frequencies with increased control voltages (increasing the lower limit on control voltages).

Gain vs V_{CTRL} @ 100Hz - Resistive Loads

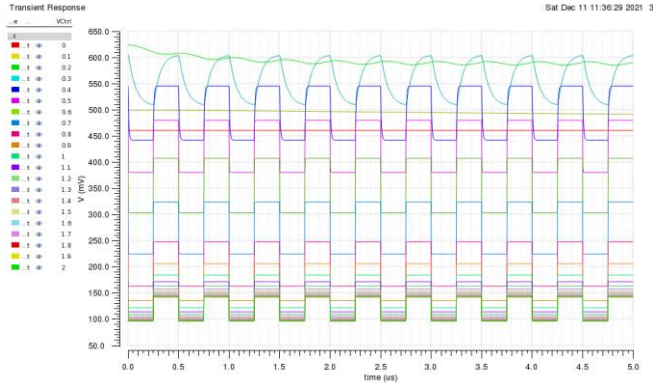


Gain vs resistive loads on the buffer output varies significantly

Resistance	Min Gain	Max Gain	Range
100	4.3	6.3	2.0
500	13.7	19.8	6.1
1k	19.6	24.99	5.4
10k	1.744	33.6	31.9
100k	-12.3	35.3	47

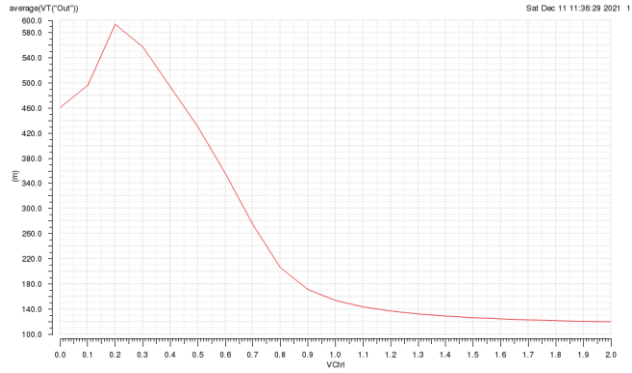
Resistive loads less than 100Ω suffer dramatic losses in gains.

Transient Response (vs V_{CTRL}) with Load = 500Ω

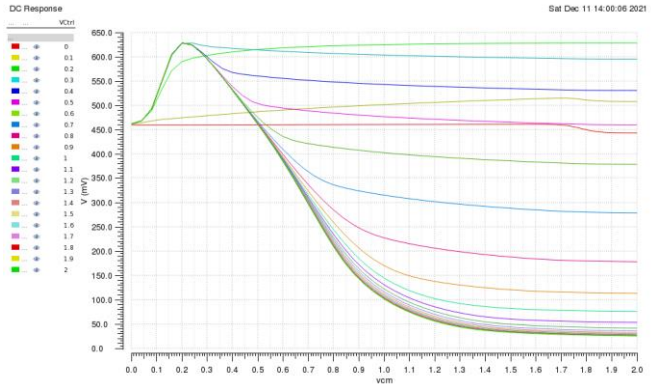


For a good slew rate with resistive loads ensure control voltage is above 0.5v to allow for enough tail current through the control MOSFET. Thus, recommended control voltage is 0.5v+.

Avg. Tran. Response vs V_{CTRL} with V_{CM} = 0.9v

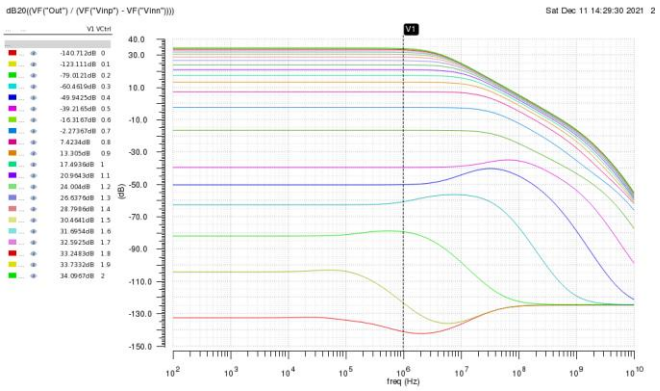


V_{OUT} vs V_{CM} (vs V_{CTRL}) with Load = 500Ω



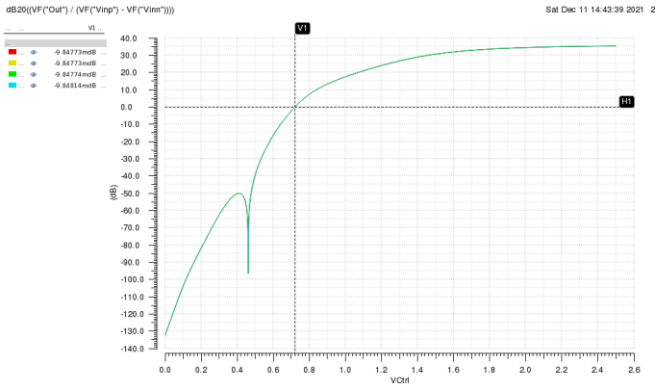
Capacitive Loads

Freq. Response (vs V_{CTRL}) with Load = 10pF



Bandwidth of 10MHz achievable with control voltage above 0.8v. Increasing control voltage sees gain increasing to approx. 35dB and bandwidth reducing to 1MHz.

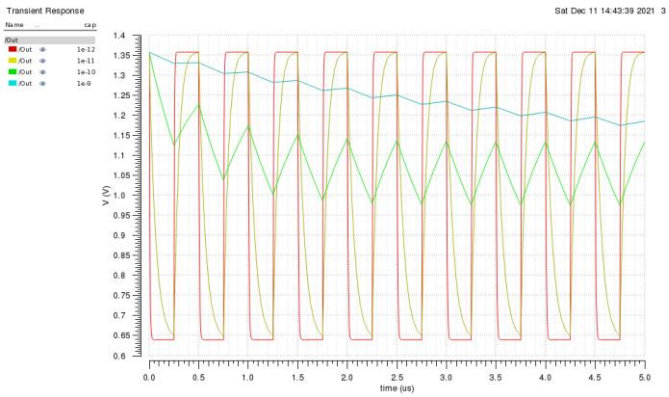
Gain vs V_{CTRL} @ 100Hz - Capacitive Loads



Gain varies with V_{CTRL}. Usable gain range is from 0- approx. 36dB and control voltages from 0.72v and above.

Max G	Min G	Gain Range
36.7	-16.6 @0.6v	53.3dB

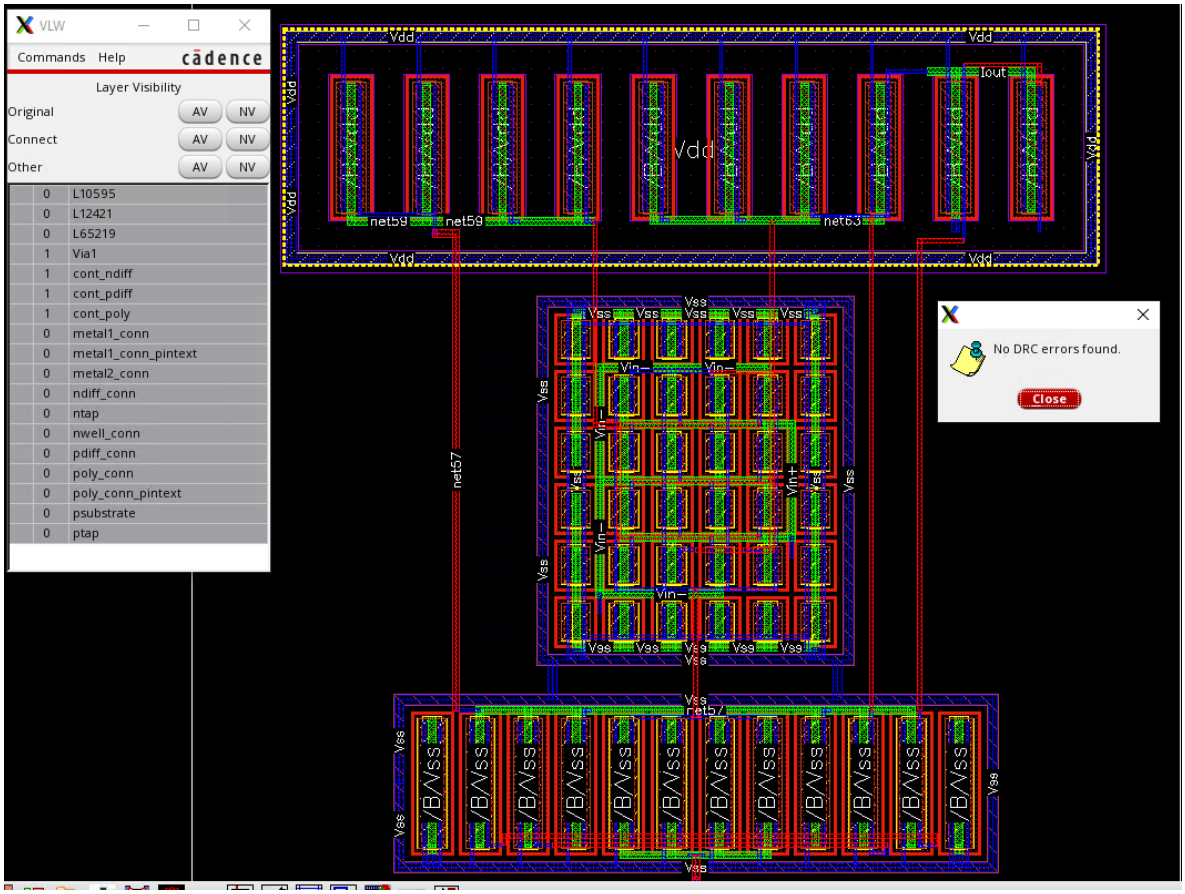
Transient Response – Cap. Loads, V_{CTRL} = 1.6v



Capacitances greater than 10p suffer from reduced slew rate. Recommended capacitive loads for the buffered output of capacitances less than 10pF.

Appendix

DRC



LVS