Team Design Tutorial
PlanAhead Design Tool

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This tutorial document was last validated using the following software version: ISE Design Suite 14.5

If using a later software version, there may be minor differences between the images and results shown in this document with what you will see in the Design Suite.

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Revision History

Date	Version	Revision
04/25/2013	14.5	Validated with Release.

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Team Design Tutorial

Tutorial Objectives

This tutorial provides an overview of the Team Design flow. In this tutorial, you will complete a design acting as a team leader and various team members. The objective of this tutorial is to familiarize you with partitions and the Team Design flow using the PlanAhead™ software.

The Team Design flow is a hierarchical design methodology that uses partitions to allow a large, complex design to be broken up into smaller logical blocks.

- These blocks can be implemented independently and simultaneously.

- This allows each block to be individually designed, implemented, and verified in context with the rest of the design.

- When all blocks are complete, the entire design is brought together in an assembly run in which results can be imported and preserved.

A Team Design flow team consists of:

- One team leader

- One or more team members

Project Setup

Initially, as team leader, you will:

- Define partitions on each team member block. Each team member block is a black box.

- Define Pblocks.

- Review existing physical and timing constraints.

- Synthesize an initial version of the design using Xilinx® Synthesis Technology (XST) incremental synthesis.

- Promote synthesis results for the Top partition.

- Run a Design Rules Check (DRC).

- Implement the initial design.

- Create PlanAhead projects for each team member.

Team Member Work

When a PlanAhead project has been created for each team member, you will complete the work of each team member as follows:

- Update the project to include actual design files for the team member block.

- Synthesize the updated team member design while importing the Top partition

  Other team member blocks are black boxes.

- Implement the team member design.

   Other team member blocks are black boxes.

- Promote successful synthesis and implementation results to a location accessible by the team leader.

Design Assembly

The team leader then assembles the design by importing the results from each team member project. You will:

- Assemble the design by importing the results from each team member project.

- Update the team leader project to include NGC files for each team member block.

- Set up implementation to import each team member block while implementing the Top partition.

- Verify design assembles while maintaining placement and routing results from each team member.

Tutorial Design Description

This tutorial uses an incremental synthesis flow to create separate netlist for each partitioned instance. These individual netlists are required for a team design flow.

The design used throughout this tutorial contains:

- A RISC processor

- FFTs

- Gigabit transceivers

- Two USB port modules (to be partitioned)

- An xc7k70tfbg676 device

Software Requirements

The PlanAhead tool is installed with ISE Design Suite software. Before starting the tutorial, be sure that the PlanAhead tool is operational, and that the tutorial design data is installed.

For installation instructions and information, see the *ISE Design Suite 14: Release Notes, Installation, and Licensing (UG631)*.

Hardware Requirements

Xilinx recommends a minimum of 2 GB of RAM when using the PlanAhead tool on larger devices. For this tutorial, a smaller design is used, and the number of designs open at one time is limited. Although 1 GB is sufficient, it can impact performance.

Preparing the Tutorial Design Files

This tutorial uses a reference design, **PlanAhead_Tutorial_TD.zip**, which you can download from the Xilinx PlanAhead Tutorials web page at:

http://www.xilinx.com/cgi-bin/docs/rdoc?v=14.5;t=planahead+tutorials

Extract the zip file contents into any write-accessible location. The extraction directory will be referred to in this tutorial as *<Extract_dir>*.

> ✅ **RECOMMENDED:** *The tutorial sample design data is modified while performing this tutorial. A new copy of the original PlanAhead_Tutorial data should be extracted each time you run this tutorial.*

This tutorial includes a project file that has already been implemented. To reduce the data size, some implementation files were removed from the design, leaving only the required results data in the run directories.

Lab 1: Team Design

Step 1: Opening a Project and Setting Partitions

The PlanAhead design tool enables you to create several project types depending on where in the design flow the tool is being used. RTL sources can be used to create a project for development and analysis, synthesis, implementation, and bit file creation.

This tutorial uses an existing PlanAhead tool project, and focuses on the team design aspects in the software. You will not create a new design using the New Project wizard.

Opening the PlanAhead RTL Project

To open the PlanAhead RTL project:

1. Open the PlanAhead tool.

- On Windows, select the Xilinx PlanAhead Desktop icon, or select:

   Start > All Programs > Xilinx Design Tools > ISE Design Suite 14.5 > PlanAhead > PlanAhead.

- On Linux, go to the `<Extract_Dir>` directory and type: **planAhead**.

2. From the Getting Started page, click **Open Project**.

3. Browse to `<Extract_Dir>` and open the project file located at:

   `./Projects/project_TL/project_TL.ppr`

   The Project Manager view opens. You can view the design source files in the Hierarchy tab of the Sources view. These files include:

- VHDL and Verilog files

- A User Constraint File (UCF) named `top_full.ucf`. The UCF contains timing constraints and I/O pin locations.

Opening the Elaborated Design

Use the Elaborated Design view to define partitions in an RTL project. When the Elaborated Design view is opened:

- The RTL code is elaborated.

- The design hierarchy is displayed.

This is a pre-synthesized view of the design that is used to define partitions and create constraints. To open the Elaborated Design view:

1. In the Flow Navigator, click **Open Elaborated Design**.

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When you open the elaborated design, the PlanAhead tool opens a Critical Messages dialog box, warning you that the tool is unable to resolve certain cells or nets related to the cpuEngine and the usbEngine modules. These are black box cells which you will soon be defining as partitions.

2. Click **OK** to close the Critical Messages dialog box.
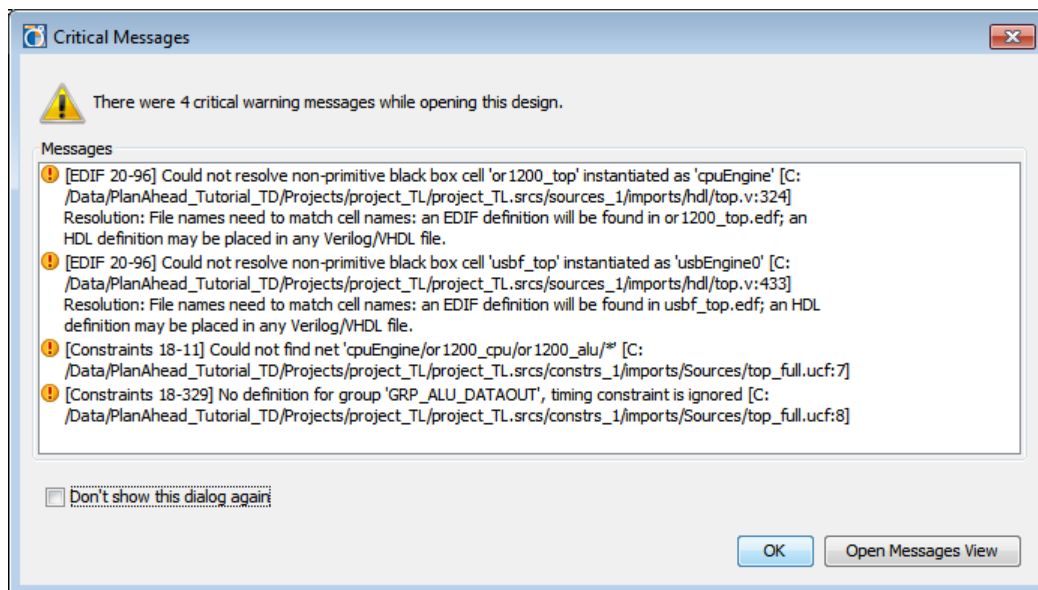
Figure 1: Critical Messages – Black Box Cells

The two **usbEngine** modules and the **cpuEngine** module are good candidates for partitioning for the following reasons.

- They are logically isolated from one another and do not benefit from optimizations with other blocks.

- They are timing critical blocks that can be developed independently and are beneficial to preserve once implemented.

- The interface timing in and out of these blocks are not critical as they are registered.

You can use the PlanAhead design rule checks to help identify modules that are good candidates for partitions.

You can floorplan partitioned instances just like any other instance. Creating Pblock (AREA_GROUP) constraints can help achieve timing closure and improve runtime.

The steps below show you how to set partitions and create appropriate Pblock constraints for the team member instances. Pblocks are required in a Team Design flow for each team member partition.

Setting Partitions on Team Member Instances

To set partitions on team member instances:

1. From the Elaborated Design view, click the **RTL Netlist** tab.

2. Press **Ctrl** and select:

    - **usbEngine0**

    - **usbEngine1**

    - **cpuEngine**
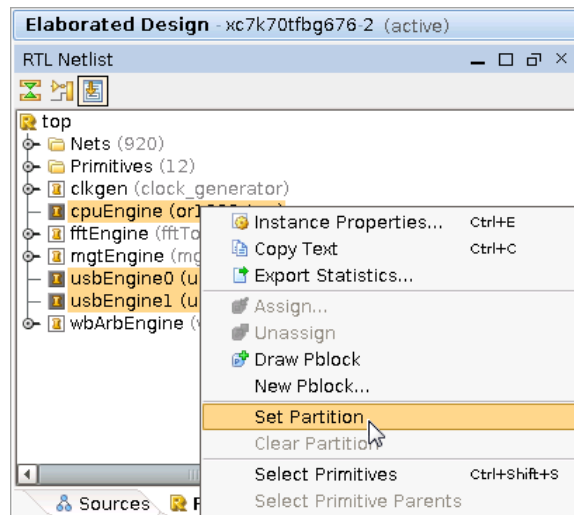
Figure 2: Set Partition

3. **Right-click** to open the popup menu, and select **Set Partition**.

Although three partitions are defined here, there are only two team members in addition to the team leader. Both **usbEngine** instances are managed by a single team member because there is only one set of Hardware Description Language (HDL) code associated with this module.

Step 2: Drawing Pblocks for the Team Member Partitions

In this step, you:

- Define Pblocks.

- Review existing physical and timing constraints.

This step does not affect synthesis results. You could perform it post-synthesis in the Synthesized Design view instead.

For more information on defining Pblocks refer to the *Floorplanning Methodology Guide (UG633)* and the *Design Analysis and Floorplanning Tutorial: PlanAhead Design Tools (UG676)*.

To draw Pblocks for the team member partitions:

1. Change the layout to be Floorplanning by selecting **Layout > Floorplanning.**

2. From the RTL Netlist window, select **usbEngine1**.

3. Right-click and select **Draw Pblock**.
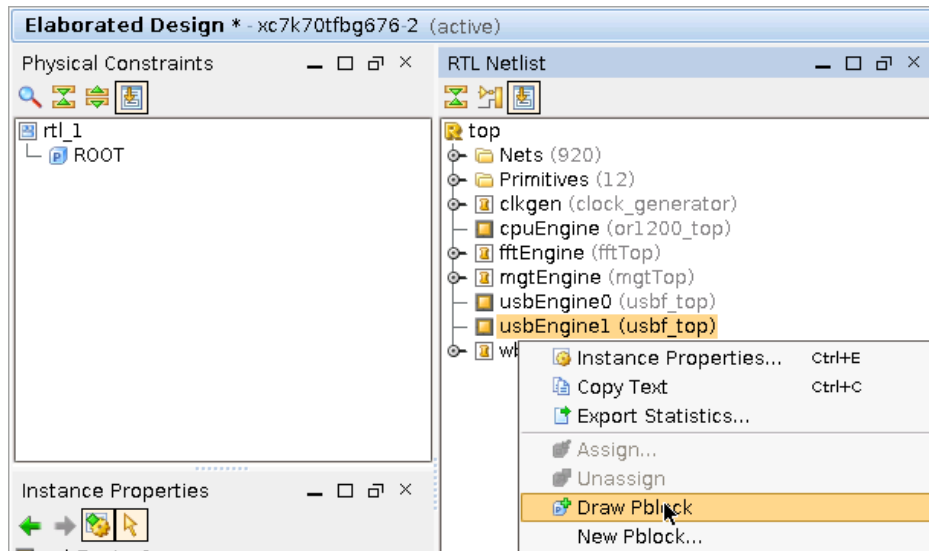
Figure 3: Selecting the Draw Pblock Tool

4. With the Draw Pblock tool active, move the cursor to the Device window.

5. Click the top-left corner of the device where the CLBs start, and drag down and to the right to create a rectangle covering most of the top-left quadrant, as seen in Figure 3 .
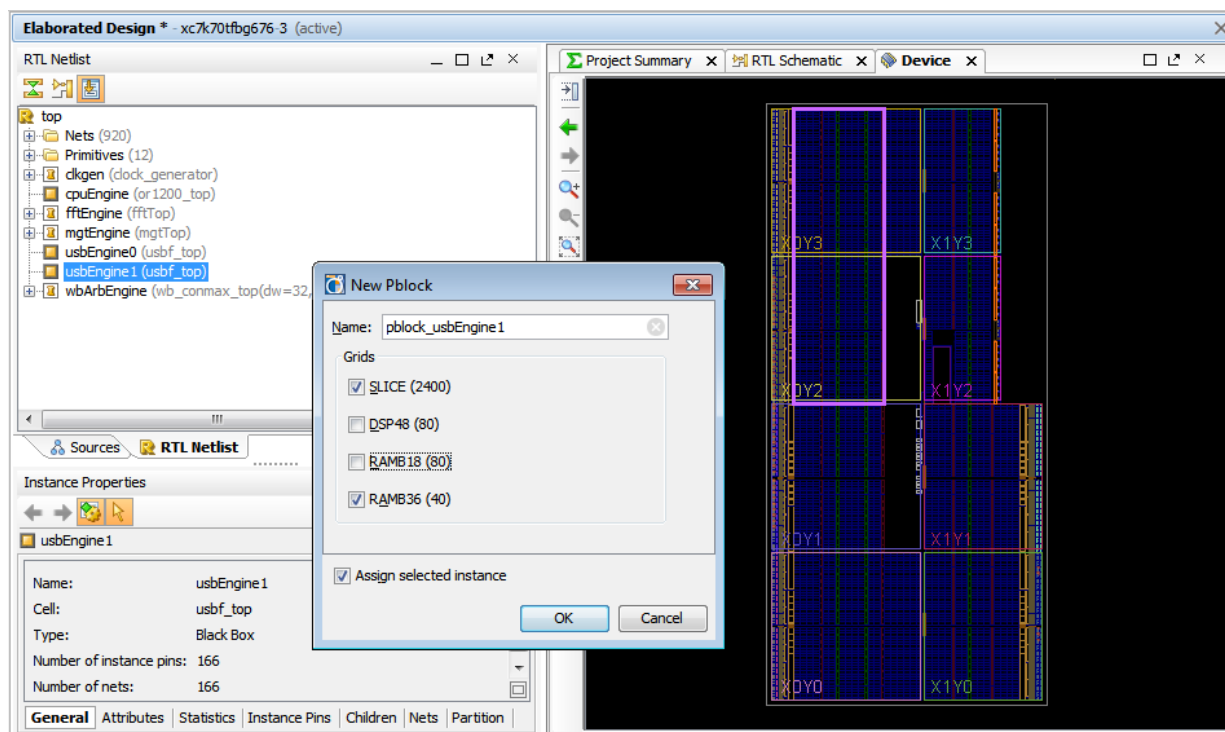
Figure 4: Pblock Rectangle for usbEngine1

7. In the New Pblock dialog box:

   - Verify that the SLICE and RAMB36 grids are selected.

   - Deselect other resources that are not needed.

   - Verify that the number of available RAMB36 is 40.

   If the Pblock rectangle does not include sufficient resources, the design may fail to place.

8. Click **OK**.

9. If the numbers of available resources are different than shown, adjust the size of the Pblock rectangle by selecting it and resizing it until it contains:

   - SLICE (2400)
   - RAMB36 (40)

10. Repeat the steps above for **usbEngine0** in the bottom-left quadrant.

   Only SLICE and RAMB36 (40 of them) are required for this block.

11. Repeat the steps above for **cpuEngine** in the bottom-right quadrant.

   For **cpuEngine**, the Pblock contains all four ranges, as seen in Figure 4, or may be defined as clock regions X1Y0 to X1Y1:
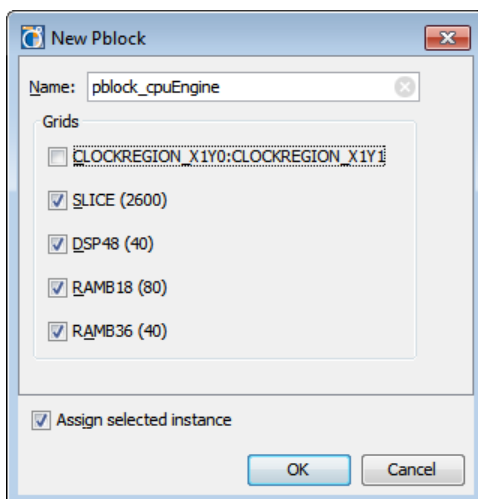
Figure 5: New Pblock Resources
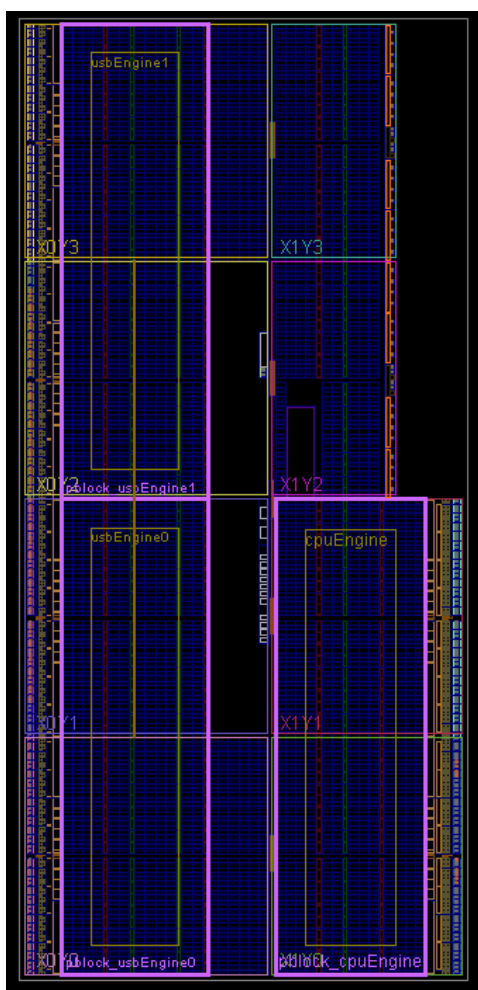
Figure 6: Completed Floorplan for Pblocks usbEngine0, usbEngine1, and cpuEngine

Step 3: Synthesizing and Implementing the Design

In the previous steps, you:

- Defined partitions on the elaborated HDL design.

- Created Pblock constraints.

In this step, you will:

- Run synthesis.

- Run DRC.

- Run implementation.

During synthesis, XST recognizes that the design has partitions, and runs the design through an incremental flow.

In this flow XST generates individual NGC files for each partition. In this design the top partition contains all logic in top.v, as well as all logic from hierarchical blocks that are not their own partition (**fftEngine**, **mgtEngine**, and **wbArbEngine**). All of logic from the top partition will be synthesized to "top.ngc". Since the instances **usbEngine0**, **usbEngine1**, and **cpuEngine** are black boxes and contain no logic in this initial project, no NGC files will be generated for these partitions.

This tutorial uses an RTL project. For a bottom-up or third-party incremental synthesis flow:

- Run synthesis outside the PlanAhead tool.

- Use a netlist project instead of an RTL project in the PlanAhead tool.

Running Synthesis

This design uses default synthesis options. To run synthesis:

1. In the Flow Navigator, click **Run Synthesis**, as seen in Figure 6.

2. Before running synthesis, PlanAhead must save all your constraints for the partition and floorplan changes. If prompted to save your design, click **Save**.

3. After synthesis completes a Synthesis Completed dialog box will appear.

4. Choose to **Open Synthesized Design**, and click **OK** to open the Synthesized Design in the next step.

   This loads the synthesis results and allows for additional DRC checking.

   Note: You will be prompted to close the Elaborated Design. You will need it open later, so to save time, you should select **No**.

5. Click **OK** to close the **Undefined Modules** dialog box, and again to close the **Critical Messages** dialog box. It is expected to have black boxes in the design at this point.
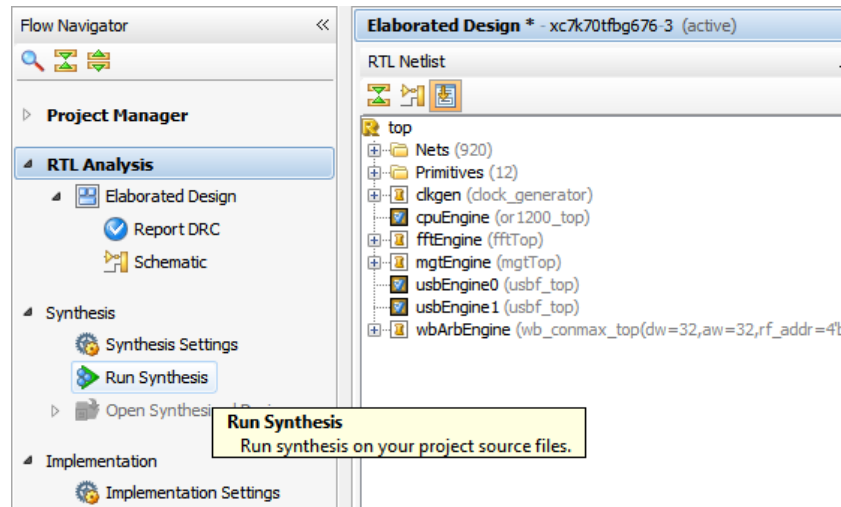
Figure 7: Run Synthesis

Running DRC on Partitions

You can run Design Rule Checks (DRC) on the Elaborated Design, although the checks at this stage are limited. Xilinx recommends that you run a DRC on the post-synthesis design before implementation.

With the synthesized design open, to check DRC, run partition-specific DRCs.

1. In the Flow Navigator under Synthesized Design, click **Report DRC**.

2. From the Report DRC dialog box, deselect all rules except **Partition** and **Team Design**.

3. Click **OK**.
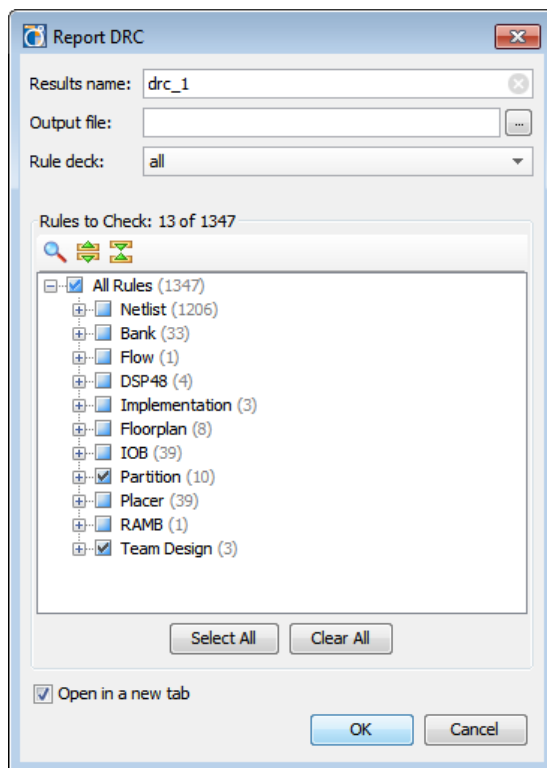
Figure 8: Run Partition Design Rule Checks

DRC Messages

The PlanAhead tool can report the following message types for the DRC rules:

- Advisory
- Warning
- Error
- Fatal

In this case, the DRC returns several warning messages. You can safely ignore them. The DRC messages are caused by the black boxes in the design.

Note: In an actual design, investigate all DRC messages, and correct any serious issues.

Running Implementation

Before transmitting the design to each team member, the team leader should run implementation to check that all timing and floorplan constraints are valid. Since the **usbEngine** modules and **cpuEngine** modules are black boxes, the implementation results will not be of any other value at this point.

1. In the Flow Navigator, click **Run Implementation**.

2. As implementation is running, click the **Report** tab to see a list of all implementation reports.

3. As each process finishes, the related reports are available for review.

4. After NGDBuild finishes, double-click the **NGDBuild Report** to open the report.

5. Scroll to the bottom of the report file to review the partition information, as seen in Figure 7.
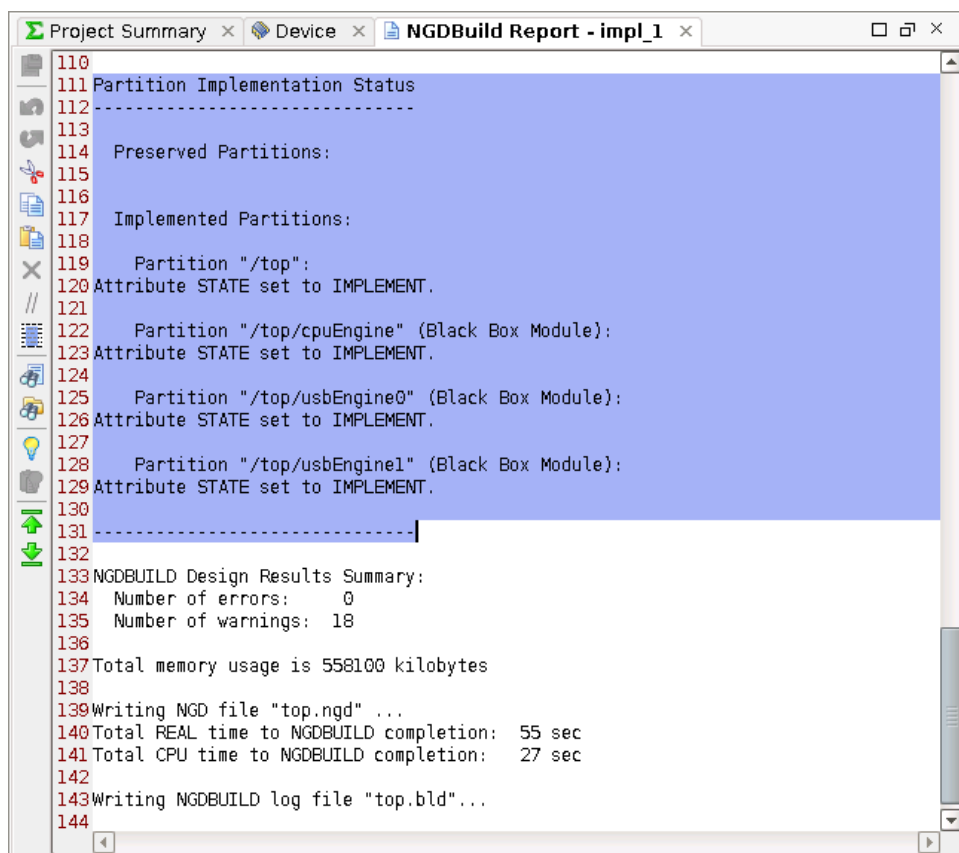
Figure 9: Partition Implementation Status in Report Files

The three team member partitions are all listed as Black Box Module. Partition information is provided in every report file (NGDBuild, Map, and PAR). This allows you to easily verify the status of all partitions on a given run.

6. In the Implementation Completed dialog box, select **Promote Partitions**, and click **OK**.

The Promote Partitions dialog box opens as seen in Figure 8.

Step 4: Promoting Synthesis and Creating Team Member Projects

The design is now ready for the team members to start their work.

- Before generating PlanAhead projects for each team member, promote the initial *synthesis* results.

- Because the *implementation* results of the previous step are not used by team members, the *implementation* results do not need to be promoted.

Promoting Successful Synthesis Results

To promote the successful synthesis results after synthesis (or implementation) has completed:

1. Click **Promote Partition** in the Flow Navigator (located under Implementation), if the Promote Partitions dialog box is not already open.

2. In the Promote Partitions dialog box, select the top partition in the **synth_1** run to be promoted.

Figure 10: Promote Partitions Dialog Box

Do not to promote other partitions at this stage. No useful data exists for the other partitions. Promoting them will require additional steps by each team member to change the promoted partition state values back to implement for their runs.

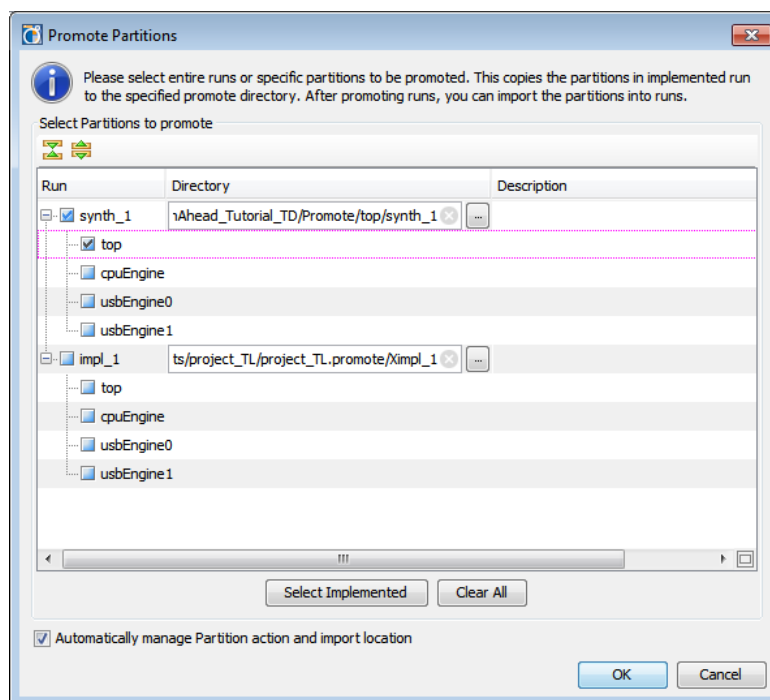3. Set the Directory for the **synth_1** run to:

   ```
   <Extract_Dir>/Promote/top/synth_1
   ```

   The default Directory setting could be used, but since this promoted synthesis data will be accessed by multiple team members it is more effective to promote the data to a location outside of the project directory.

4. Enter an optional description about the promoted data.

5. Verify that **Automatically Manage Partition Action and Import Location** is checked.

   Checking this option enables the PlanAhead tool to update the partition state and import directory for the next synthesis run, whether by the team leader or by a team member. If this box is not checked, the team leader must manage these attributes.

6. Click **OK** to promote the top partition synthesis results.

7. The Promoted Partitions view now appears, as seen in Figure 9.

   You can open this view using the **Window > Promoted Partitions** command from the main menu. You can close it by clicking on the **Close Window** icon. ×
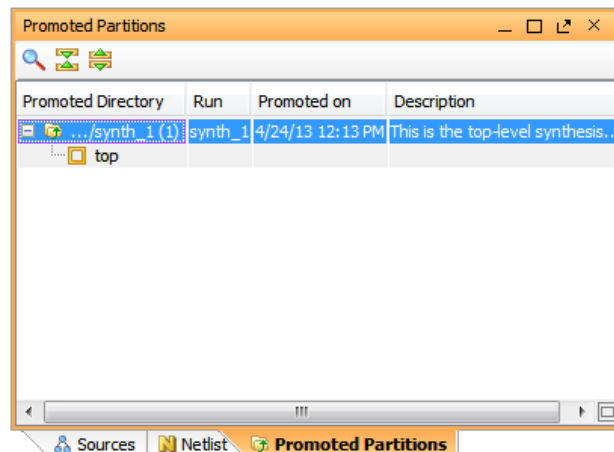
Figure 11: Promoted Partitions

8. In the Flow Navigator, under Project Manager, select the Specify Partitions command to open the Specify Partitions dialog box, as shown in Figure 10.

   The Specify Partitions dialog box shows in the Action column that the top partition will be imported from the location specified in the Import From column. The Specify Partitions dialog box lets you choose the appropriate action for the different partitions used in the design. You can choose to import a partition that has been previously synthesized or implemented, or re-implement the partition in the context of the design. You will examine this topic in greater detail later in this tutorial.

9. Click **Cancel** to close the **Specify Partitions** dialog box.
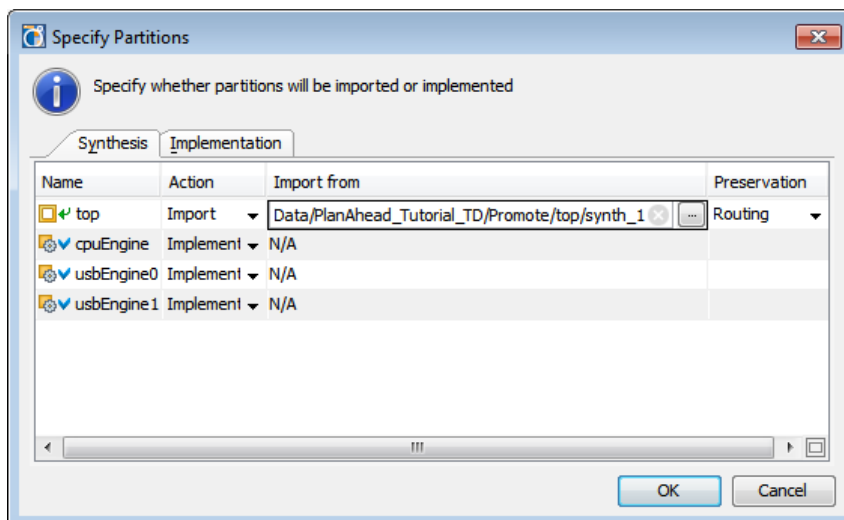
Figure 12: Specify Partitions

Creating Team Member Projects for usbEngine and cpuEngine

To create a consistent starting point for all team members, create multiple copies of the current project. For this tutorial, you will create two copies:

- One project for the **cpuEngine** partition,

- One project for the **usbEngine** partitions.

    The usbEngine instances are copies of a single module, and will be managed by a single team member.

To create team member projects for **usbEngine** and **cpuEngine:**

1. Select **File > Save Project As**.
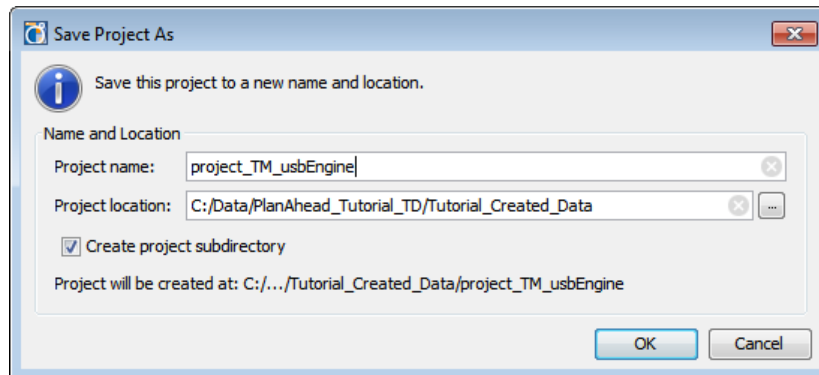
Figure 13: Save Project As

2. Enter **project_TM_usbEngine** as the Project Name

3. Specify the following as the Project location:

   <Extract_Dir>/Tutorial_Created_Data

4. Verify **Create Project Subdirectory** is checked.

5. Click **OK**.

6. Repeat 1 through 5 above, with the following parameters:

   • Project Name: **project_TM_cpuEngine**

   • Project location: ***<Extract_Dir>*/Tutorial_Created_Data**

At this time, you should have three projects for the design team to work from:

• *<Extract_Dir>*/Projects/project_TL: The original top-level design project created by the team lead.

• *<Extract_Dir>*/Tutorial_Created_Data/project_TM_usbEngine: The project to be used by the team member working on the two usbEngine partitions.

• *<Extract_Dir>*/Tutorial_Created_Data/project_TM_cpuEngine: The project to be used by the team member working on the cpuEngine partition.

In addition, you have created the synthesis data for the top-level partition, and stored it in a separate partition repository, under *<Extract_Dir>*/Promote.

In the next step of the tutorial you will switch roles, to change from team leader to the designer of the cpuEngine partition.

Step 5: Working on cpuEngine as Team Member

Acting as the team leader in the previous steps, you:

- Set up the design.

- Created a workspace for each team member.

You will now switch roles and implement each block as a team member.

While the work of the team members is usually done in parallel, for this tutorial each team member block is handled sequentially.

For each team member project, you will:

- Update the project sources to include the completed logic for the team member block.

- Synthesize the project.

- Implement the project.

- Promote the results.

Adding Sources to cpuEngine

Begin by adding the design sources to the **cpuEngine** project since it is already open from the last step. Make sure that the current PlanAhead project is **project_TM_cpuEngine**. If it is not, open this project now.

To add sources to **cpuEngine**:

1. Switch to the Project Manager view by click on Project Manager in the Flow Navigator.

2. In the Sources window, use the Hierarchy tab to expand top and select cpuEngine (`or1200_bb.v`).

    This is the black box module for **cpuEngine** that was used for the initial project. You will now replace this black box module with logic.

3. Right-click, and select **Remove File from Project**.
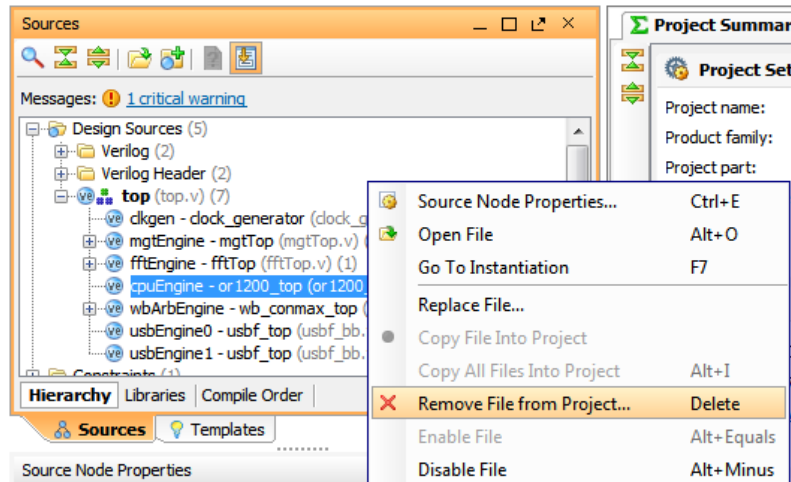
Figure 14: Remove or1200_bb.v Black Box Module

The Remove Sources dialog box opens.
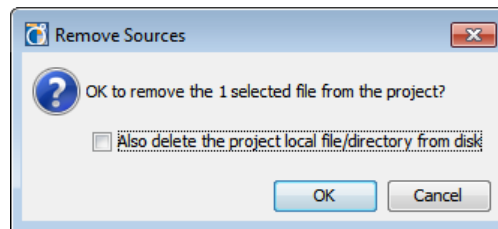
Figure 15: Remove from Project

4. Click **OK**.

5. At the top of the Sources window, click the Add Sources icon.

6. From the Add Sources wizard, select **Add or Create Design Sources**.

7. Click **Next**.

8. Click **Add Directories** to add the completed sources for the **cpuEngine** instance.

9. Browse to the following location:

    <Extract_Dir>/Sources/hdl/.

10. Select the or1200 directory.

11. Click **Select**.
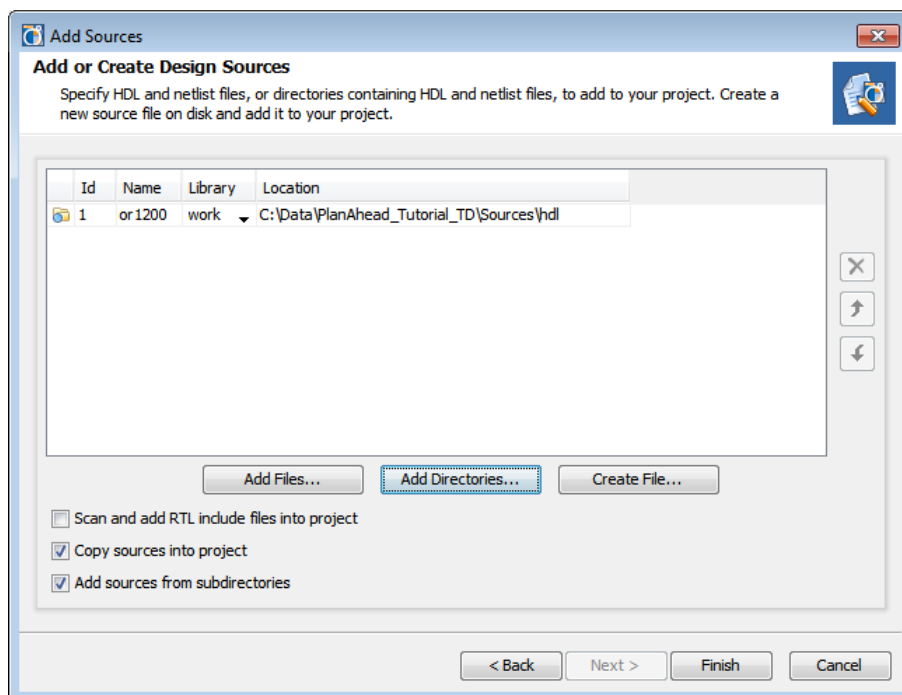
Figure 16: Add Source Directories – or1200

12. Verify the directory to be added.

13. Click **Finish**.

14. In the Hierarchy tab of the Sources view, you should see the cpuEngine module can now be expanded.

Synthesizing and Implementing cpuEngine

The Elaborated Design and Synthesized Design views are now out of date. To update them, you will:

- Reload (or close and reopen) these views.

- Verify the partition settings for synthesis and implementation.

- Launch the runs.

- Promote the results.

To reload the design:

1   If the Elaborated Design view was closed, click **Open Elaborated Design** in the Flow Navigator to load the latest version of the design.

2. If the Elaborated Design view is open, the banner across the top states that the view is out of date. Click **Reload** to reload the view.
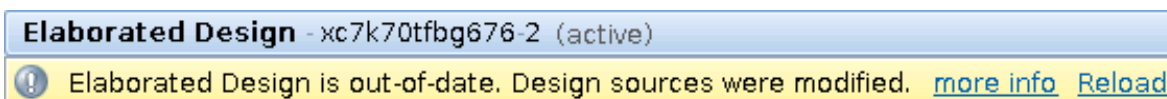
Figure 17: Design Out-of-Date

3. Click **OK** to clear the Critical Message dialog box.

4. In the Netlist view, verify that **cpuEngine** is no longer a black box, and also note that the two usbEngine instances remain black boxes in the current project.

5. In the Flow Navigator, under Project manager, click **Specify Partitions**.

6. In the Specify Partitions dialog box, from the **Synthesis** tab, verify that:

    a) Top is set to **Import**.

    b) All other partitions are set to **Implement**.

    At this point, there is no other data to import besides the top-level synthesis results provided by the team leader. Top is the only partition that has been promoted.

    If Top is not set to *import* for synthesis, either of the following might have occurred:

    - Top was not promoted correctly.

    - Automatically Manage Partition Action and Import Location was not checked in the Promote Partition dialog box.

    If Top was not correctly promoted, it cannot be imported now. You must return to Step 4: Promoting Synthesis and Creating Team Member Projects, to promote the top partition.

Figure 18: Specify Partitions Dialog Box

7. Click the Implementation tab to verify that all partitions are set to **Implement**.
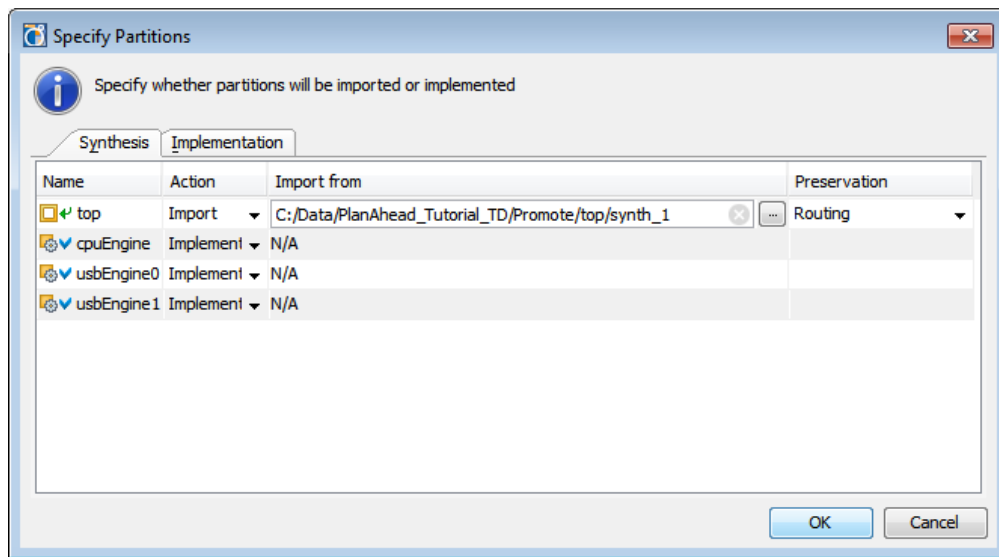
8. Click **OK** to close the **Specify Partitions** dialog box.

Note: To save time, instead of running synthesis and implementation in the following sequence, open the completed project at: <Extract_Dir>/Projects/project_TM_cpuEngine_completed. When the project is open, from the Flow Navigator select **Open Implemented Design**.

9. In the Flow Navigator, click **Run Implementation** to synthesize and implement the design.

10. If prompted, click **Yes** to launch synthesis prior to implementation.

11. In the Implementation Completed dialog box, select **Open Implemented Design**.

12. If prompted, click **No** to not **close** the **Elaborated Design**.

13. Click **OK** to any **Undefined Modules Found** or **Critical Messages** dialog boxes. These are expected messages.

Verifying and Promoting Results of cpuEngine

With the Implemented Design open, the Device view shows that:

- The Pblock for **cpuEngine** is relatively full.

- The two Pblocks for the **usbEngine** modules are relatively empty.

    Because the **usbEngine** instances were black boxes, no logic exists for these two blocks in the implemented design. Logic elements belonging to the top partition is placed in the **usbEngine** Pblocks because it was not restricted from being placed there.

    The Highlight Primitives command, in the popup menu of the Device view, can be used to create a highlighted view as shown in the following figure.
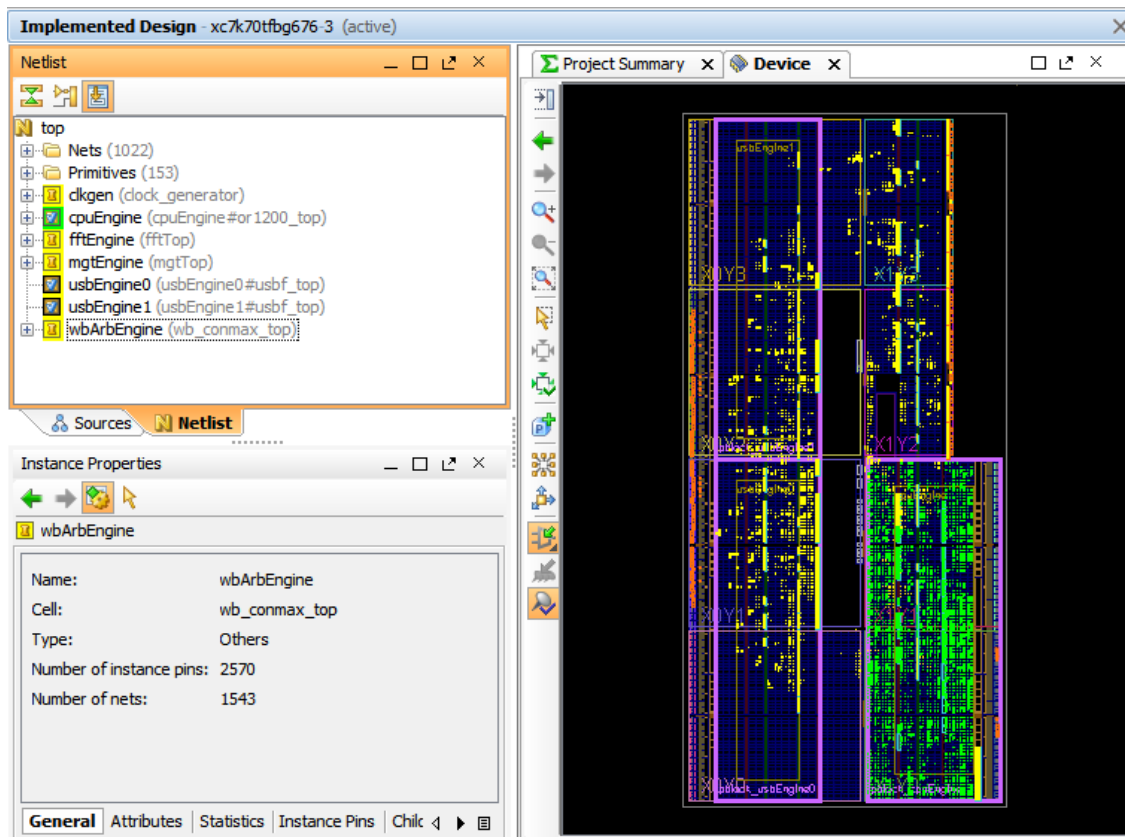
Figure 19: Implemented Design - cpuEngine

4. To verify that timing has been met, review any of the following:

    -   The Timing Score in the Design Runs view

    -   The details of the Timing Results window

    -   The Timing Score in the Project Summary window

5. In the Flow Navigator, click **Promote Partitions** to promote the successful synthesis and implementation results.

    Note: If the Elaborated Design view is not opened, you are prompted to open it.

6. Select only the **cpuEngine** instance in both the synthesis and implementation runs.

7. Set the `Promote` directories.

    -   `synth_1: <Extract_Dir>/Promote/cpuEngine/synth_1`

    -   `impl_1: <Extract_Dir>/Promote/cpuEngine/impl_1`

    The `Promote` directory used in team design should be a network location or repository that is accessible by all team members. This tutorial changes the default promote location to a folder outside the project directory structure to emulate such a location.
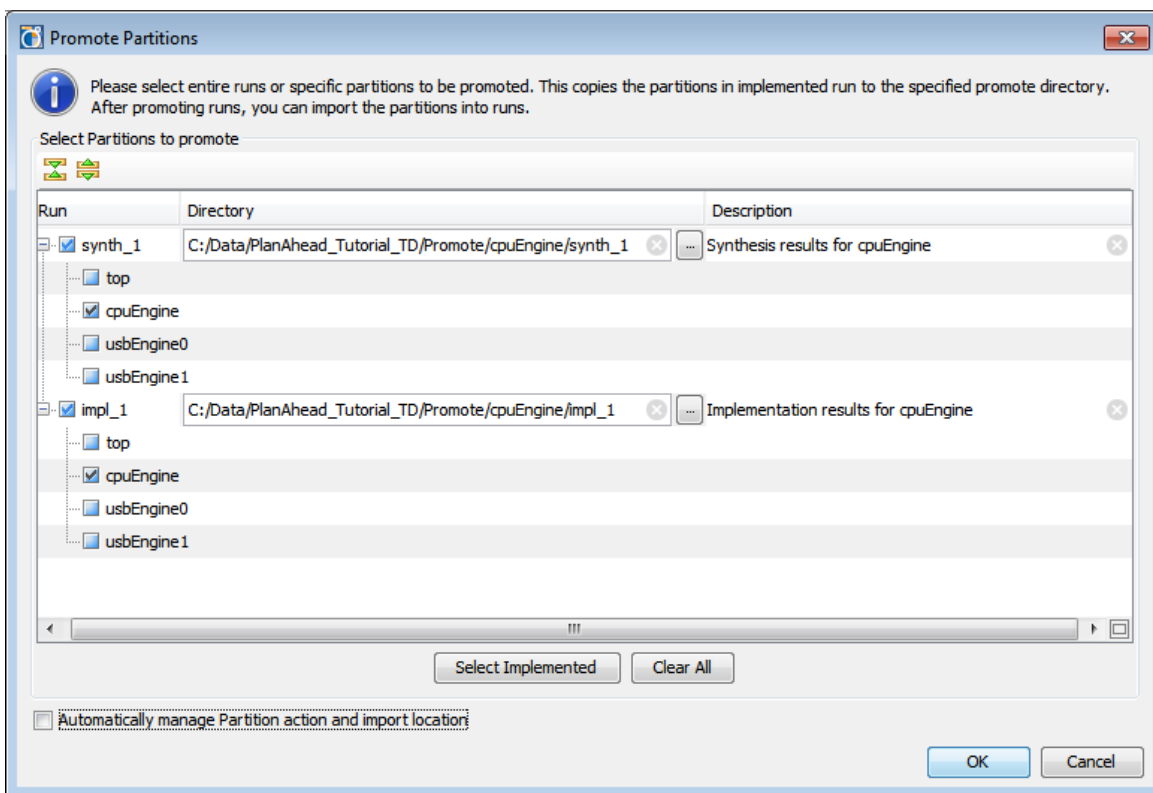
Figure 20: Promote cpuEngine

8. Uncheck **Automatically Manage Partition Action and Import Location**.

   While disabling **Automatically Manage Partition Action and Import Location** is not critical to this tutorial, Xilinx recommends removing it for team members in a team design flow.

   The **cpuEngine** team member might continue working on this block. Removing this option prevents the software from automatically importing an updated **cpuEngine** partition on the next run. This way the promoted partition results can be imported by the Team Leader as needed or as appropriate, rather than every time the cpuEngine designer makes a change.

9. Click **OK** to promote the partitions.

Step 6: Working on usbEngine as Team Member

In this Step, you will repeat the procedures of Step 5 as a team member working on **usbEngine**.

If multiple processors are available, you can perform this step in parallel while the **cpuEngine** project is implementing.

Adding Sources to usbEngine

To add sources to usbEngine:

1. Close the current open project unless:

    - You are doing this step in parallel, and

    - The **cpuEngine** has not yet finished implementation, or has not been promoted.

2. Open the PlanAhead project:

    `<Extract_Dir>/Tutorial_Created_Data/project_TM_usbEngine`

3. Click the **Project Manager** view.

4. In the Sources view, use the Hierarchy tab to expand top and **select one** of the two **usbEngine**   instances (usbf_bb.v).

    This black box module definition is used for the two **usbEngine** instances in the initial project. It will now be replaced with logic.

5. **Right-click** to open the popup menu and select **Remove File from Project**.

6. Click **OK** in the **Remove Sources** dialog box.
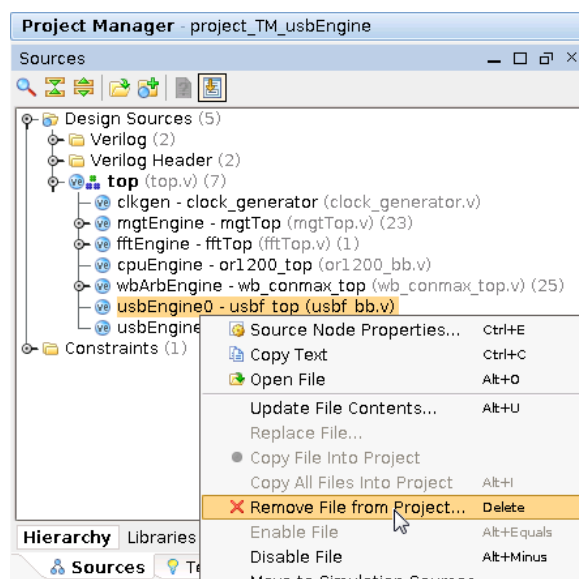
Figure 21: Remove Black Box Module usbf_bb.v

8. At the top of the Sources window, click the **Add Sources** icon.

9. From the Add Sources wizard, select **Add or Create Design Sources**.

10. Select **Next**.

11. Click **Add Directories**.

12. Browse to: *<Extract_Dir>*/Sources/hdl/

13. Select the usbf directory to add the completed sources for the **usbEngine** instance.

14. Click **Select**.

15. Click **Add Files**

16. Select the file: *<Extract_Dir>*/Sources/hdl/rtlRam.v

17. Verify the file and directory to be added.

18. Click **Finish**.

Figure 22: Add Sources - usbEngine

Synthesizing and Implementing usbEngine

To synthesize and implement **usbEngine:**

1. In the Flow Navigator, click **Open Elaborated Design** to open the Elaborated Design view.

2. Click **OK** to close the **Critical Messages** dialog box.
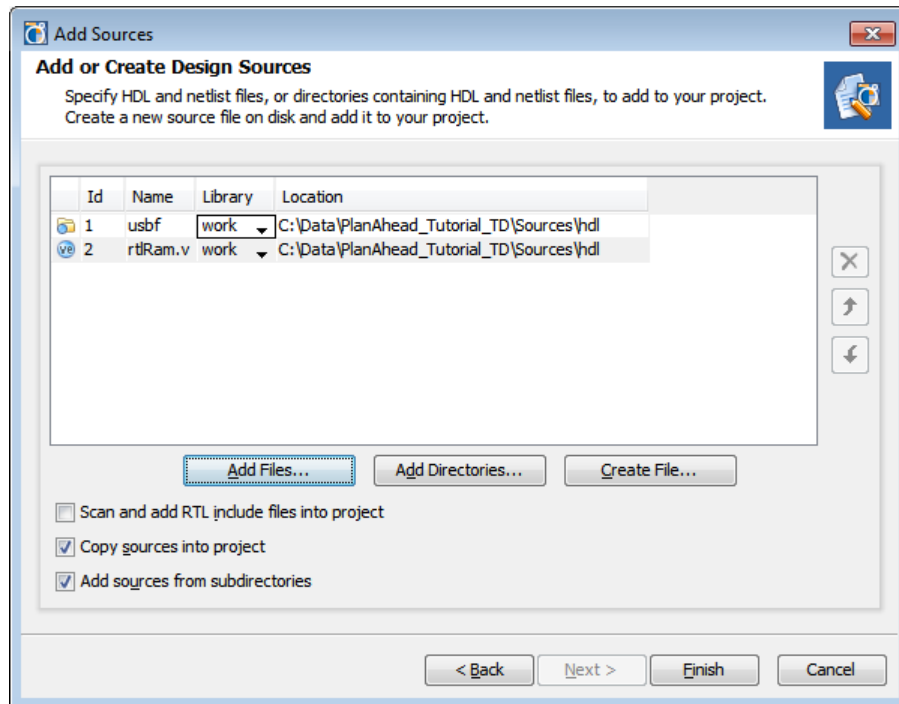
3. Verify that the two **usbEngine** instances are no longer black boxes.

    Notice that in this version of the design, the cpuEngine is still a black box.

4. In the Flow Navigator, under Project Manager, click **Specify Partitions**.

5. From the Synthesis tab, verify that:

    a) Top is set to **Import**.

    b) All other partitions are set to **Implement**.

    There is no other data to import besides the top-level synthesis results. Top is the only partition that has been promoted.

    If Top is not set to *import* for synthesis, either of the following might have occurred:

    *   Top was not promoted correctly.

    *   Automatically Manage Partition Action and Import Location was not checked in the Promote Partition dialog box.

    If Top was not correctly promoted, it cannot be imported now. You must start over at [Step 4: Promoting Synthesis and Creating Team Member Projects](#), or earlier.

6. Click the **Implementation** tab to verify that all partitions are set to **Implement**.

7. Click **OK** to exit the Specify Partitions dialog box.

Note: To save time, instead of running synthesis and implementation in the following sequence, open the completed project at: ***<Extract_Dir>*/Projects/project_TM_usbEngine_completed**. When the project is open, from the Flow Navigator select **Open Implemented Design**.

8. In the Flow Navigator, click **Run Implementation** to synthesize and implement the design.

9. If prompted, click **Yes** to launch synthesis prior to implementation.

10. In the Implementation Completed dialog box, select **Open Implemented Design**.

11. Click **No**, if prompted to **close** the **Elaborated Design**.

12. Click **OK** to any **Undefined Modules Found** or **Critical Messages** dialog boxes. These are expected messages.

Verifying and Promoting Results of usbEngine

With the Implemented Design open, the Device view shows that:

- The Pblocks for **usbEngine0** and **usbEngine1** are relatively full.
- The Pblock for the **cpuEngine** instance is relatively empty.

  Because the **cpuEngine** instance was a black box, it is expected to be empty. However, some logic can be seen in this region. The logic from the top level partition was not restricted from being placed inside the **cpuEngine** Pblock.

  You can use the Highlight Primitives tool to create a highlighted view.
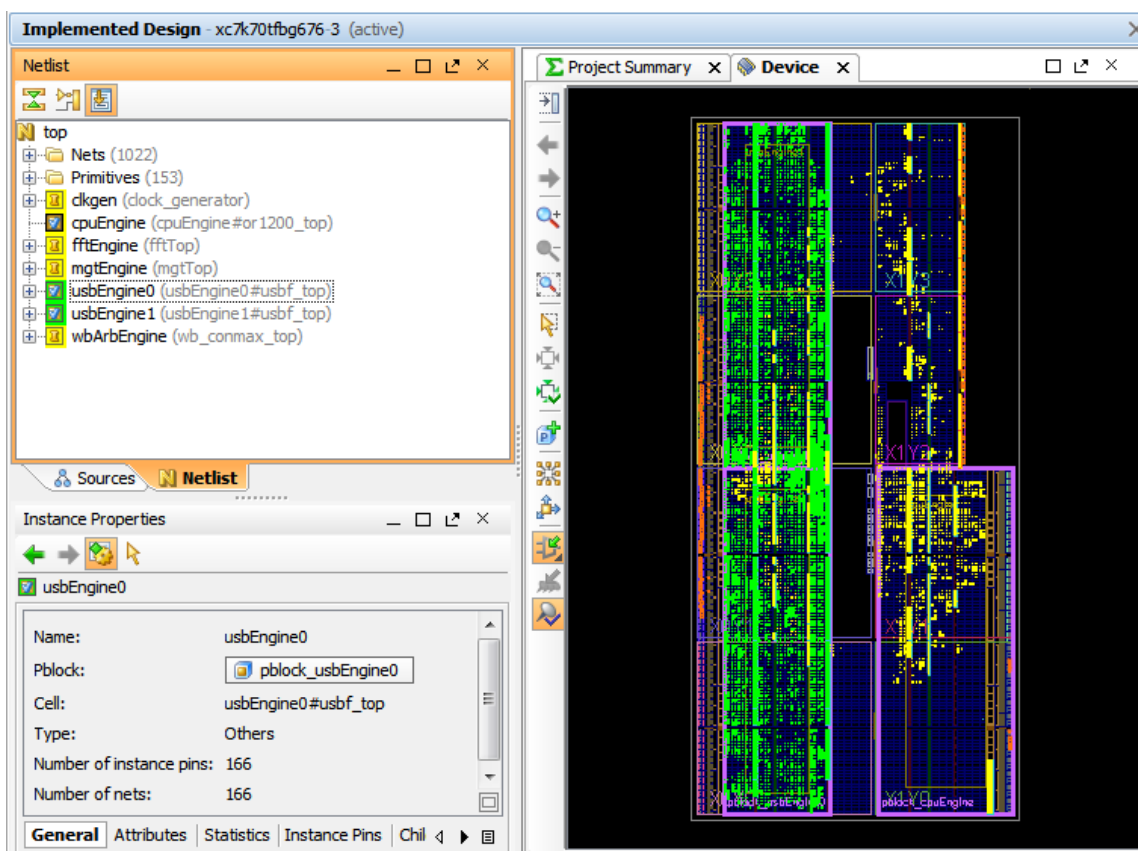

Figure 23: Implemented Design - usbEngine

1. To verify that timing has been met, review any of the following:

   - The Timing Score in the Design Runs view
   - The details of the Timing Results window
   - The Timing Score in the Project Summary window

2. In the Flow Navigator, click **Promote Partitions** to promote the successful synthesis and implementation results.

3. If the Elaborated Design view is not opened, you are prompted to open it.

4. Select only the **usbEngine0** and **usbEngine1** instances in both the synthesis and implementation runs.

5. Set the Promote directories.

    *   `synth_1: <Extract_Dir>/Promote/usbEngine/synth_1`

    *   `impl_1: <Extract_Dir>/Promote/usbEngine/impl_1`

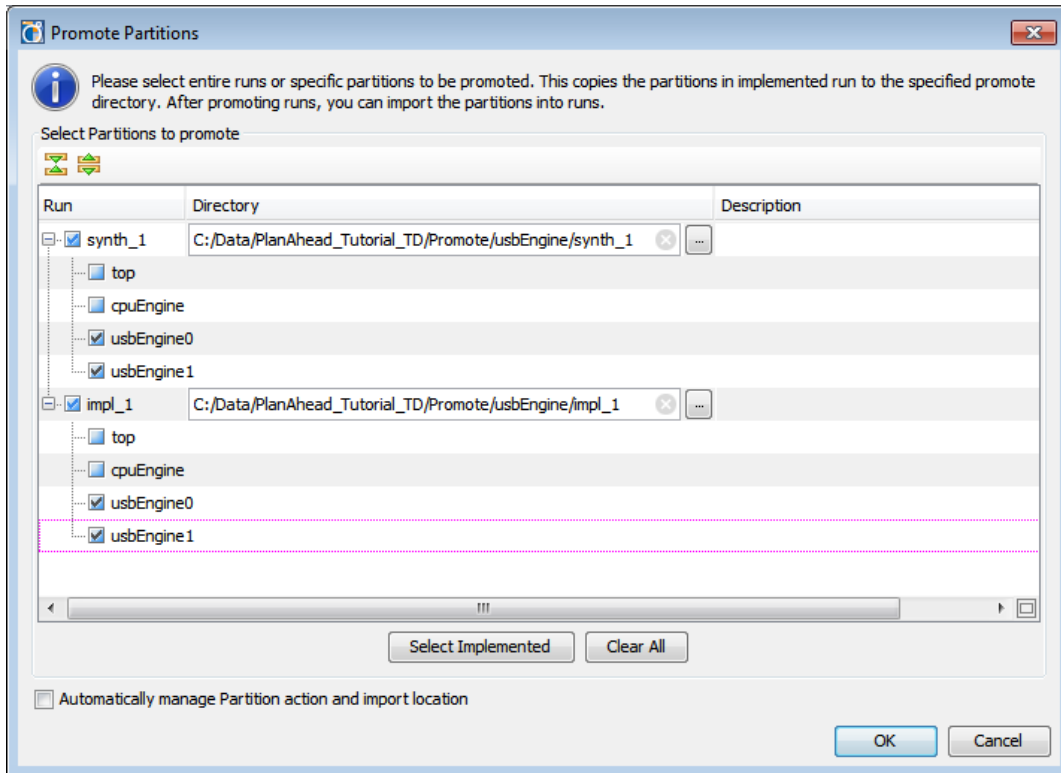6. Uncheck **Automatically manage Partition action and import location**.

Figure 24: Promote Settings for usbEngine0 and usbEngine1

7. Click **OK** to promote the **usbEngine0** and **usbEngine1** partitions.

8. After the partitions have been promoted, you can **close** the **current project**.

Step 7: Running the Assembly as Team Leader

In the previous steps, each team member synthesized, implemented, and promoted a version of their block. The team leader can now assemble the design. The team leader:

- Reopens the team leader project.
- Sets up the partitions for import.

Setting Up the Team Leader Project To Do an Assembly Run

To set up the team leader project to do an assembly run:

1. **Reopen** the following **project**:

   `<Extract_Dir>/Projects/project_TL`

   This is the original project. It already contains:

   - The defined team member partitions.
   - The successful synthesis results for the top module.
   - The Pblocks for the team member blocks.

   Now, update the project to define the team member blocks as logic instead of black boxes. To do this, add the netlists files (NGC) from the successful synthesis runs of each team member's promoted partition.

2. From the Project Manager, click **Add Sources**.

3. Select **Add or Create Design Sources**.

4. Click **Next**.

5. Select **Add Files**.

6. Add the following files:

   - `<Extract_Dir>/Promote/usbEngine/synth_1/usbEngine0#usbf_top.ngc`
   - `<Extract_Dir>/Promote/usbEngine/synth_1/usbEngine1#usbf_top.ngc`
   - `<Extract_Dir>/Promote/cpuEngine/synth_1/cpuEngine#or1200_top.ngc`
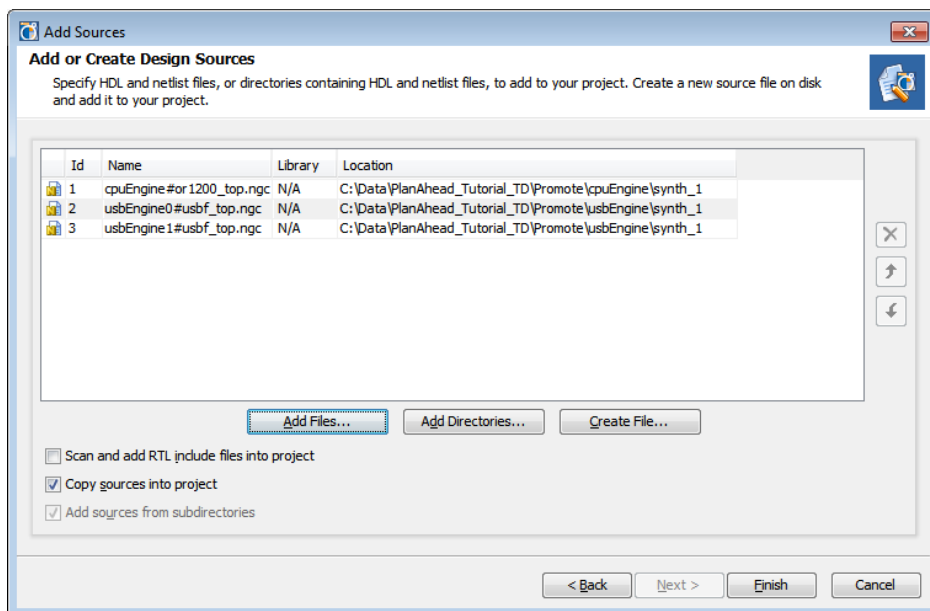
7. Click **Finish**.

Figure 25: Add Post Synthesis Results for Team Member Partitions

8. In the Flow Navigator, click **Open Synthesized Design**.

    All partitions are now promoted and defined for this project. It is not necessary to rerun synthesis. The latest synthesis results of all team members (including the team leader) are used for this assembled design.
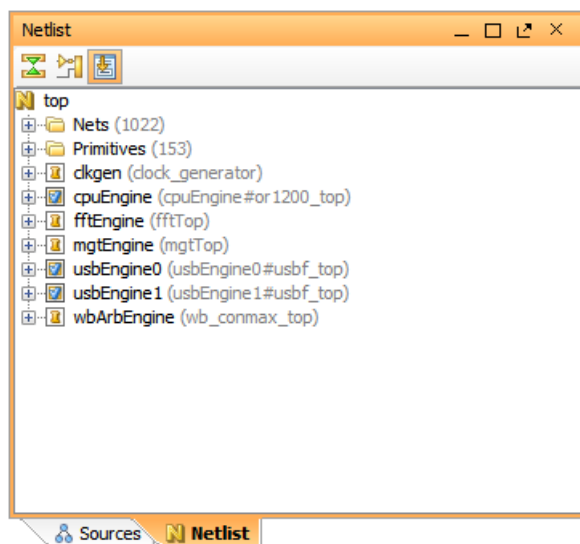

Figure 26: Synthesized Design with All Partitions Promoted

Updating Partition Settings and Running the Assembly

To update partition settings and run the assembly:

1. In the Flow Navigator, click **Specify Partitions** and access the **Implementation** Partition settings. The Synthesis tab can be left as is since synthesis is not being run again.

2. Leave the Top partition action as **Implement**.

3. Change the following remaining partition actions to **Import**:

    - cpuEngine
    - usbEngine0
    - usbEngine1

4. Change the **Import from** field to the location to which the team members promoted the implementation results.

    - cpuEngine: <Extract_Dir>/Promote/cpuEngine/impl_1
    - usbEngine0: <Extract_Dir>/Promote/usbEngine/impl_1
    - usbEngine1: <Extract_Dir>/Promote/usbEngine/impl_1

Because both **usbEngine** instances were implemented together and promoted together, the **Import From** location is also the same.
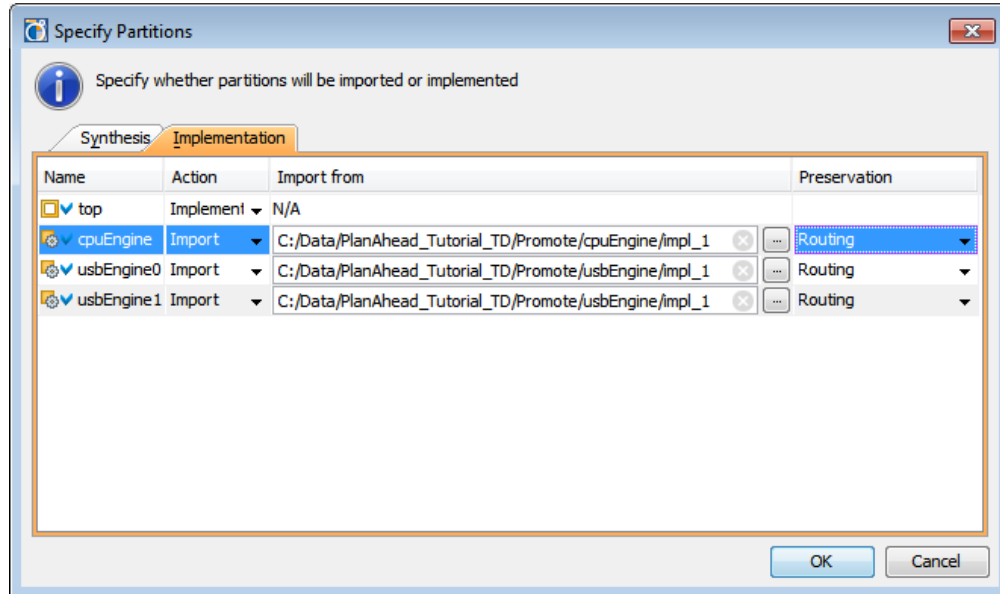

Figure 27: Partition Settings for Assembly Run

5. Click **OK**.

6. Click **OK** on the **Reset out-of-date run** dialog to reset **impl_1**.

Note: To save time, instead of rerunning implementation on the current project, open the completed project at: `<Extract_Dir>/Projects/project_TL_assembled`. When the project is open, from the Flow Navigator select **Open Implemented Design**.

7. Click **Run Implementation** in the Flow Navigator to launch implementation and assemble the promoted partitions into the top-level design of the Team leader.

8. In the Implementation Completed dialog box, select **Open Implemented Design**.

There should be no **Critical Messages** or **Undefined Modules Found** dialog boxes. These would be unexpected messages.

Verifying and Promoting Assembly Results

In this design:

- Each team member block is logically isolated from other team member blocks.

- All the boundaries are registered.

- The placement of each team member block was sufficient the first time through.
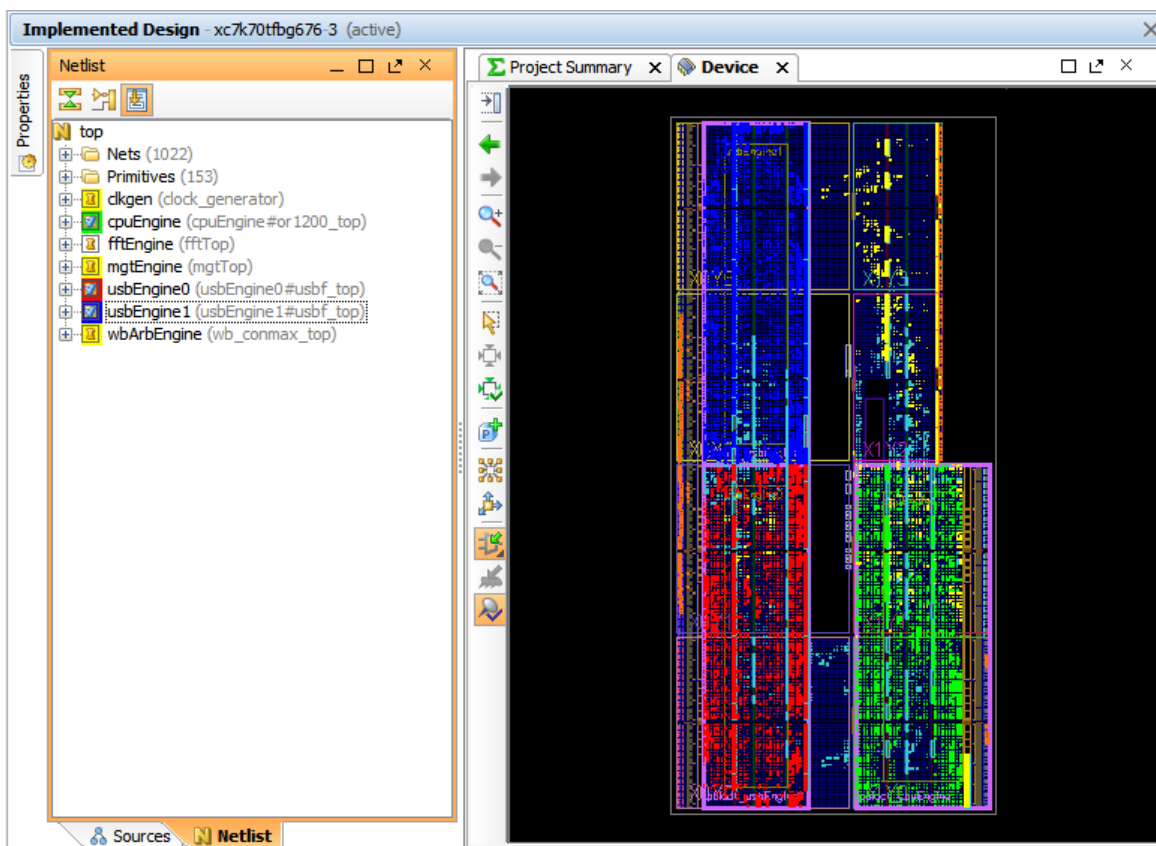

Figure 28: Implemented Design View of the Assembled Design

For more complex designs, this assembly run may be the first of many. The process described in this tutorial may be repeated as necessary.

Each team member project can now start to import other team member blocks from this promoted assembly run. This helps interface timing to converge early in the design cycle, instead of leaving other team member blocks as black boxes and discovering interface timing issues at the end of the design.

With the Implemented Design view open, you can see the entire design, as seen in Figure 27. You can use the Highlight Primitives command to create this highlighted view.

Verifying That Timing Has Been Met

To verify that timing has been met, review any of the following:

- The Timing Score in the Design Runs view
- The details of the Timing Results window
- The Timing Score in the Project Summary window

Verifying That All Team Member Partitions Were Imported

To verify that all team member partitions were imported, review the Implemented Partition section of the Project Summary view.
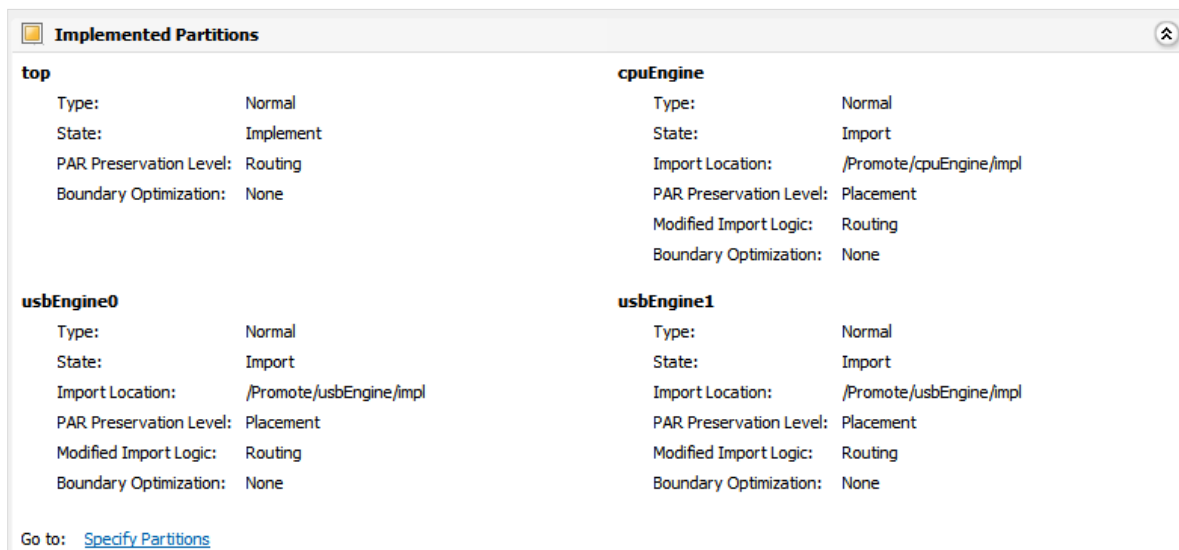

Figure 29: Partition Summary Section of Project Summary

Promoting Successful Synthesis and Implementation Results

Modifications to the design may require some or all of this flow to be repeated. Using these successful assembly results in future iterations may be beneficial. To promote the successful synthesis and implementation results:

1. In the Flow Navigator, click **Promote Partitions**.

2. If the Elaborated Design view is not opened, you are prompted to open it. Click **OK**.

3. Select all partitions in both the synthesis and implementation to be promoted.

    Because the placement of the Top partition meets all interface timing, each team member can now begin to import Top, as well as other team member partitions to maintain this interface timing in all future iterations.

4. Set the `Promote` directories:

    *   `synth_1: <Extract_Dir>/Promote/top/synth_1`

    *   `impl_1: <Extract_Dir>/Promote/top/impl_1`

    Note: `Promote/top/synth_1` already exists from an earlier step, but you will need to add `impl_1` to the `Promote/top` folder.
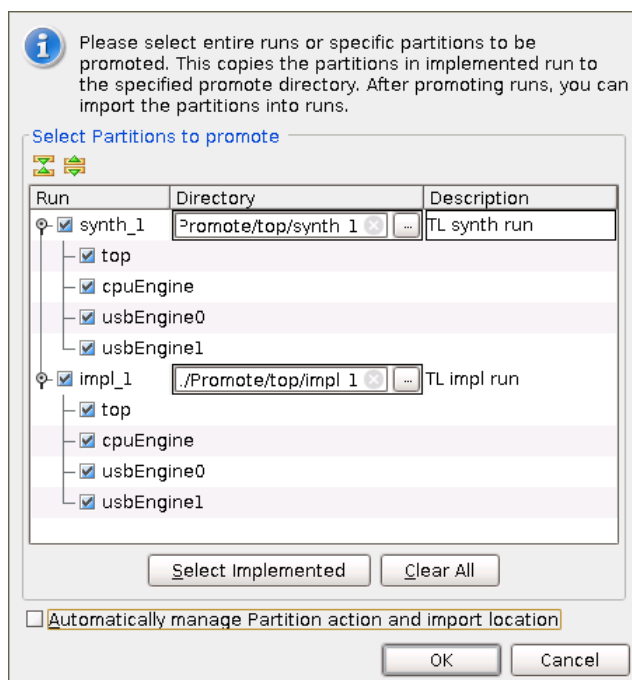

Figure 30: Promote Settings for Assembled Design

For this tutorial, the synthesis results for the team leader have not changed from when they were last promoted. However, the team leader might develop additional logic in the top

level design in parallel with the other team members. Promoting synthesis and implementation now ensures that all team members can work on the latest design.

5. Uncheck **Automatically Manage Partition Action and Import Location**.

   Disabling **Automatically Manage Partition Action and Import Location** prevents the software from automatically changing the import locations of the team member partitions to the location to which they were just promoted (`Promote/top`).

   Instead, the software maintains the locations defined in the previous steps. This simplifies running the assembly step in future iterations.

6. Click **OK**.

Conclusion

In this tutorial, you did the following:

- Used partitions and the Team Design methodology to synthesize and implement a design in multiple parts.

- Assembled the full design.

- Synthesized and implemented blocks as black boxes.

- Promoted successfully synthesized and implemented partitions to a central repository.

- Created PlanAhead projects for each team member.