RTL and Technology Schematic Viewers Tutorial

UG685 (v14.1) April 24, 2012

This tutorial document was last validated using the following software version: ISE Design Suite 14.1

If using a later software version, there may be minor differences between the images and results shown in this document with what you will see in the Design Suite.

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/01/11	13.1	Updated to show that design is available from ISE Examples. Updated graphics.
10/19/11	13.3	Revalidated for the 13.3 release. Editorial updates only; no technical content updates.
01/18/12	13.4	Revalidated for the 13.4 release. Editorial updates only; no technical content updates.
04/24/12	14.1	Revalidated for the 14.1 release. Editorial updates only; no technical content updates.

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Chapter 1

Schematic Viewer: Brief Overview

Design Flow Benefits

The goal of this tutorial is to provide a quick introduction to the main capabilities of the Schematic Viewer available from the ISE® Design Suite and how you can use these capabilities for design analysis and debugging. With the rapid growth in the size and complexity of FPGA designs, it is critical to have tools that ease the way you analyze and debug your designs.

Some common questions can be answered by using the Schematic Viewer:

- How is my HDL code interpreted by the synthesis tool?
- How is my HDL code mapped to the target technology?
- Where is my critical timing path situated?

In addition, today's advanced designs are often completed by several designers located in different parts of the world, where each designer is responsible for a part of the design. This complicates design analysis even further, and good debugging tools become critical.

Graphical tools such as the Schematic Viewer, PlanAhead™ tool, and FPGA Editor significantly simplify design analysis.

In this tutorial, we introduce the latest version of the Schematic Viewer, a tool which provides powerful ways to view and analyze your designs from different perspectives.

Key Features

The Schematic Viewer provides a flexible interface that allows you to focus on the part of the design that interests you. This ability to incrementally expand or "localize" the view on demand provides a significantly faster means to navigate through your design.

The Schematic Viewer provides you with powerful analysis features, such as:

- Drawing the schematic by selecting the only elements of interest
- Extracting Input and Output logic cones
- Removing objects that are not of interest
- Navigating Forward and Back history of previous analysis steps
- Working with multiple schematics of the same netlist

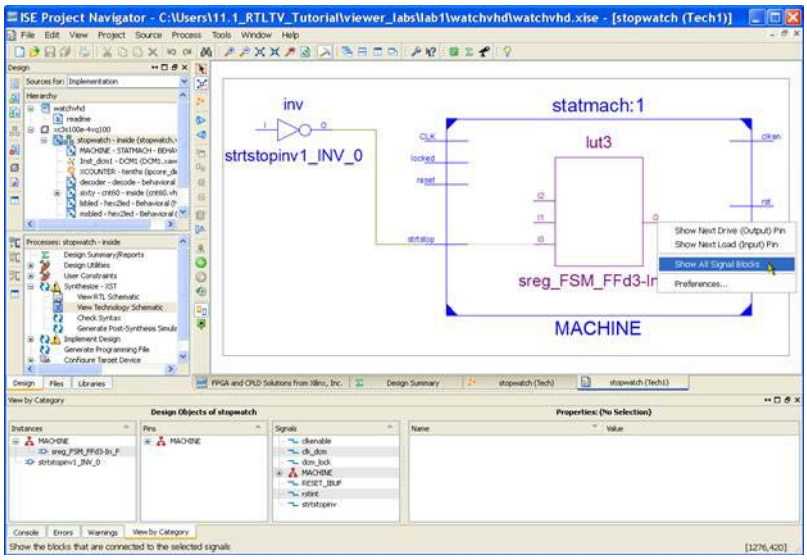

Figure 1-1: **Schematic Viewer**

The Schematic Viewer as shown in Figure 1-1 has significantly improved performance, which improves your ability to deal with higher complexity designs.

Ultimately, the Schematic Viewer provides you with the fundamental capabilities to visualize:

- RTL views of the design
- Post-synthesis netlists
- Critical timing path delays reported in the post-place and route timing report (from Timing Analyzer)

RTL View

RTL View is a Register Transfer Level graphical representation of your design. This representation (`.ngr` file produced by Xilinx Synthesis Technology (XST)) is generated by the synthesis tool at earlier stages of a synthesis process when technology mapping is not yet completed. The goal of this view is to be as close as possible to the original HDL code. In the RTL view, the design is represented in terms of macro blocks, such as adders, multipliers, and registers. Standard combinatorial logic is mapped onto logic gates, such as AND, NAND, and OR.

Post-Synthesis Netlist

Graphical representation of the post-synthesis ("optimized and mapped") netlist (`.ngc` file produced by XST) contains Xilinx primitives as defined in the UNISIM library, such as LUTs, DCM, I/O buffers, and flip-flops. The Schematic Viewer allows you to visualize the primitive properties and the constraints attached to them.

Critical Path View

When used as a cross probe target from the Timing Analyzer report, the critical timing path of your design is represented using the post-place and route netlist. This netlist is different from the post-synthesis netlist and represents your design in terms of slices.

Flexibility for Both Project Navigator and Command Line Users

Your particular design methodology (command line vs. Project Navigator) determines which set of features you can use in the Schematic Viewer. Use Table 1-1 to familiarize yourself with the features available to you.

Case 1: Project Navigator

Table 1-1: **Design Features**

Synthesis Tool	RTL View	Post-Synthesis Netlist	Critical Path	Notes
XST	Yes	Yes	Yes	Use ISE Design Suite to fully implement your design, and use XST as your synthesis tool.
Third party	-	-	Yes	Use ISE Design Suite to fully implement your design, and use a third-party synthesis tool.

Case 2: Command Line

Although you cannot launch Schematic Viewer in a standalone mode, there is a workaround to emulate this use model and enable you to use the Schematic Viewer to explore the XST RTL View or XST post-synthesis netlists. Post-map and post-place and route netlists are not handled in this mode.

Please refer to Chapter 10, Lab 7: Using the Schematic Viewer as a Standalone Tool for more information.

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Chapter 2

Tutorial Description

Overview

Throughout this tutorial, we will use the small stopwatch design which is delivered with the Xilinx® ISE® Design Suite installation as an example design. We intentionally selected a small design to allow you to complete the labs as quickly as possible.

Less than one hour is required to complete the entire tutorial which covers all major features.

We suggest:

- Running the labs in order. That said, the labs are independent and can be run in any order if you want to immediately focus on one particular functional area.
- Creating a separate design directory for each lab and copying the original design files to that directory. Please refer to Chapter 3, Lab Preparation: Getting Started, for more information.

Because the majority of Schematic Viewer features can be accessed using either the RTL, Post-Synthesis netlist, or Critical Path views, we will use the Post-Synthesis netlist view in the majority of labs to demonstrate the main features.

Table 2-1 gives you a brief overview of all the labs.

Table 2-1: **Lab Overview**

Title	Duration	Covered Features
Chapter 4, Lab 1: Basic Features	9 minutes	• Selecting Schematic Viewer startup mode • Working with the Explorer Wizard • Understanding the Schematic Viewer interface • Zooming views • Expanding schematics • Removing elements from a schematic • Coloring new elements • Navigating history • Using Start and End signal markers
Chapter 5, Lab 2: Working with Hierarchical Netlists	9 minutes	• Selecting hierarchical blocks in the Explorer Wizard • Expanding hierarchical blocks • Starting schematic exploration with the top-level block
Chapter 6, Lab 3: Using Schematic Viewer for Timing Analysis	6 minutes	• Visualizing critical paths in the Schematic Viewer • Annotating the critical path with path delays

Table 2-1: **Lab Overview**

Title	Duration	Covered Features
Chapter 7, Lab 4: Simplifying Design Analysis	7 minutes	• Using Start and End signal markers • Deleting schematic elements • Using multiple schematics of the same netlist • Starting a new schematic with selected elements • Using colors to mark various elements
Chapter 8, Lab 5: Comparing Two Design Implementations	5 minutes	• Loading and comparing two netlists of the same design
Chapter 9, Lab 6: Dealing with Large Designs	3 minutes	• Handling large designs
Chapter 10, Lab 7: Using the Schematic Viewer as a Standalone Tool	3 minutes	• Learning how command line users can take advantage of the Schematic Viewer

Prerequisites

The labs you will run through require some basic knowledge about the Project Navigator environment. Before starting these labs, you should know:

- How to open and close an existing project
- How to add a new UCF (implementation constraint file) to the project and specify basic timing constraints using Constraint Editor
- How to run the basic implementation flow
- How to launch and use Timing Analyzer

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Chapter 3

Lab Preparation: Getting Started

Installing a Design

Throughout the labs, you will use the small stopwatch design and target a Spartan®-3E xc3s100e-4-vq100 device. This design is delivered with the Xilinx® ISE® Design Suite installation.

1. In Project Navigator, select **File > Open Example**.
2. In the Open Example dialog box, select the **watchvhd** design and specify `c:\viewer_labs\labs1` as the Destination directory.

   The watchvhd project is unarchived in the specified destination directory and is opened for use in Project Navigator.

Setting Up Project Navigator Preferences

To ensure that the lab graphics provided in this tutorial match the schematic you see on your screen, you have to setup the Light Background Color Scheme for Schematic Viewer before starting the lab.

1. To open the Preferences dialog box, select **Edit > Preferences**.
2. In the left pane, expand **RTL/Technology Viewers** and select the **Color Scheme** sub-category.

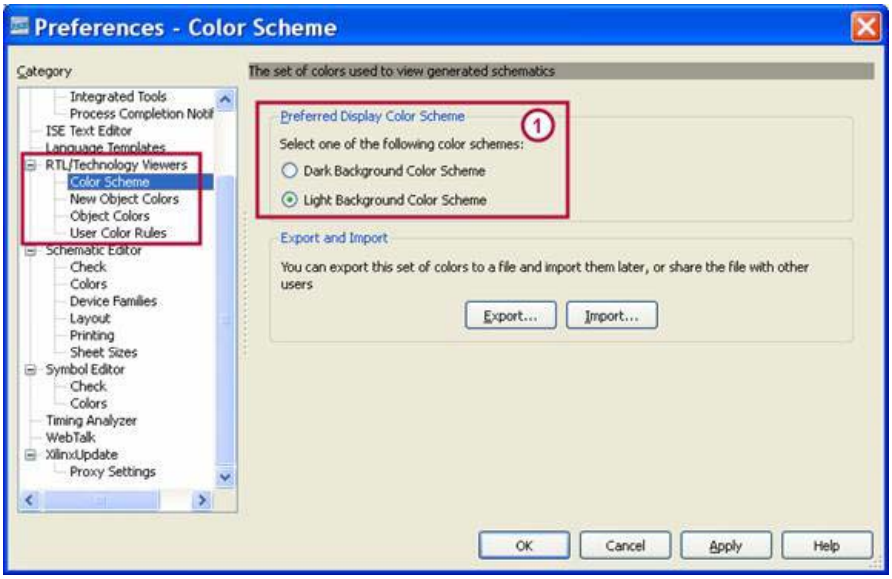

Figure 3-1: **Color Scheme Selection**

3. Select **Light Background Color Scheme** in zone 1 (see Figure 3-1) of the dialog box, click **Apply**, and click **OK** to finish.

Now you are ready to start the labs.

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Chapter 4

Lab 1: Basic Features

Objectives

The goal of this lab is to familiarize you with the basic Schematic Viewer operations which will be used extensively in later exercises. These include:

- Selecting Schematic Viewer startup mode
- Working with the Explorer Wizard
- Understanding the Schematic Viewer interface
- Zooming views
- Expanding schematics
- Removing elements from a schematic
- Coloring new elements
- Navigating history
- Using Start and End signal markers

Note: For the sake of clarity and simplicity, all the above features will be demonstrated using a flattened post-synthesis netlist. Hierarchical netlist navigation will be introduced in the next lab.

Lab

Step 1: Creating the Lab Project

Create and open the stopwatch project and set the **Light Background Color Scheme** for Schematic Viewer, as described in the Chapter 3, Lab Preparation: Getting Started.

Step 2: Setting XST Options and Synthesizing the Design

1. In the Processes pane, right-click **Synthesize - XST**, and select **Process Properties** to open the Synthesis Options dialog box.

2. Set the Keep Hierarchy option to **No** as shown in Figure 4-1.

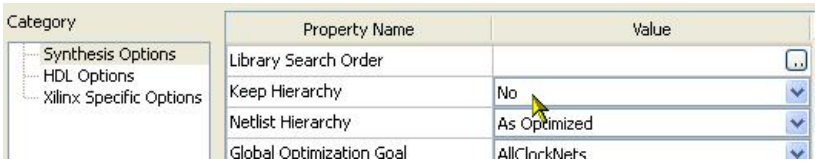

Figure 4-1: **Setting Keep Hierarchy Option**

3. Synthesize the design by double-clicking the **Synthesize - XST** process in the Processes pane.

Step 3: Launching the Explorer Wizard

Before you can view a schematic of your design, you need to select the elements you want to use as a starting point for your design exploration.

You can start design exploration in the two different startup modes:

- **Start with the Explorer Wizard**. In this mode, the Explorer Wizard is the initial screen, which allows you to select the elements that you want to see on the initial schematic. This mode will be used in the current lab.
- **Start with a schematic of the top-level block**. In this mode, the Explorer Wizard is bypassed and an initial schematic is created with only the top-level block displayed. You can then use the logic expansion capabilities of the Schematic Viewer to start expanding from the top-level block. You need to familiarize yourself with the basic Schematic Viewer operations and learn how you can manipulate hierarchical blocks before using this mode. Please refer to Chapter 5, Lab 2: Working with Hierarchical Netlists for more information on this startup mode.

1. After synthesis is complete, start the Schematic Viewer by double-clicking the **View Technology Schematic** process in the Processes pane, or, alternatively, by selecting **Tools > Schematic Viewer > Technology**.
2. Select the **Start with the Explorer Wizard** startup mode as shown in Figure 4-2.

Figure 4-2: **Set Viewer Startup Mode**

The Explorer Wizard enables you to select elements for exploration start up. See Figure 4-3.

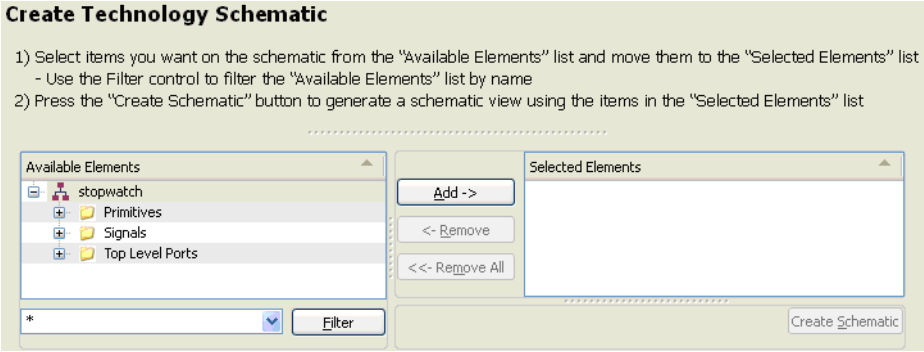

Figure 4-3: **Explorer Wizard**

The Available Elements window shows all the objects available in the design. They are classified in the following categories: primitives, signals, top-level ports, and hierarchical blocks.

Note: Hierarchical blocks are visible in hierarchical netlists only. Please refer to Chapter 5, Lab 2: Working with Hierarchical Netlists for more information on working with hierarchical designs.

3. In the Available Elements list, expand **Primitives**, select **MACHINE/sreg_FSM_FFd1** and **MACHINE/sreg_FSM_FFd1-In**, and add them to the Selected Elements list using the **Add** button. See Figure 4-4.

Figure 4-4: **Available Elements**

If the list of elements is too long, you can use the Filter to reduce the search scope. As an example in our case, you can specify **MACHINE/sreg_FSM_FFd1*** as a search criteria as shown in Figure 4-5.

Figure 4-5: **Filtering**

4. Click the **Create Schematic** button to create the schematic.

Step 4: Using the Schematic Viewer Interface

The Schematic Viewer graphical user interface (GUI) has the following components as shown in Figure 4-6.

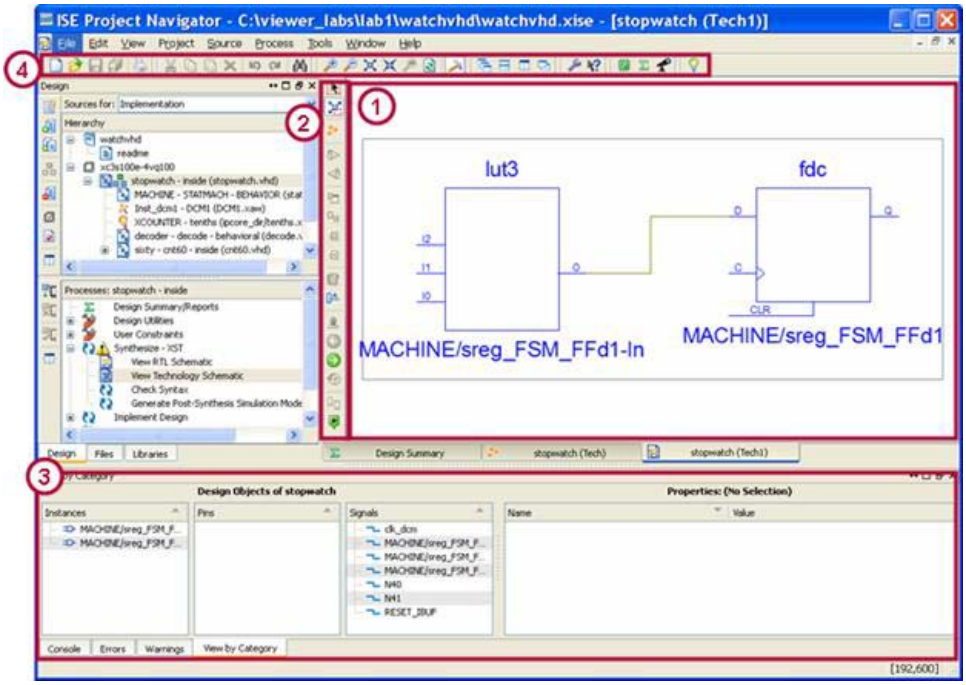

Figure 4-6: **Schematic Viewer**

1. **Workspace**: The schematic window is the main window where you explore your design by adding or removing elements.
2. **Schematic Viewer Toolbar**: This toolbar contains the functions specific to the Schematic Viewer.
3. **View by Category Panel**: This panel contains two types of information: objects visible on the schematic (instances, pins and signals) and object properties. For example, you can select a BRAM primitive in your schematic and see all its properties, including BRAM initialization values.

   Note: You must select the View by Category tab to see this panel.
4. **General Toolbar**: This toolbar contains functions shared by different graphical tools such as Zoom (shown in Figure 4-7).

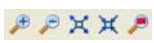

Figure 4-7: **Zoom Toolbar**

Note: Menu control functions are accessible from specific or general toolbars and can be invoked from the menus. For example, all zoom functions can be called from the **View > Zoom** menu.

We will mainly deal with the schematic window and toolbars in the labs.

Step 5: Zooming

Zooming is a basic function which is constantly used during design analysis. Schematic Viewer has five zooming operations which can be accessed from the general toolbar shown in Figure 4-7, or via the **View > Zoom** menu. However, the Schematic Viewer supports specific mouse stroke operations, allowing you to perform zoom operations more quickly.

We suggest that you play with different zoom operations to familiarize yourself with them. They will be very helpful during the rest of the tutorial. Table 4-1 gives an overview of Zoom operations and their access methods.

Table 4-1: **Zoom Functions**

Zoom Operation	Toolbar Button	Menu Command	Shortcut
Zoom In		**View > Zoom > In**	Do either of the following: • Press **F8**. • Click and drag down and to the left.
Zoom Out		**View > Zoom > Out**	Do either of the following: • Press **F7**. • Click and drag up and to the right.
Zoom to Full		**View > Zoom > To Full View**	Do either of the following: • Press **F6**. • Click and drag up and to the left.
Zoom to Box		**View > Zoom > To Box**	Starting from the upper left corner, click and drag to draw a bounding box around the area.
Zoom to Selected		**View > Zoom > To Selected**	Select the objects you want to center in the window, and press **F11**.

Step 6: Expanding the Schematic View

Although the initial schematic view is your starting point, you will typically want to expand the view to include more objects of interest. There are several ways to expand the schematic.

First, you need to select an element to which you would like to add a new (not yet visible) element. You can select the following types of elements to be expanded: net, block, pin of a block, and port.

To expand the view from the selected object, use the mouse right-click context menu and select the elements you want to add, such as drivers, loads, driver and loads, or to extract, such as an input or output logic cone.

On the current schematic, select different objects and observe the context menu. Although similar, the exact content depends on the object type chosen and where it is located in the design.

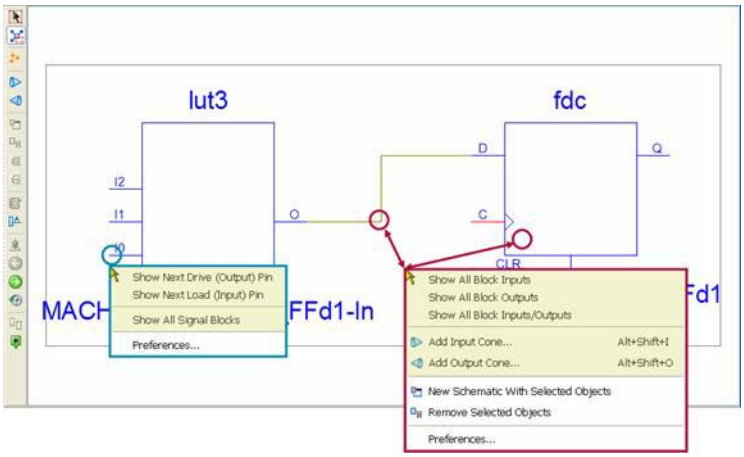

Figure 4-8: **Context Menu**

Example

1. Select the **I2** pin of the **lut3** primitive, and select **Show Next Drive (Output) Pin** from the context menu to see its driver. The following schematic appears, as shown in Figure 4-9.

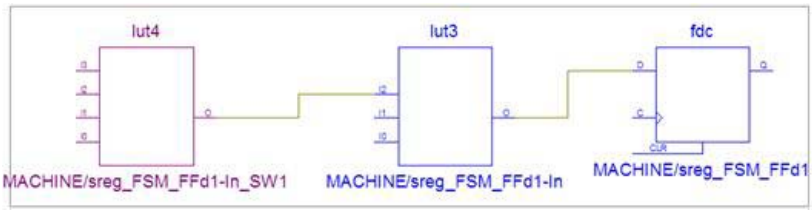

Figure 4-9: **Example Schematic**

2. The newly added lut4 element has a different color. The Schematic Viewer automatically colors newly added objects so they can be easily localized on the schematic. You can enable or disable this feature using the Schematic Viewer toolbar (see Figure 4-10). In addition, you can modify new object colors using the Preference menu.

Figure 4-10: **Colorize New Objects Button**

3. If you want to incrementally expand nets, block pins, or ports, you can just point the cursor on the desired object and perform a left mouse double-click. This is a very handy shortcut over using the context menu.

Double-click the **I0** pin of **lut3** primitive, and the result appears as shown in Figure 4-11.

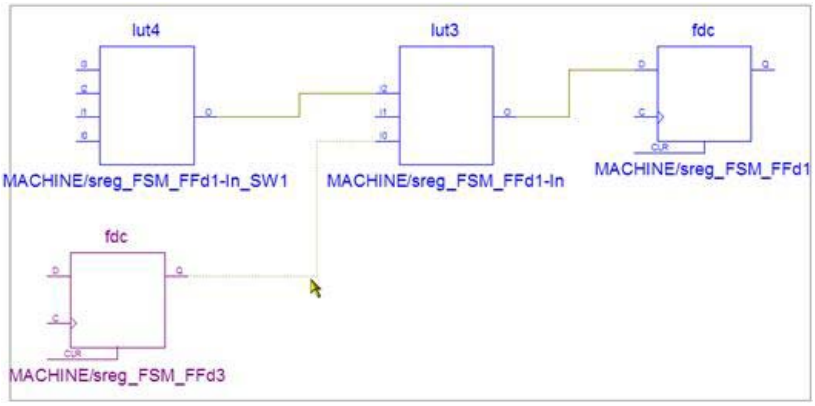

Figure 4-11: **Incremental Expansion**

A new **fdc** flip-flop was added to the schematic, but it is connected to the **I0** pin by a net in the form of a dashed line. The presence of a dashed line means that there are other objects connected to this net in your design, but they are not yet visible.

4. Continue to double-click the (dashed-line) net until it becomes a solid line, meaning that all elements connected to the net are now visible as shown in Figure 4-12.

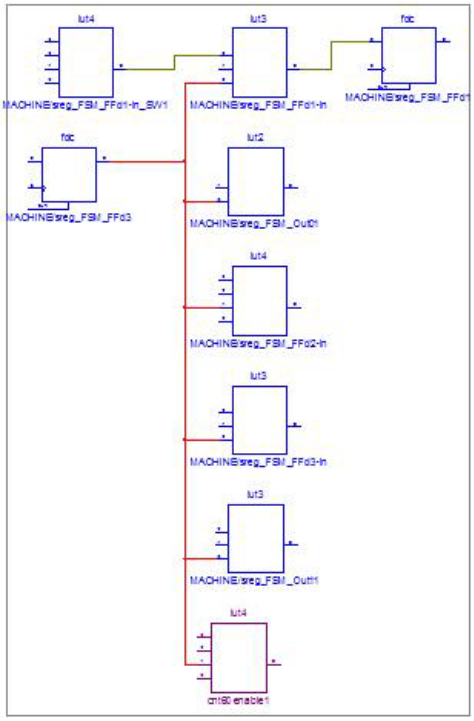

Figure 4-12: **Connecting the Net**

Step 7: Using Start and End Signal Markers

Start and End signal markers allow you to easily identify source and destinations of a selected signal.

1. To use this feature you have to first enable it using a button in the Schematic Viewer toolbar. This button has two states. The green state indicates the feature is enabled, and the red state indicates the feature is disabled. Push the button shown in Figure 4-13 to put it into the enabled state.

Figure 4-13: **Start and End Markers Button (Enabled)**

Figure 4-14: **Start and End Markers Button (Disabled)**

2. Select any signal on the schematic to see its source and destinations. See Figure 4-15.

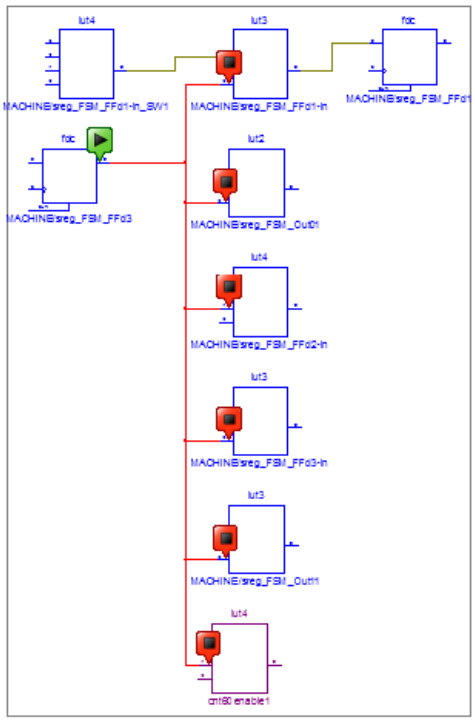

Figure 4-15: **Sources and Destinations**

Step 8: Navigating the History

The Previous Schematic button (or **Ctrl+Z**) provides the ability to return to previous schematic steps, and the Next Schematic button (or **Ctrl+Y**) provides the ability to move forward. For example, you can use the Previous Schematic button to return to a previous schematic step so you can continue design exploration in a different direction. See Figure 4-16 and Figure 4-17.

Figure 4-16: **Previous Schematic Button**

Figure 4-17: **Next Schematic Button**

1. Push the Previous Schematic button several times to get the following view, shown in Figure 4-18.

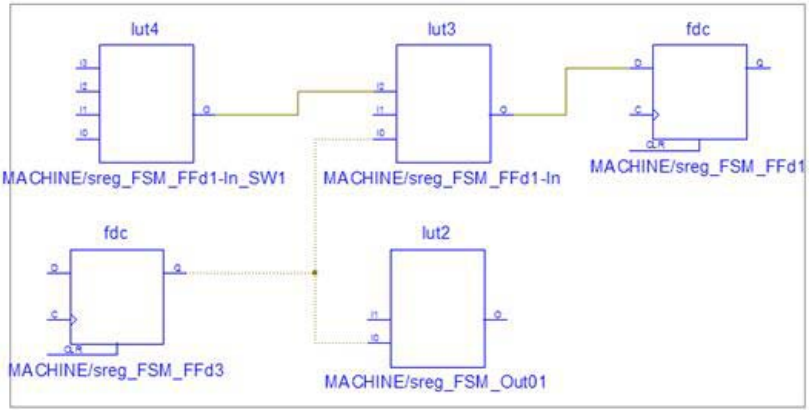

Figure 4-18: **Previous View**

2. Right-click the **lut2** primitive, and select **Show All Block Inputs/Outputs**. See Figure 4-19.

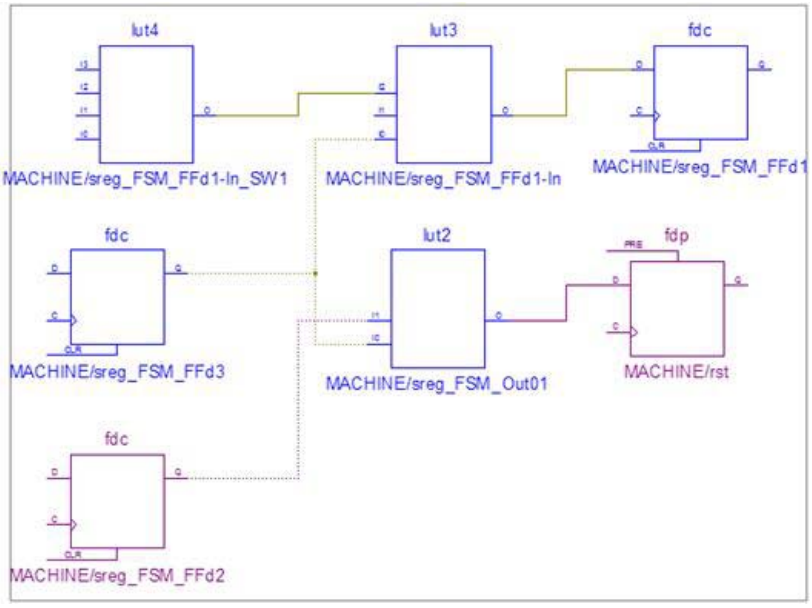

Figure 4-19: **Show All Block Inputs and Outputs**

Step 9: Removing Elements from the Schematic

During schematic expansion you may find that some previously added elements are not of interest for your particular design analysis. These elements can be selected and removed from the schematic. You can use **Delete** keyboard key, the Remove Selected Objects button from the toolbar as shown in Figure 4-20, or the **Edit > Delete** menu command.

Figure 4-20: **Remove Selected Objects Button**

To select a single element, just use a single click. To select multiple elements, you can select the first one and then incrementally add other ones by holding the **Ctrl** key and clicking them. Or, you can use in-box selection by holding down the **Ctrl** key and dragging over the objects you want to select.

1. Select the **lut4** and **lut3** primitives on the schematic.
2. Press the **Delete** keyboard key to remove them.

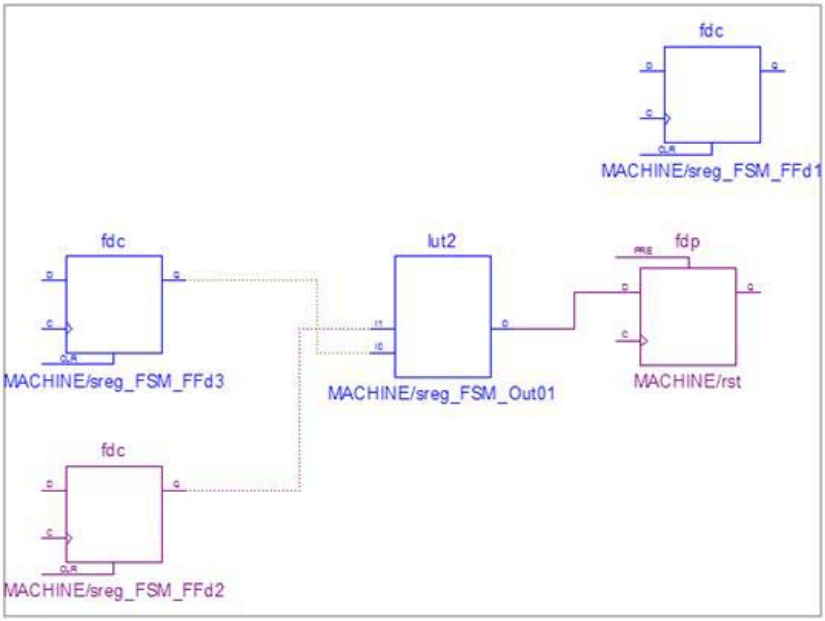

Figure 4-21: **Deleting Items**

Conclusion

In this lab you learned the basic operations available in the Schematic Viewer:

- Selecting Schematic Viewer startup mode
- Using the Explorer Wizard to select elements to start a schematic investigation
- Performing zoom operations based on mouse strokes
- Expanding schematics in different ways
- Coloring new elements
- Navigating history
- Using Start and End signal markers
- Removing elements from schematics

Lab 2: Working with Hierarchical Netlists

Objectives

The goal of this lab is to familiarize yourself with hierarchical netlists and to learn how you can manipulate hierarchical blocks during design analysis. This includes:

- Expanding external and internal hierarchical blocks
- Showing and hiding the entire contents of a hierarchical block

In addition, you will learn some special considerations you need to take into account when working with hierarchical blocks.

Finally, you will see how to start schematic exploration using the Starting schematic exploration with the top-level block startup mode introduced in Chapter 4, Lab 1: Basic Features.

Lab

Step 1: Creating the Lab Project

Create the stopwatch project and set the **Light Background Color Scheme** for Schematic Viewer as described in Chapter 3, Lab Preparation: Getting Started.

Step 2: Setting XST Options and Synthesizing the Design

1. In the Processes pane, right-click **Synthesize - XST**, and select **Process Properties** to open the Synthesis Options dialog box.
2. Set the Keep Hierarchy option to **Yes** as shown in Figure 5-1.

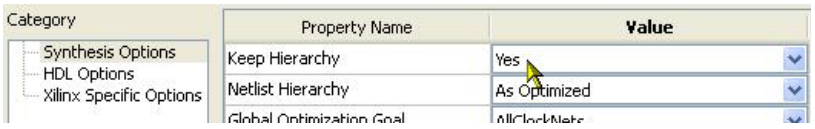

Figure 5-1: **Keep Hierarchy**

3. Synthesize the design using the **Synthesize - XST** process.

Step 3: Launching the Explorer Wizard

1. After synthesis is complete, start the Schematic Viewer by double-clicking the **View Technology Schematic** process, and select the **Start with the Explorer Wizard** startup mode.
2. In the Explorer Wizard, all hierarchical blocks (including the top-level block) are represented by the hierarchy symbol as shown in Figure 5-2. You can click the plus symbol in front of a hierarchical block to further expand its contents.

Figure 5-2: **Hierarchy Symbol**

3. Select the hierarchical block named **MACHINE**, move it to Selected Elements using the **Add** button, and click **Create Schematic**. See Figure 5-3.

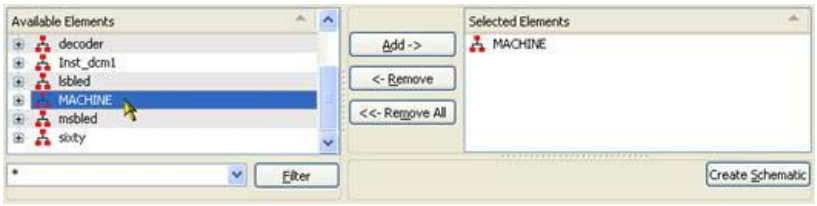

Figure 5-3: **Selecting Hierarchical Elements**

Step 4: Understanding Hierarchical Block Symbols

The created schematic appears as shown in Figure 5-4.

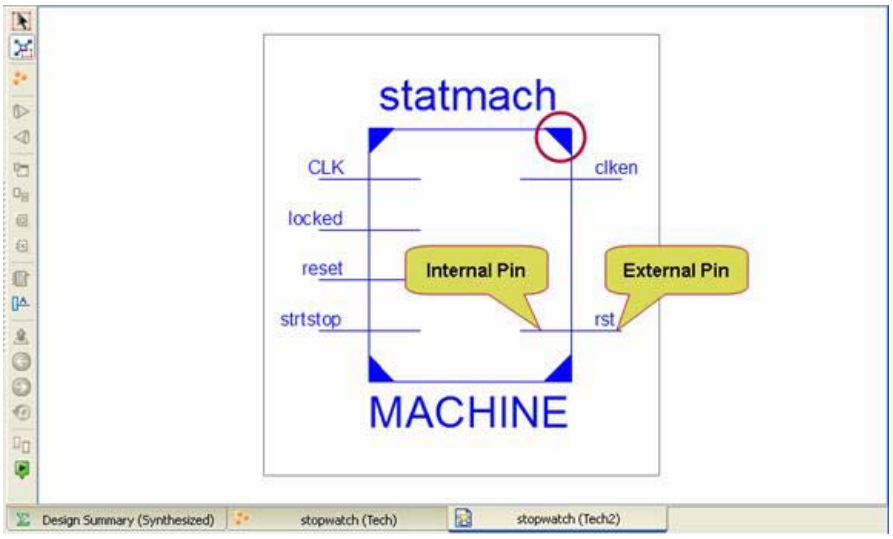

Figure 5-4: **Schematic Representation**

Two items distinguish a hierarchical block from a primitive:

- All hierarchical blocks have triangles in four symbol corners as shown in Figure 5-4 and Figure 5-5.
- In addition to external pins, hierarchical blocks also have internal pins. Internal pins allow you to explore the content of a hierarchical block while showing it on the same page.

Figure 5-5: **Triangle Symbol**

Expansion operations from the mouse right-click context menu (available for primitive pins and blocks) are available for internal and external pins and for the hierarchical block itself. In addition, you can use the incremental expansion approach (mouse double-click) on internal and external pins.

Step 5: Expanding Hierarchical Blocks

1. Double-click the internal and external **strstop** pin of the **MACHINE** block to get the following schematic (Figure 5-6).

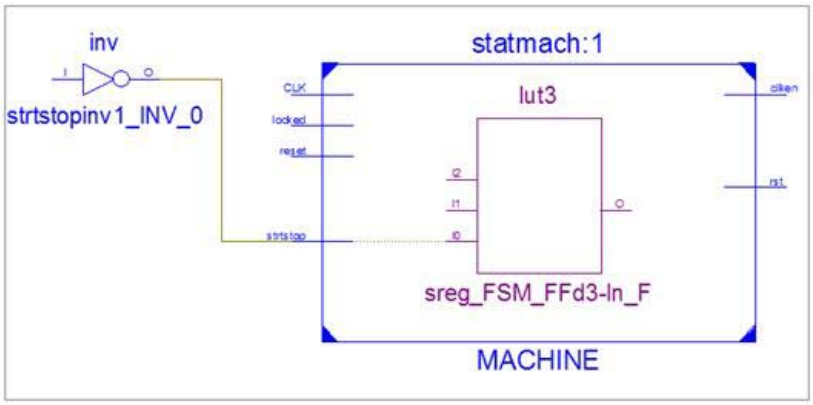

Figure 5-6: **MACHINE Block**

2. Right-click the **clken** external pin of the **MACHINE** block, and select the **Show Next Load (Input) Pin** option.

   The cnt60enable1 block appears as shown in Figure 5-7.

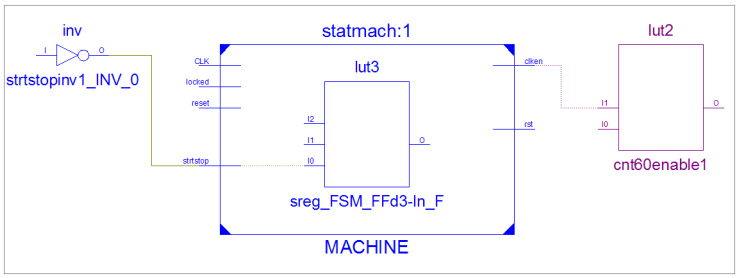

Figure 5-7: **Expanding Blocks**

Step 6: Showing and Hiding Block Contents

You can view the entire contents of the hierarchical block by using the Show Block Contents button (Figure 5-8) from the schematic toolbar or by using the right-click context menu. To hide its contents, use the Hide Block Contents button (Figure 5-9).

Figure 5-8: **Show Block Contents Button**

Figure 5-9: **Hide Block Contents Button**

1. Select the **MACHINE** block, and click the Show Block Contents button to see its entire contents as shown in Figure 5-10.

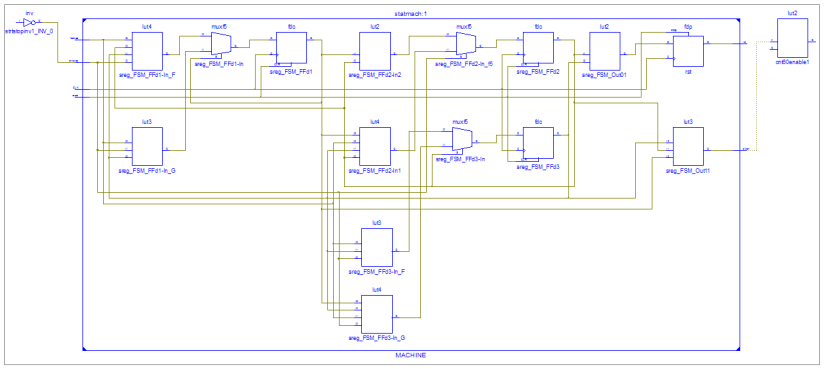

Figure 5-10: **View Block Contents**

2. Select the **MACHINE** block, and click the Hide Block Contents button to hide its entire contents as shown in Figure 5-11.

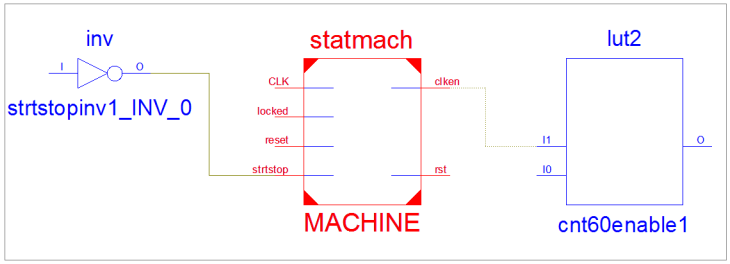

Figure 5-11: **Hide Block Contents**

Step 7: Using Bottom-Up Design Expansion

In the previous steps, you were mainly dealing with top-down schematic expansion. Now we will use the Schematic Viewer in a "bottom-up" mode.

1. Select the following two tabs (Figure 5-12), and close them using the close window button (Figure 5-13).

Figure 5-12: **Tabs to Close**

Figure 5-13: **Close Window Button**

2. Restart the Schematic Viewer by double-clicking the **View Technology Schematic** process, and select the **Start with the Explorer Wizard** startup mode.
3. Expand the **MACHINE** hierarchical block, expand **Primitives**, select **sreg_FSM_FFd3-In_F** and add it to the Selected Elements using the **Add** button, and click **Create Schematic**. See Figure 5-14.

Figure 5-14: **Restarting Schematic Viewer**

4. Right-click **sreg_FSM_FFd3-In_F**, and select **Show All Block Inputs**.
5. Comparing the start-up schematic (Figure 5-15) with the one we obtained at Step 6: Showing and Hiding Block Contents (Figure 5-16), you see that the **sreg_FSM_FFd3-In_F** primitive is not placed inside the **MACHINE** hierarchy block. In addition, **MACHINE** I/Os are represented as primary design pins.

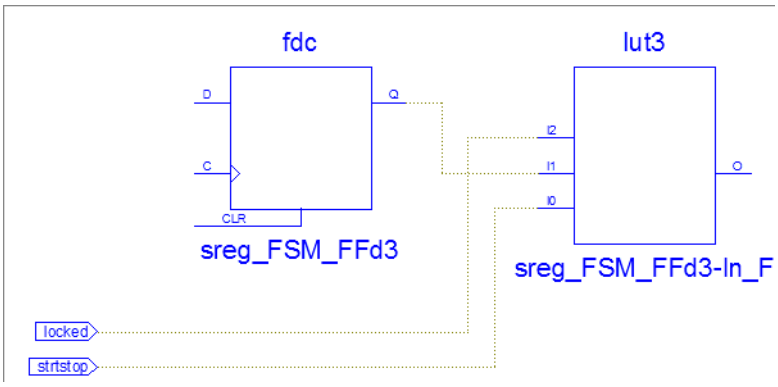

Figure 5-15: **Start-Up Schematic**

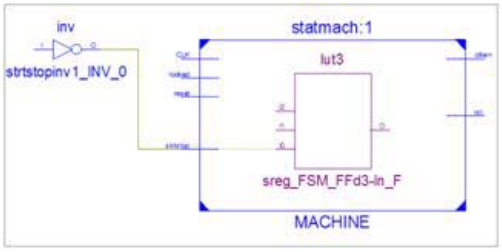

Figure 5-16: **Step Schematic**

6. Further incremental design exploration shows that schematic expansion stops at **MACHINE** hierarchy boundaries as shown in Figure 5-17.

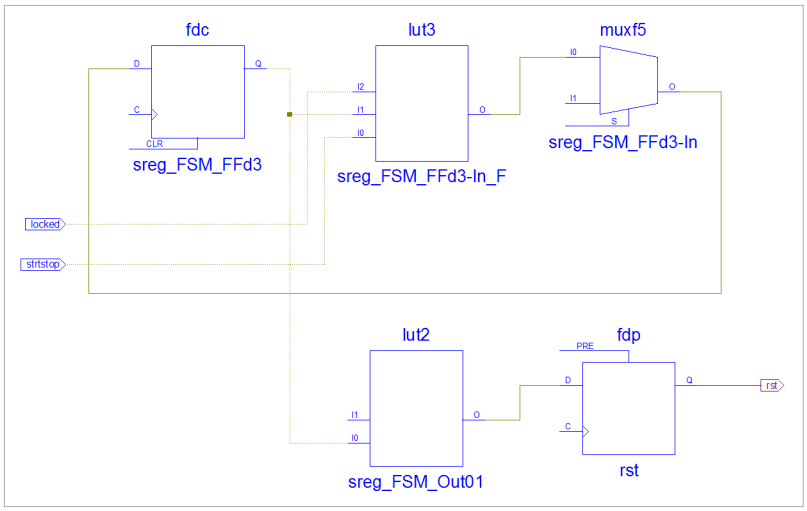

Figure 5-17: **Hierarchical Boundaries**

To cross hierarchy in a bottom-up direction, use the Pop button to pop to the calling schematic (Figure 5-18):

Figure 5-18: **Pop Button**

7. Press the Pop button to cross hierarchy in a bottom-up direction as shown in Figure 5-19.

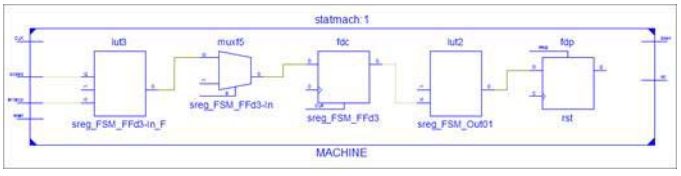

Figure 5-19: **Upper Hierarchical Level**

You can now continue further schematic exploration inside as well as outside the MACHINE block. Use the Pop button each time you need to go to the upper hierarchy level.

Step 8: Starting Schematic Exploration with the Top-Level Block

In Chapter 4, Lab 1: Basic Features, we introduced two modes to start schematic exploration:

- Start with the Explorer Wizard
- Start with a schematic of the top-level block

Until now, we exclusively used the first mode. Now we will learn how to use the second mode.

1. Close all currently opened schematic tabs using the close window button.
2. Restart the Schematic Viewer by double-clicking the **View Technology Schematic** process.
3. Select the **Start with a schematic of the top-level block** startup mode, and click the **OK** button as shown in Figure 5-20:

Figure 5-20: **Startup Modes**

The following startup schematic appears, as shown in Figure 5-21.

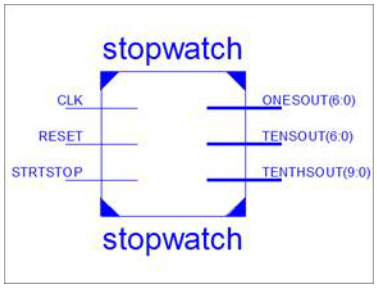

Figure 5-21: **Top-Level Block**

4. You can start design exploration by using all previously described schematic expansion methods.

Conclusion

In this lab, you learned how to use the Schematic Viewer on a design with hierarchical blocks. This included learning how the blocks are represented in the Explorer Wizard and how they can be expanded for design analysis.

In addition, you learned how to start schematic exploration using the **Starting schematic exploration with the top-level block** startup mode introduced in Chapter 4, Lab 1: Basic Features.

Lab 3: Using Schematic Viewer for Timing Analysis

Objectives

Critical timing paths from the post-place and route timing report can be easily visualized in the Schematic Viewer by cross probing from the Timing Report to the Schematic Viewer. The visualized critical path can be used as a starting point for further design exploration. Moreover, it is easy to annotate the critical path with timing delays.

The goal of this lab is to demonstrate how to cross probe from the timing report to the Schematic Viewer and how to annotate the visualized timing path with reported delays.

Lab

Step 1: Creating the Lab Project

Create the stopwatch project and set the **Light Background Color Scheme** for Schematic Viewer as described in the Chapter 3, Lab Preparation: Getting Started.

Step 2: Specifying Timing Constraints

To use the cross probing mechanism, add a new UCF file called `stopwatch.ucf` to the project. Then, using Constraints Editor, specify a period constraint of 3.5 ns for the CLK signal as shown in Figure 6-1.

Figure 6-1: **Clock Signal Definition**

Step 3: Specifying XST Options and Implementing the Design

1. In the Processes pane, right-click **Synthesize - XST**, and select **Process Properties** to open the Synthesis Options dialog box.

2. Set the Keep Hierarchy option to **Yes** as shown in Figure 6-2.

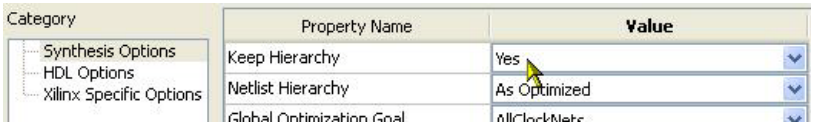

Figure 6-2: **Keep Hierarchy**

3. Implement the design by double-clicking the **Place & Route** process in the Processes pane.
4. Open Timing Analyzer for the post-place and route design, as shown in Figure 6-3.

Figure 6-3: **Analyze Post-Place & Route Static Timing**

Step 4: Viewing the Critical Path in the Schematic Viewer

In the timing Report Navigation section, select the critical path to access the detailed data path information. The detailed path view allows you to cross probe (from the mouse right-click context menu) to different views, for example, FPGA Editor or a Datasheet view.

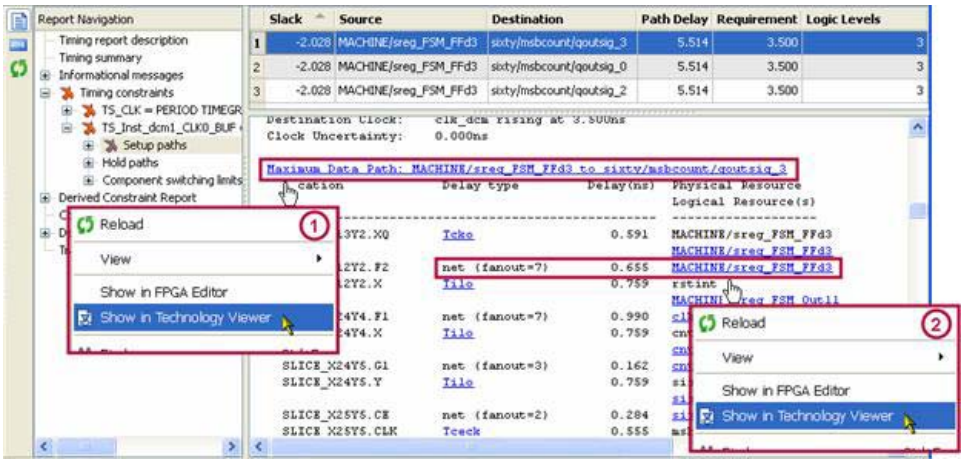

Figure 6-4: **Report Navigation**

In this lab, we will focus on the links dedicated to Schematic Viewer only (Figure 6-4):

- Selecting (1) the Maximum Data Path enables you to visualize the entire data path.
- Selecting (2) a net from the Physical Resource column enables you to visualize just a portion of a data path connected by a selected net.

1. Right-click **Maximum Data Path**, and select **Show in Technology Viewer.** This draws the selected data path in the Schematic Viewer as shown in Figure 6-5.

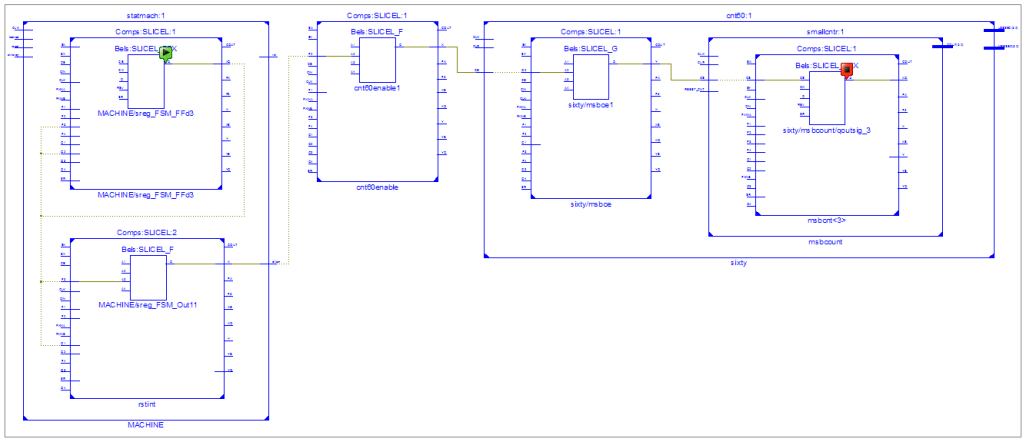

Figure 6-5: **Schematic Viewer**

2. Observe the following:
   - The start point of the critical path is marked with a start icon (Figure 6-6).

Figure 6-6: **Start Icon**

   - Slices are represented as hierarchical blocks. This means that you can explore their internal contents using internal pins as well as their external connections.
   - You can use *all* available features (described in earlier labs) to further explore the schematic.

Step 5: Annotating the Schematic with Timing Delays

Delays from detailed path report (Figure 6-7) can be directly visualized on a schematic.

```
Maximum Data Path: MACHINE/sreg_FSM_FFd3 to sixty/msbcount/qoutsig_0
  Location             Delay type          Delay(ns)  Physical Resource
                                                      Logical Resource(s)
  -------------------------------------------------    --------------------
  SLICE_X13Y2.XQ       Tcko                  0.591    MACHINE/sreg_FSM_FFd3
                                                      MACHINE/sreg_FSM_FFd3
  SLICE_X12Y2.F2       net (fanout=7)        0.655    MACHINE/sreg_FSM_FFd3
  SLICE_X12Y2.X        Tilo                  0.759    rstint
                                                      MACHINE/sreg_FSM_Out11
  SLICE_X24Y4.F1       net (fanout=7)        0.990    clkenable
  SLICE_X24Y4.X        Tilo                  0.759    cnt60enable
```

Figure 6-7: **Path Report**

1. Select the schematic sheet with the visualized data path.
2. Click the Select Block Pin Annotation button (Figure 6-8) from the Schematic Viewer toolbar.

Figure 6-8: **Select Block Pin Annotation Button**

3. In the following dialog box, check the **Delay Values** option. Check the **Pin Names** option as shown in Figure 6-9.

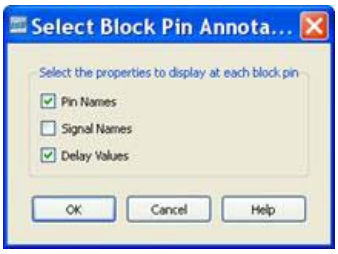

Figure 6-9: **Select Block Pin Annotation Button**

A schematic view of the data path annotated with timing delays appears, as shown in Figure 6-10.

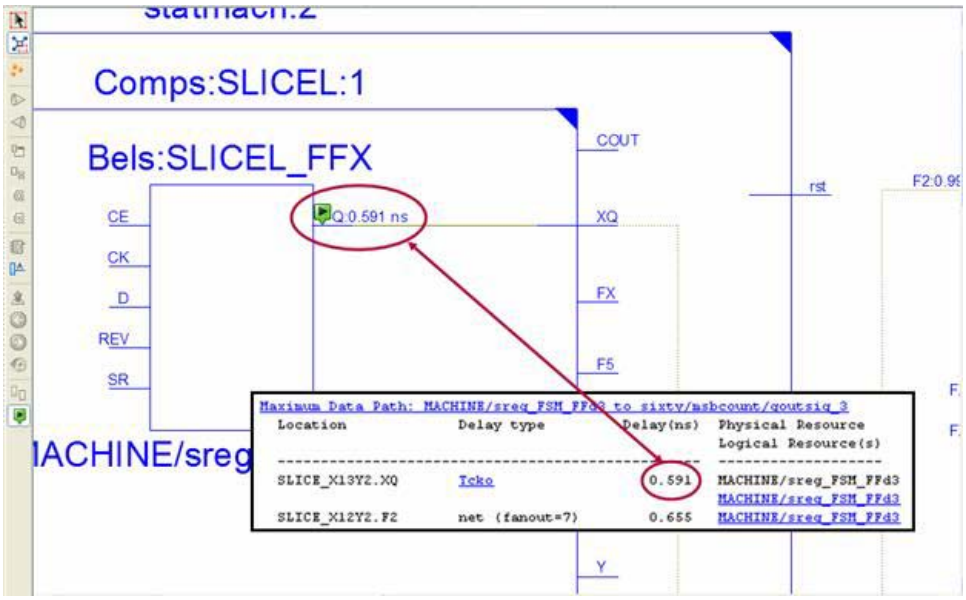

Figure 6-10: **Data Path Annotated with Timing Delays**

Conclusion

In this lab, you learned how the Schematic Viewer can be used to help visualize key information during timing analysis. You were able to select critical timing paths from the timing report, and graphically visualize them in the Schematic Viewer. Finally, you annotated the critical path in the Schematic Viewer with timing delays from the timing report.

Lab 4: Simplifying Design Analysis

Objectives

Very often, during design exploration, you must deal with a significant number of elements incrementally added to the schematic sheet. The sheer number of elements on the schematic can complicate the design analysis process.

The goal of this lab is to show you several methods to reduce design complexity and make the analysis process more efficient. These methods include capabilities to:

- Use Start and End Signal markers to quickly identify source and destinations of selected signals
- Remove elements that are not of interest from the schematic sheet
- Work with multiple schematics of the same netlist
- Start a new schematic by selecting a subset of elements from the current design view
- Use colors to highlight a specific design instance or a group of similar elements

The first two methods were already described in Chapter 4, Lab 1: Basic Features; therefore, the main focus is the last three features.

Lab

Step 1: Creating the Lab Project

Create the stopwatch project and set the **Light Background Color Scheme** for Schematic Viewer as described in Chapter 3, Lab Preparation: Getting Started.

Step 2: Setting XST Options and Synthesizing the Design

1. In the Processes pane, right-click **Synthesize - XST**, and select **Process Properties** to open the Synthesis Options dialog box.
2. Set the Keep Hierarchy option to **No** as shown in Figure 7-1.

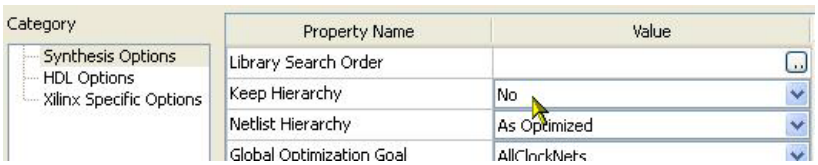

Figure 7-1: **Keep Hierarchy Option**

3. Synthesize the design using the **Synthesize - XST** process.

Step 3: Working with Multiple Schematics of the Same Netlist

To demonstrate this feature, we will select a flip-flop and analyze its input and output logic cones. To simplify schematic complexity, you will place the input logic cone on one sheet and the output logic cone on another sheet.

1. After synthesis is complete, start the Schematic Viewer by launching the **View Technology Schematic** process, and select the **Start with the Explorer Wizard** startup mode.
2. Expand **Primitives**, select the **MACHINE/sreg_FSM-FFd1** flip-flop and add it to the Selected Elements using the **Add** button, and click **Create Schematic**.
3. Right-click the visualized flip-flop, and select **Add Input Cone**.

   The input appears as shown in Figure 7-2.

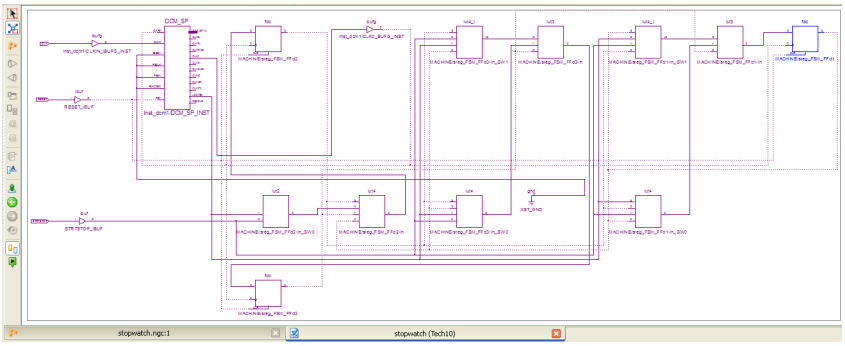

Figure 7-2: **Adding Input**

4. Click the **Stopwatch.ngc** tab to return to the Explorer Wizard. Select **Create Schematic** to open a new schematic tab. Select the visualized flip-flop, and select **Add Output Cone** from the right-click context menu.

The output appears as shown in Figure 7-3.

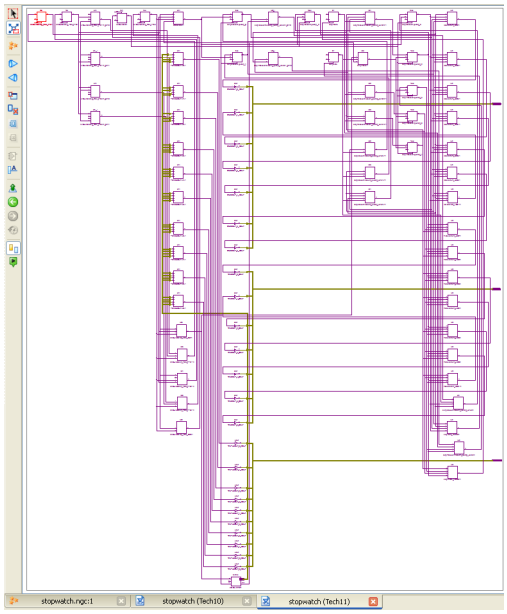

Figure 7-3: **Adding Output**

Observe that you were able to reduce complexity of the design view by dividing it into two pieces. The capability to visualize multiple schematics can be used for many different purposes. One of them is discussed in Chapter 8, Lab 5: Comparing Two Design Implementations, where you will see how to use this feature and to compare two different netlists of the same design.

Step 4: Starting a New Schematic by Selecting Elements from the Current View

Suppose during design debugging you are able to localize the source of a problem and would like to focus just on that limited portion of the design. However, the drawn schematic might have many other elements that are not of direct interest and clutter the view.

Of course, as described earlier, you can try to select those objects you are not interested in and remove them. Another way to accomplish this is to return to the Explorer Wizard and start a new schematic by selecting required elements. Depending on your particular design, these methods can be tedious and time-consuming.

Often, the best way to handle this is to directly select the required elements from the current view and start a new schematic by pushing the New Schematic with Selected Objects button (Figure 7-4) from the schematic toolbar.

Figure 7-4: **New Schematic with Selected Objects Button**

Note: In this case, the Schematic Viewer does not create a new schematic sheet. It places the new schematic on the same sheet.

1. Select the **Stopwatch (Tech1)** tab on the schematic.
2. On this sheet, select elements surrounded by the rectangle as shown in Figure 7-5.

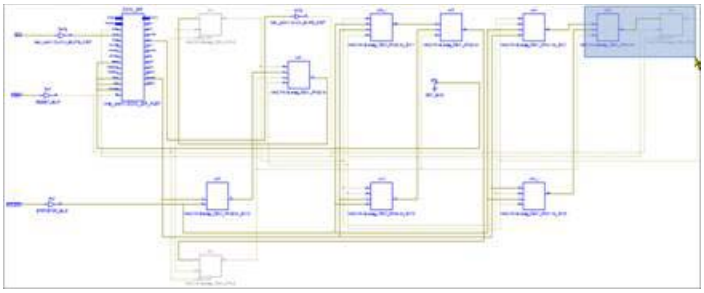

Figure 7-5: **Stopwatch (Tech1) Schematic**

3. Click the New Schematic with Selected Objects button to start a new schematic. The new schematic appears as shown in Figure 7-6. You can continue to further expand as described in earlier lab segments.

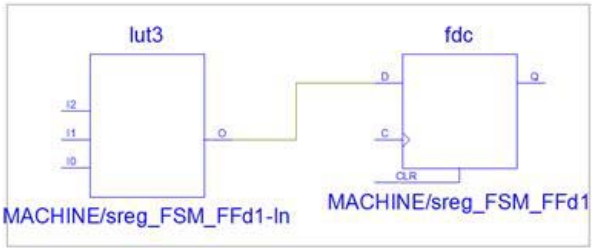

Figure 7-6: **New Schematic**

Step 5: Using Colors to Highlight a Group of Specific Elements

Select the **Stopwatch (Tech2)** tab on the schematic. The schematic appears as shown in Figure 7-7.

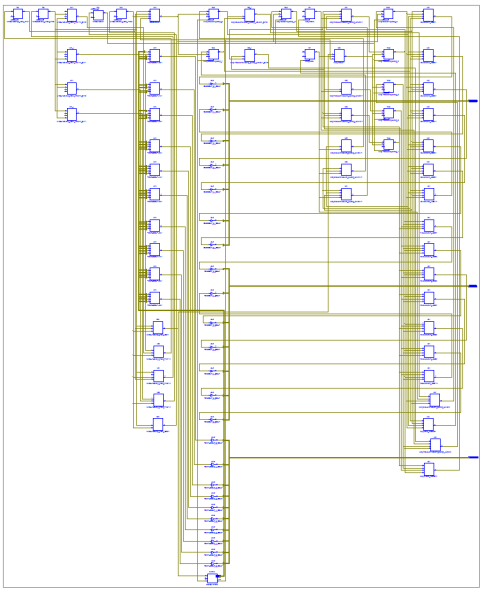

Figure 7-7: **Stopwatch (Tech2)**

You can see many elements in this view. We will highlight all **fd*** type flip-flops using a different color as a means to simplify analysis.

1. Open the Preference dialog box by selecting **Edit > Preferences**.
2. Under the RTL/Technology Viewers category, select the **User Color Rules** sub-category as shown in Figure 7-8. This is where we can define specific color rules for our needs.

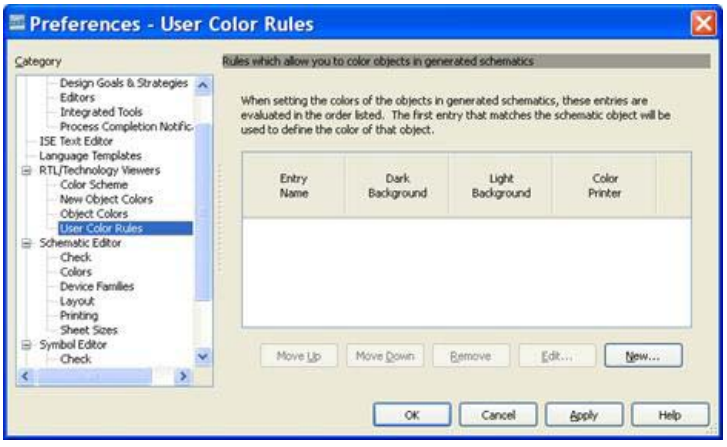

Figure 7-8: **Preferences Dialog Box**

3. Click the **New** button to open the Color Rules dialog box.

4. Specify **fd_ff_colors** as a name for the color rule. Then click the **New** button to add a new rule.

Figure 7-9: **Color Rules Dialog Box**

5. Select **Block Type** for Property Name, select **Matches (Wildcard)** as Operator, type **fd*** as a value as shown in Figure 7-9, and click **OK**.
6. In the Light Background column, select **Gray** as the color (see Figure 7-10) for fd_ff_colors, and click **OK**.

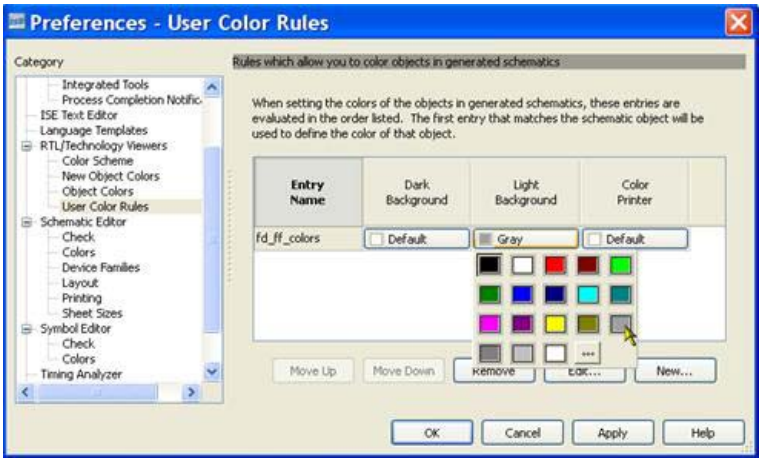

Figure 7-10: **Selecting Light Background Gray**

Now all flip-flops are colored differently (gray), which allows to you to easily recognize them on the schematic sheet as shown in Figure 7-11.

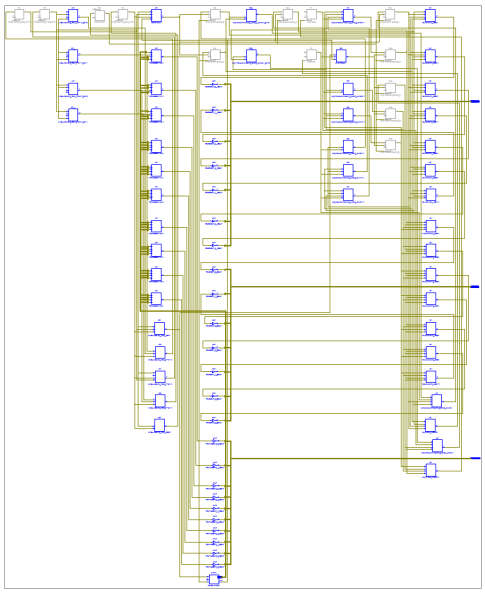

Figure 7-11: **Colored Items**

When you expand the schematic by adding new elements with particular colors defined in the Color Rules (as we did for **fd*** flip-flops), specific colors may be not be visible, because they are overwritten by New Object Colors. To see specific colors, disable New Objects Coloring using the Colorize New Objects button (Figure 7-12).

Figure 7-12: **Colorize New Objects Button**

Conclusion

In this lab you worked with several methods that allowed you to simplify the design analysis process:

- Creating multiple schematics of the same netlist
- Starting a new schematic by selecting some elements from the current design view
- Using Color Rules to color all fd type flip-flops in a particular color to easily recognize them on the schematic sheet

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Chapter 8

Lab 5: Comparing Two Design Implementations

Objectives

To meet design requirements (such as speed, area, and power requirements), you may need to modify the original HDL sources or change synthesis and implementation options. Performing such changes sometimes requires you to understand the impact of these changes in the final implementation.

The Schematic Viewer can help you in these situations, because it allows you to visualize and compare different design netlists. Please note that this can be done for the XST RTL view and post-synthesis netlists. Post-map and post-place and route netlists are not handled in this mode.

The goal of this lab is to show you how to create two design implementations with XST and visualize them in the Schematic Viewer.

Lab

Step 1: Creating a Lab Project

Create the stopwatch project and set the **Light Background Color Scheme** for Schematic Viewer as described in Chapter 3, Lab Preparation: Getting Started.

Step 2: Setting XST Options and Synthesizing the Design

1. In the Processes pane, right-click **Synthesize - XST**, and select **Process Properties** to open the Synthesis Options dialog box.
2. Set the Keep Hierarchy option to **Yes** as shown in Figure 8-1.

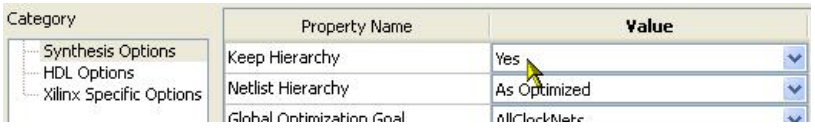

Figure 8-1: **Selecting Keep Hierarchy**

3. Synthesize the design using the **Synthesize - XST** process.
4. Open a shell prompt, go to the project directory, and copy `stopwatch.ngc` file to `default_run.ngc`.

5. In the Processes pane, right-click **Synthesize - XST**, and select **Process Properties** to open the Xilinx Specific Options dialog box.
6. Set the **Register Balancing** option to **Yes** (see Figure 8-2).

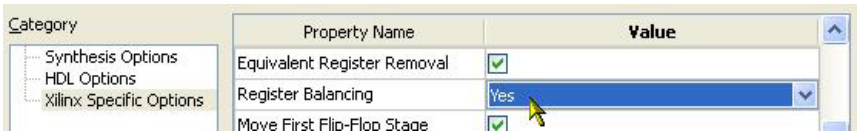

Figure 8-2: **Select Register Balancing**

7. Re-run the **Synthesize - XST** process.
8. During the Synthesis process, with **Register Balancing** enabled, XST reports that several FFs were moved forward:

```
Register(s) sreg_FSM_FFd3 sreg_FSM_FFd1 sreg_FSM_FFd2 has(ve) been
forward balanced into : sreg_FSM_Out11_FRB.
```

Take a look at how this is reflected in the Schematic View.

Step 3: Loading and Comparing Two Netlists

1. Open the Technology Viewer by using the **View Technology Schematic** process for the latest generated netlist in the **Start with the Explorer Wizard** mode. Select the hierarchical block icon (see Figure 8-3) and create the schematic.

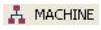

Figure 8-3: **Hierarchical Block Icon**

2. Open the previously stored `default_run.ngc` netlist by selecting **File > Open**. Select the **Start with the Explorer Wizard** mode. Project Navigator loads the netlist and starts the Schematic Viewer Wizard. Using the wizard, select the **MACHINE** hierarchical block icon (Figure 8-3) and create the schematic.
3. Simultaneously view the two schematics sheets horizontally using the Tile Windows Horizontally button (Figure 8-4) from the general toolbar. To expand the view, double-click the inside pins of the **RST** and **CLKEN** pins. The display appears as shown in Figure 8-5.

Figure 8-4: **Tile Windows Horizontally Button**

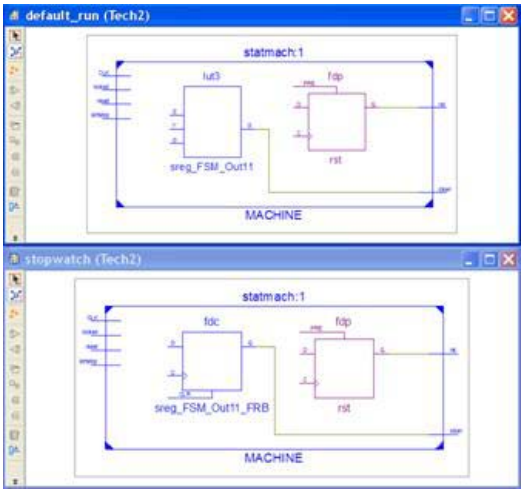

Figure 8-5: **Dual View of Schematic**

4. The bottom netlist was generated using the Register Balancing mechanism. Note how XST moved forward several FFs (creating **sreg_FSM_Out11_FRB**) towards the output of **clken** pin to improve design performance.

Conclusion

In this lab you visualized and compared two netlists for the same design, where each was generated using different XST options.

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Chapter 9

Lab 6: Dealing with Large Designs

Objectives

The latest FPGA families from Xilinx® allow you to implement ever larger and more complex designs, which can significantly complicate the analysis process. For the largest of designs, having *hundreds of thousands* of design elements is entirely possible. Visualizing the entire design on a single page is not practical.

This lab provides several tips on how you can deal with complex designs while keeping good visibility and preserving good responsiveness using the Schematic Viewer.

Tip 1: Using Hierarchical Netlists

The presence of hierarchy in the post-synthesis netlist significantly reduces its complexity for design analysis process as well as for the Schematic Viewer. Please note that the XST RTL netlist is fully hierarchical.

Preserving Hierarchy

XST enables you to either fully or partially preserve design hierarchy. However, hierarchical preservation prevents logic optimization across hierarchical boundaries of preserved blocks. As a consequence, this may negatively impact design performance.

Therefore, when using hierarchical preservation during synthesis, you have to ensure that you still meet design goals.

Rebuilding Hierarchy

Another way to generate a hierarchical netlist without a design performance impact is to use the Netlist Hierarchy option. If the value of this option is set to Rebuilt (as shown in Figure 9-1), XST automatically reconstructs the hierarchy of the final netlist even if it was fully flattened during optimization.

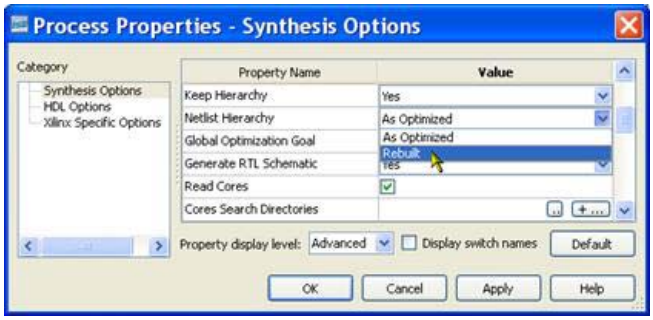

Figure 9-1: **Rebuilt Option**

This feature is not set by default, because it may increase XST synthesis runtime and could affect the accuracy of area estimation reports.

We suggest you run tests of this option on your current design to ensure that synthesis runtime is acceptable.

Tip 2: Using Multiple Schematic Sheets

Even if the hierarchy of your design is fully reconstructed, a single hierarchy level may still contain thousands of elements, complicating visualization and analysis.

If you need to deal with a significant number of elements, we suggest you take advantage of the capability to visualize the same netlist on multiple schematic sheets as shown in Figure 9-2. As you have seen in earlier labs, this process can be fully controlled and adapted for your specific needs.

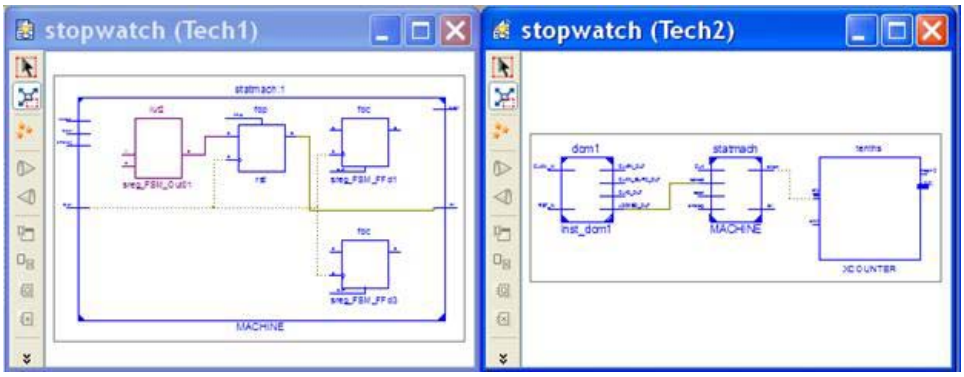

Figure 9-2: **Multiple Schematic Sheets**

Please refer to Chapter 7, Lab 4: Simplifying Design Analysis for more information.

Conclusion

In this lab you have seen an overview of methods you can use to handle large designs. The first method consists of ways to generate hierarchical netlists. The second method suggests using multiple schematic sheets to reduce the number of elements you need to visualize at any one time.

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Chapter 10

Lab 7: Using the Schematic Viewer as a Standalone Tool

Objectives

Command line users often need to run point tools, such as FPGA Editor or Schematic Viewer, for design analysis.

In the ISE® Design Suite, you cannot launch Schematic Viewer in a "standalone" mode. However, there is a workaround for this limitation, which allows you to explore the XST RTL View or XST post-synthesis netlists. Post-map and post-place and route netlists are not handled in this mode.

The goal of this lab is to demonstrate how the Schematic Viewer can be used to emulate a standalone tool to view XST RTL and post-synthesis netlists.

Use Table 10-1 to localize the required netlist.

Table 10-1: **Netlist File Extensions**

Netlist	Extension
XST RTL	.ngc
XST post-synthesis	.ngr

Lab

Step 1: Creating the Lab Project

Create the stopwatch project and set the **Light Background Color Scheme** for Schematic Viewer as described in Chapter 3, Lab Preparation: Getting Started.

Step 2: Setting XST Options and Synthesizing the Design

1. In the Processes pane, right-click **Synthesize - XST**, and select **Process Properties** to open the Synthesis Options dialog box.
2. Set the Keep Hierarchy option to **Yes** as shown in Figure 10-1.

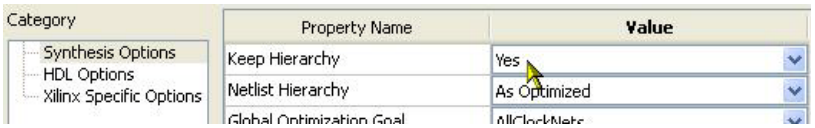

Figure 10-1: **Keep Hierarchy**

3. Synthesize the design using the **Synthesize - XST** process.
4. After synthesis is complete, close the project by selecting **File > Close Project**. Note that Project Navigator remains open.

Step 3: Opening the Post-Synthesis Netlist in Schematic Viewer

1. The post-synthesis XST `stopwatch.ngc` netlist is located in the project directory (the `.ngc` file can be generated from command line mode). To open this netlist in Schematic Viewer, select **File > Open**.
2. Select the **Start with the Explorer Wizard** startup mode. Project Navigator loads the netlist and starts the Schematic Viewer Wizard as shown in Figure 10-2. Now you can move on and explore your design.

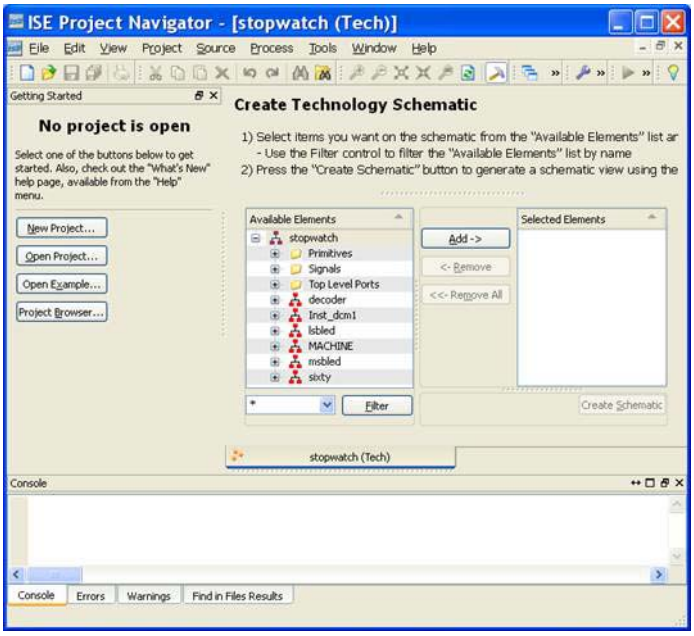

Figure 10-2: **Schematic Viewer Wizard**

Conclusion

This lab demonstrated how the Schematic Viewer can be used by command line users in a "standalone" mode. You can open any post-synthesis XST netlist in the Schematic Viewer without first opening a project.

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Appendix A

Additional Resources

Xilinx Resources

- ***Xilinx Design Tools: Installation and Licensing Guide*** *(UG798)*: http://www.xilinx.com/support/documentation/sw_manuals/xilinx14_1/iil.pdf
- ***Xilinx Design Tools: Release Notes Guide*** *(UG631)*: http://www.xilinx.com/support/documentation/sw_manuals/xilinx14_1/irn.pdf
- **Product Support and Documentation**: http://www.xilinx.com/support
- **Xilinx Glossary**: http://www.xilinx.com/company/terms.htm