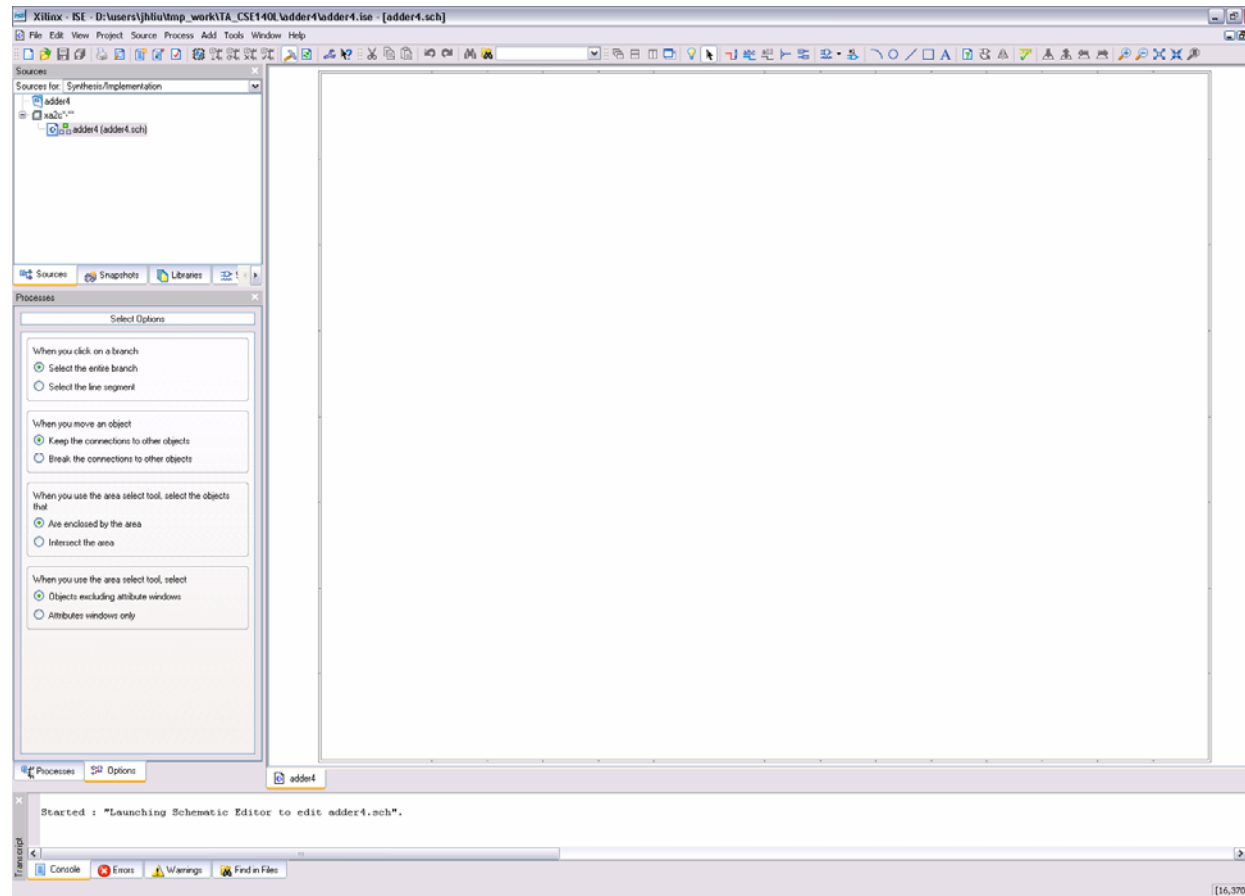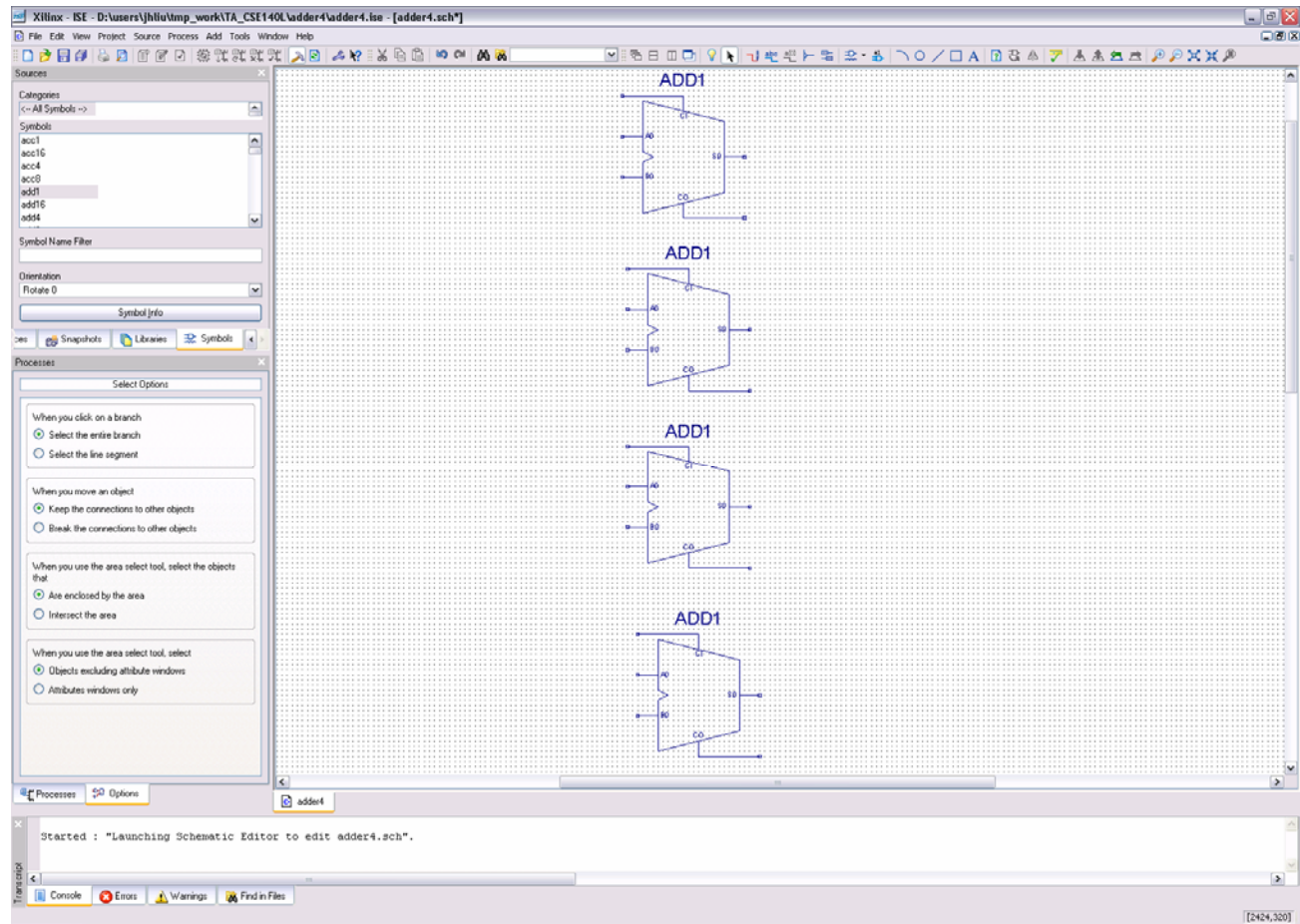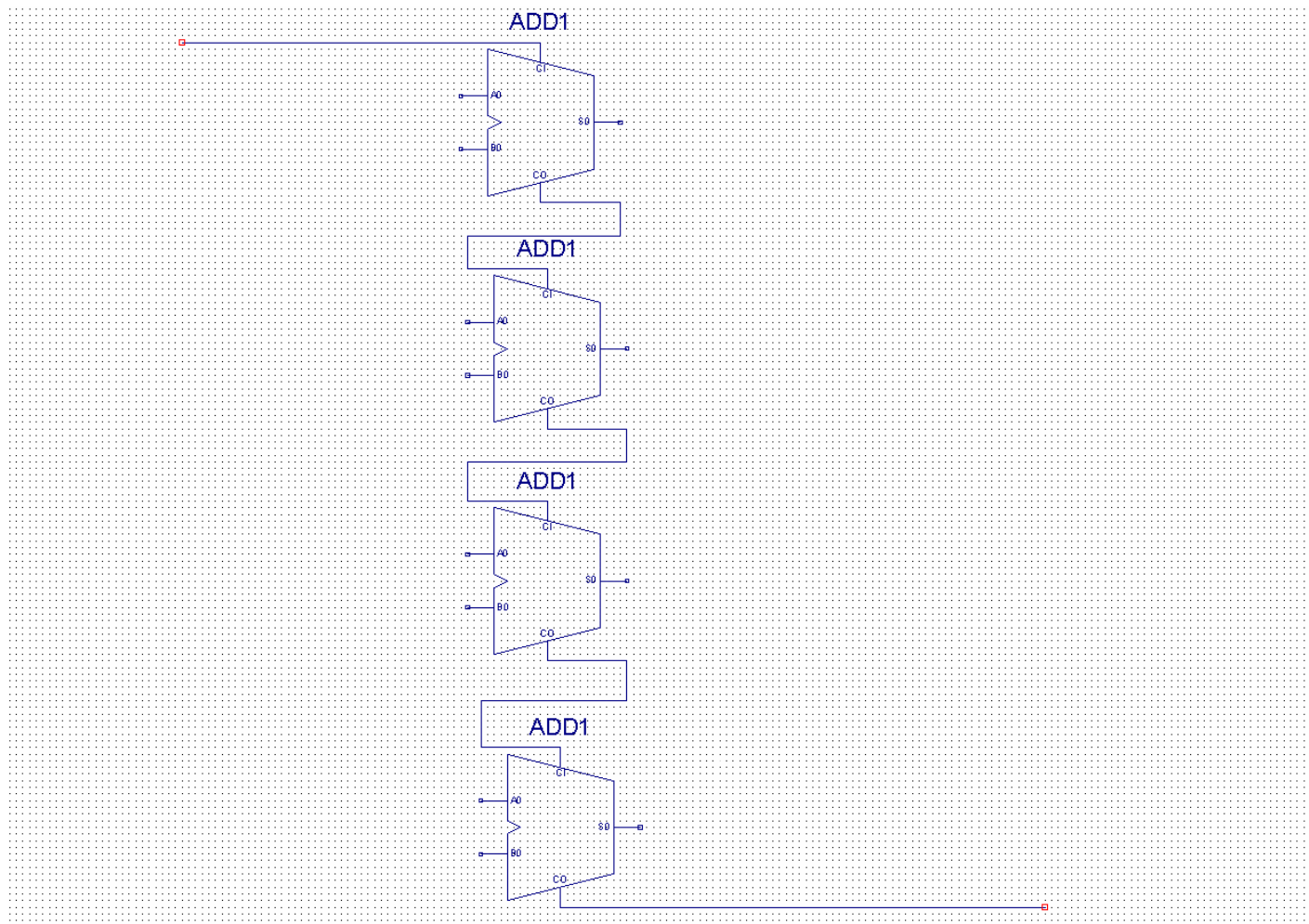# A Tutorial on Using Bus in Xilinx ISE


In this Tutorial, we will design a 4-bit adder with bus. First create a project "adder4" and add an empty schematic design file "adder4.sch" to the project.
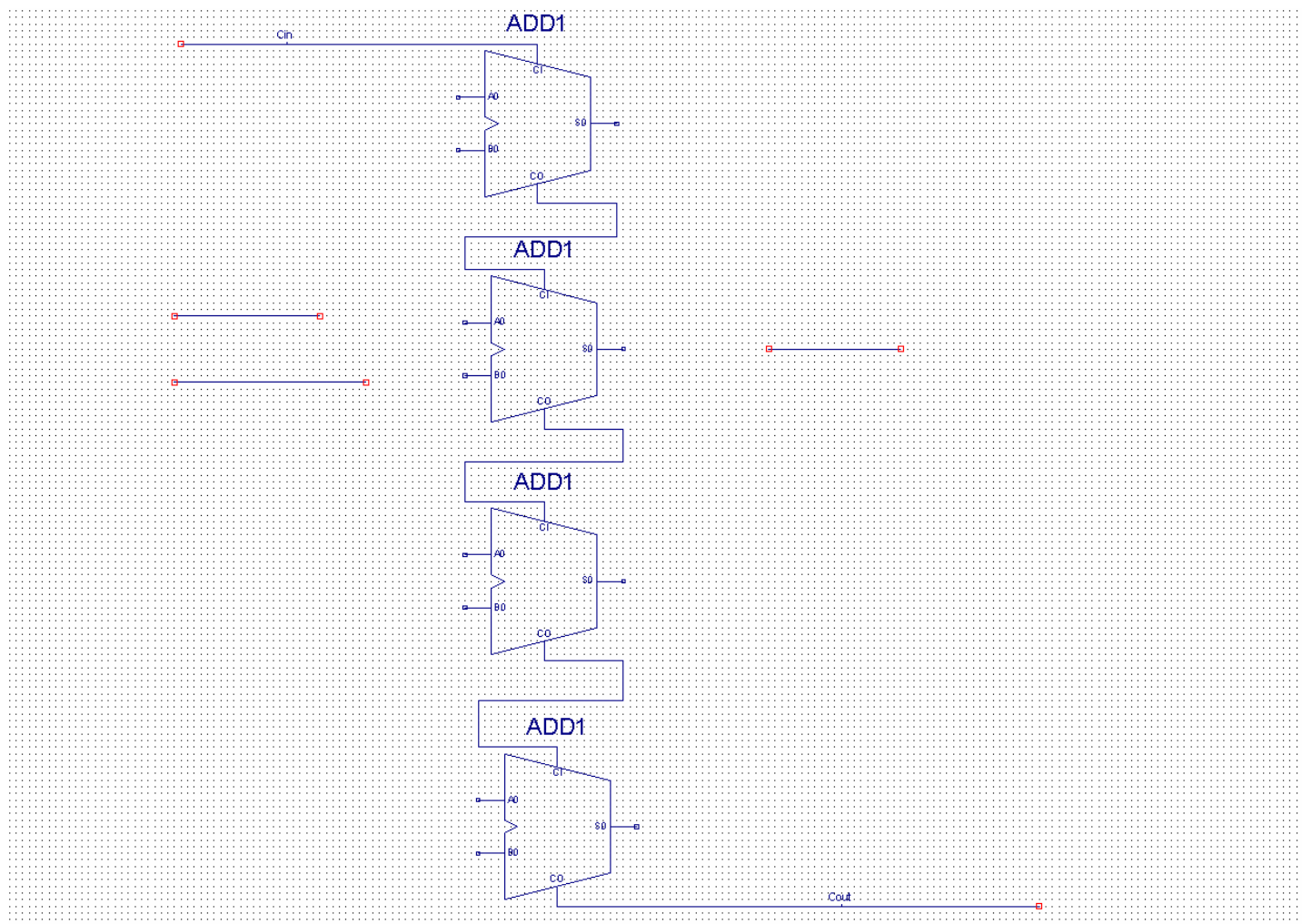
Click on on the tool bar, and select "add1" from "Symbols" window on the left. Place four "ADD1" on the canvas.

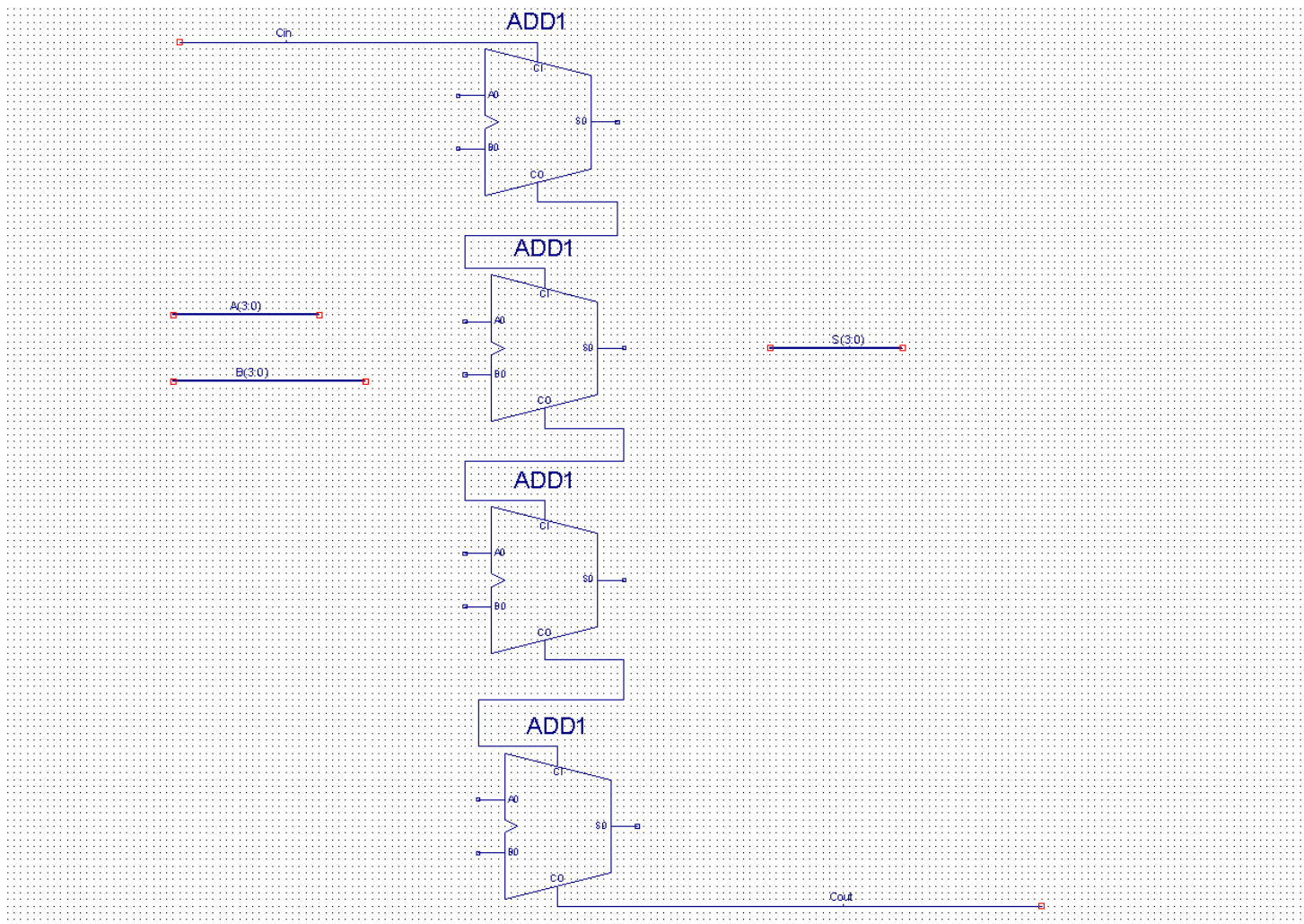Use wire tool ⌐ᵈ to connect each CO port to the next CI port with single wire. And draw single wires to the first CI input and the last CO output.
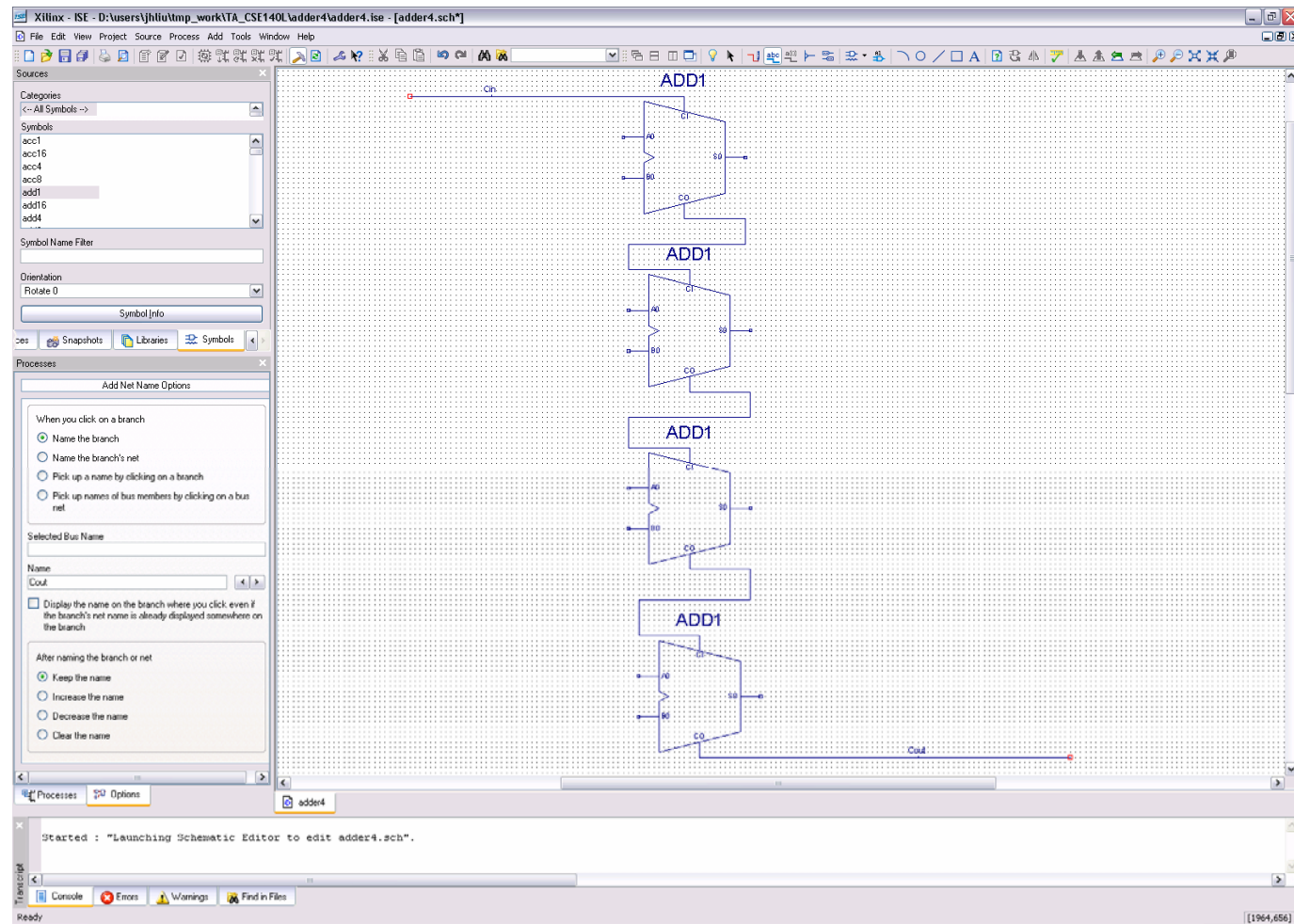
Click on the tool bar, and input "Cin" to the Name field in the Options windows on the left. Click on the top input wire to name it as "Cin". And name the bottom output wire as "Cout". Note that you may need to scroll down in option-window to see all available options.

ADD1

Cin

CI

A0

S0

B0

CO

ADD1

CI

A0

S0

B0

CO

ADD1

CI

A0

S0

B0

CO

ADD1

CI

A0

S0

B0

CO

Cout

Draw three single wires as shown in the graph.

Name these wires as "A[3:0]", "B[3:0]" and "C[3:0]", as shown in the graph. Note that they become to bus after naming.
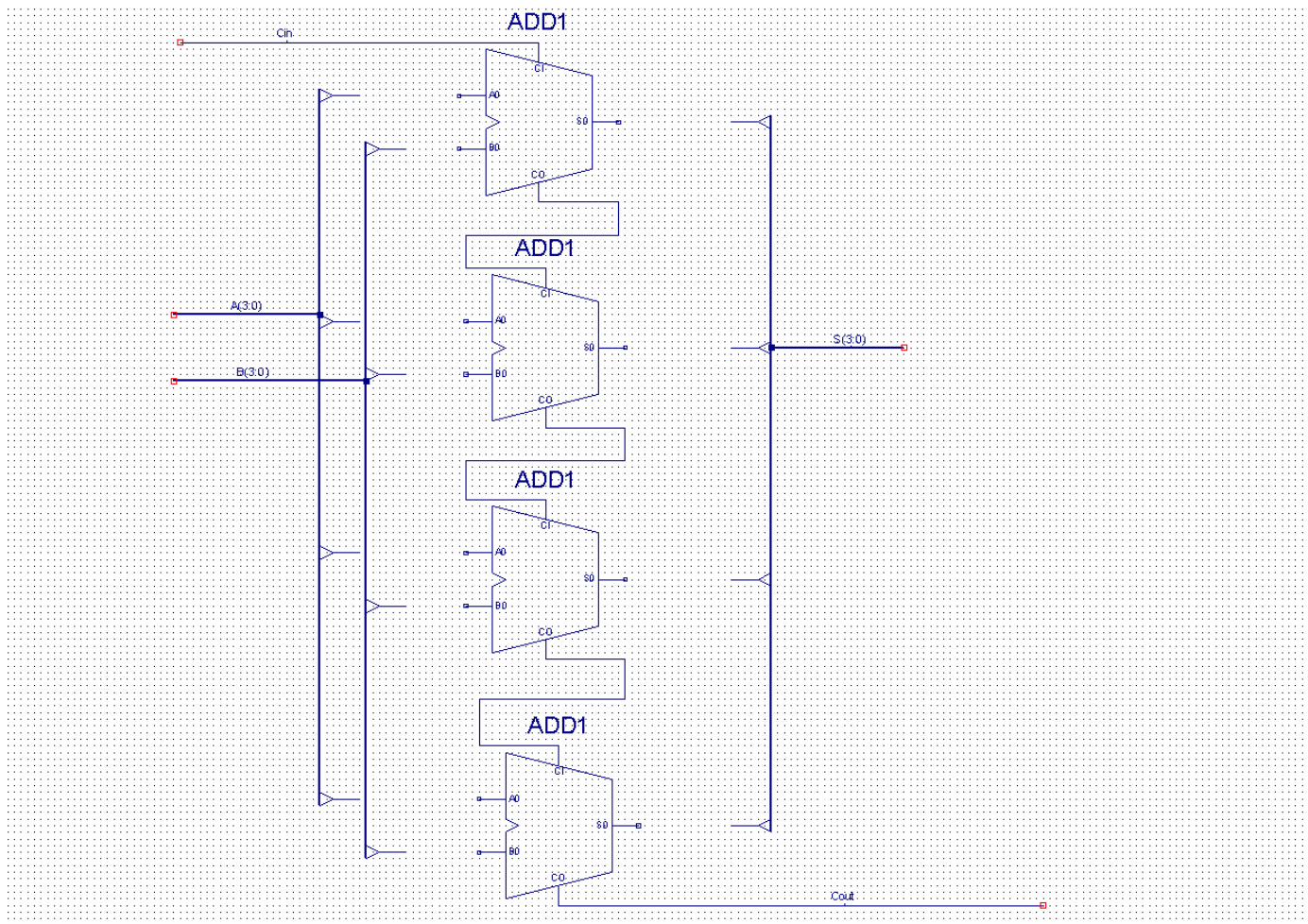
Extend these bus and put bus taps by click ⊢ , as shown in the graph. The flat end must be aligned with the bus you want to connect. And you can change the tap orientation in the Options window.

ADD1

ADD1

ADD1

ADD1

Cin

A(3:0)

B(3:0)

S(3:0)

Cout
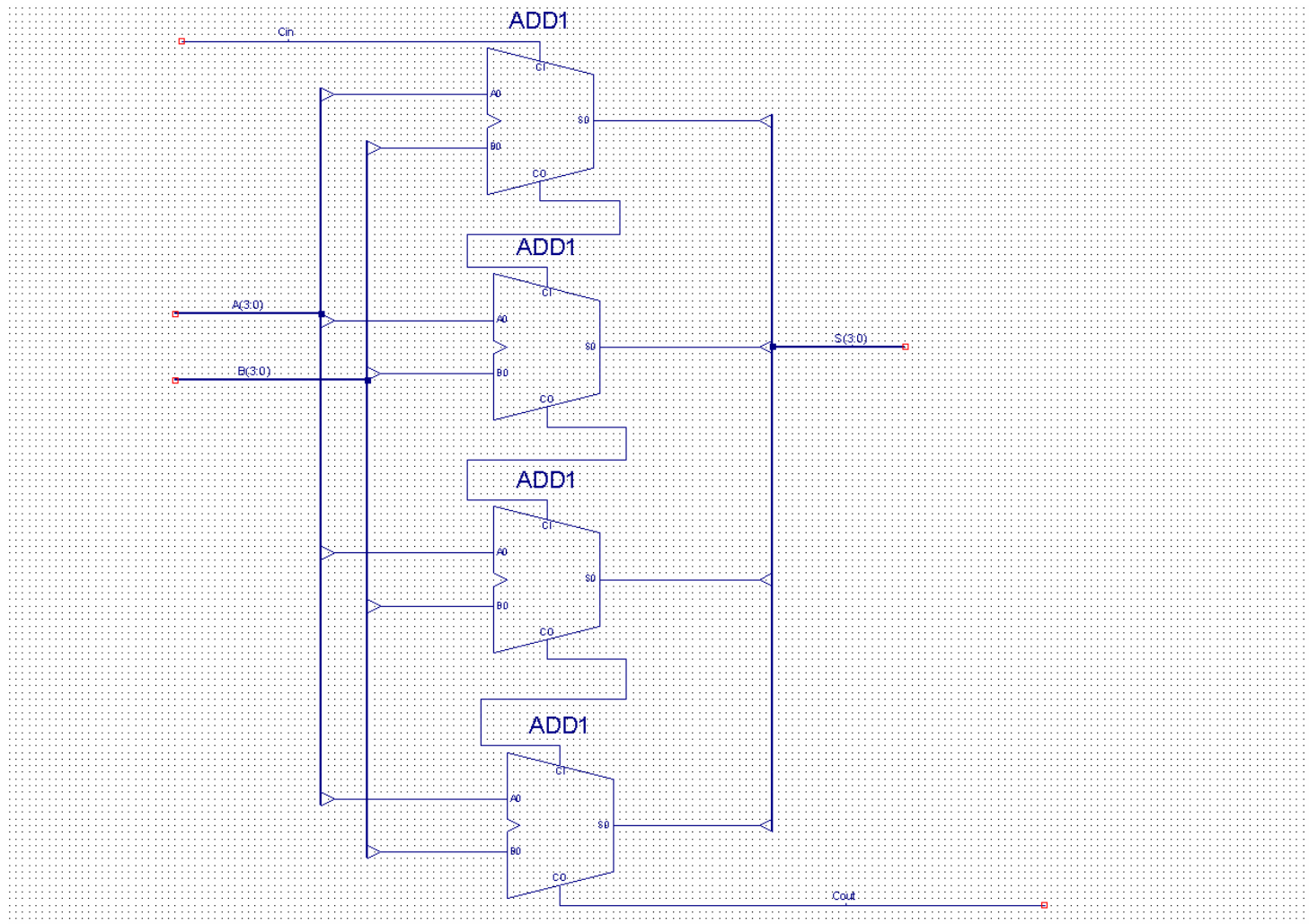
Connect each tap to a port of ADD1 by single wire.
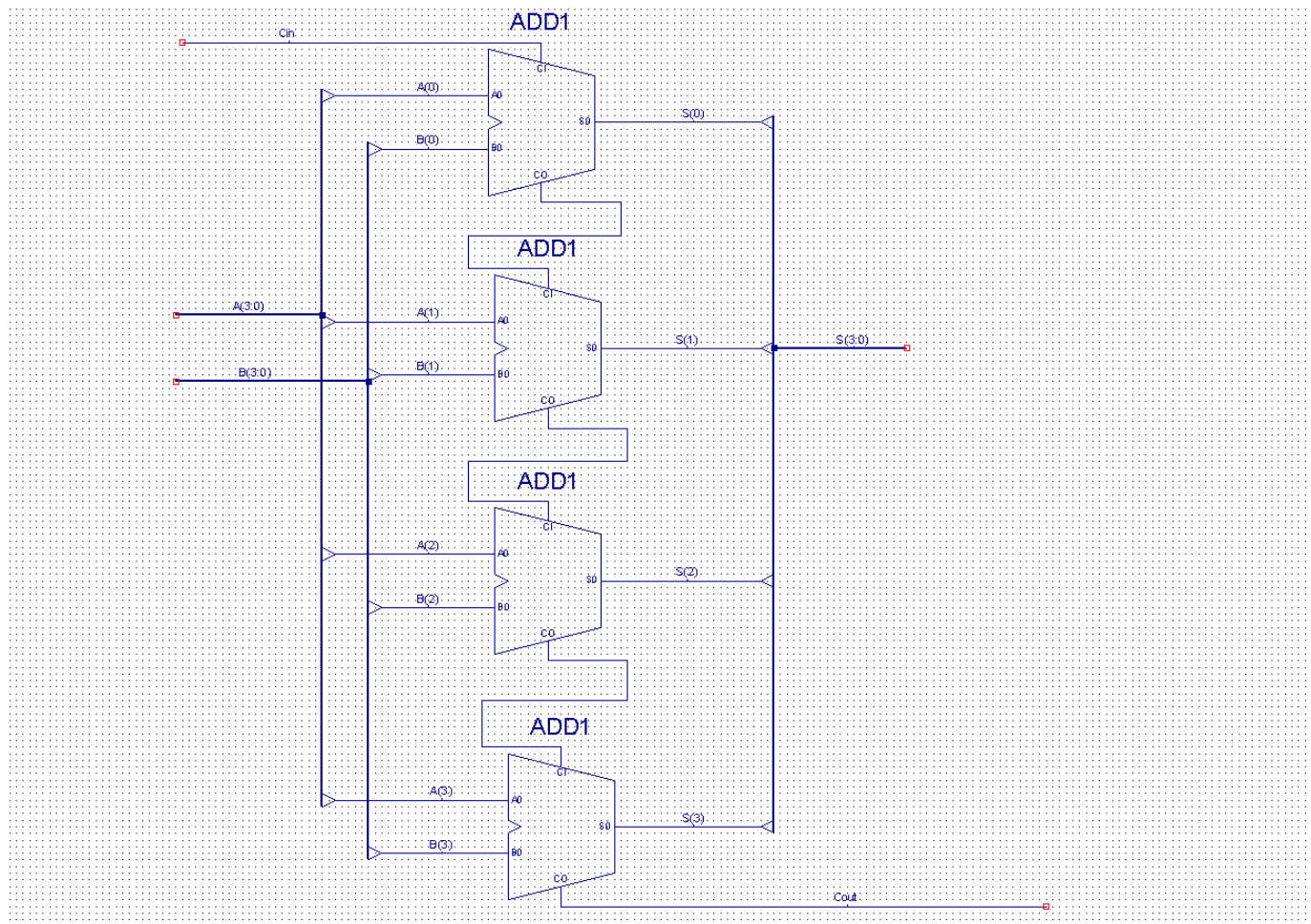
Name the each single wire as shown in the graph. Note that conceptually bus tap doesn't connect wires, but extends some wires from a bus. Therefore the branch must be a subset of the source bus, and they must have the same name.
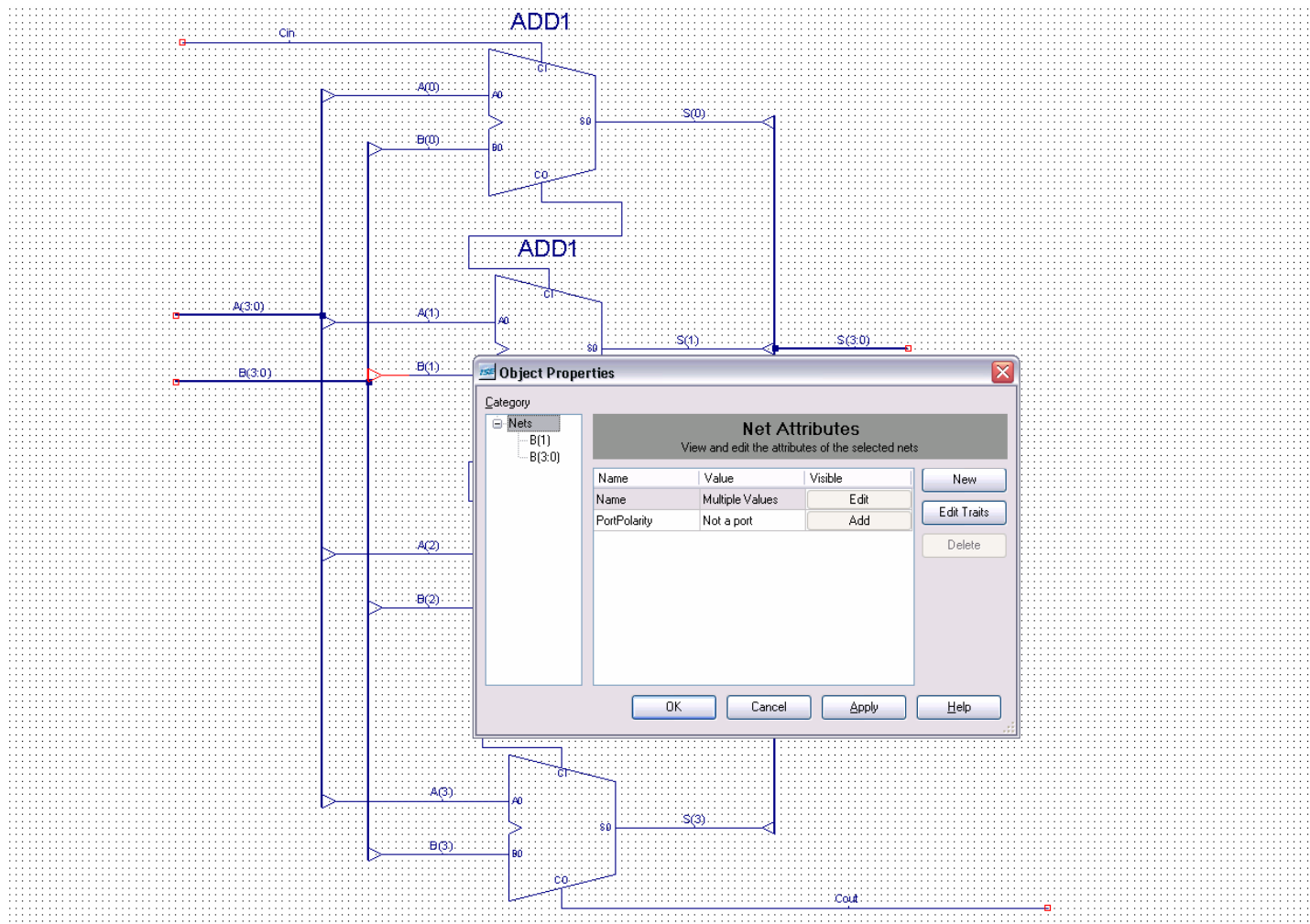
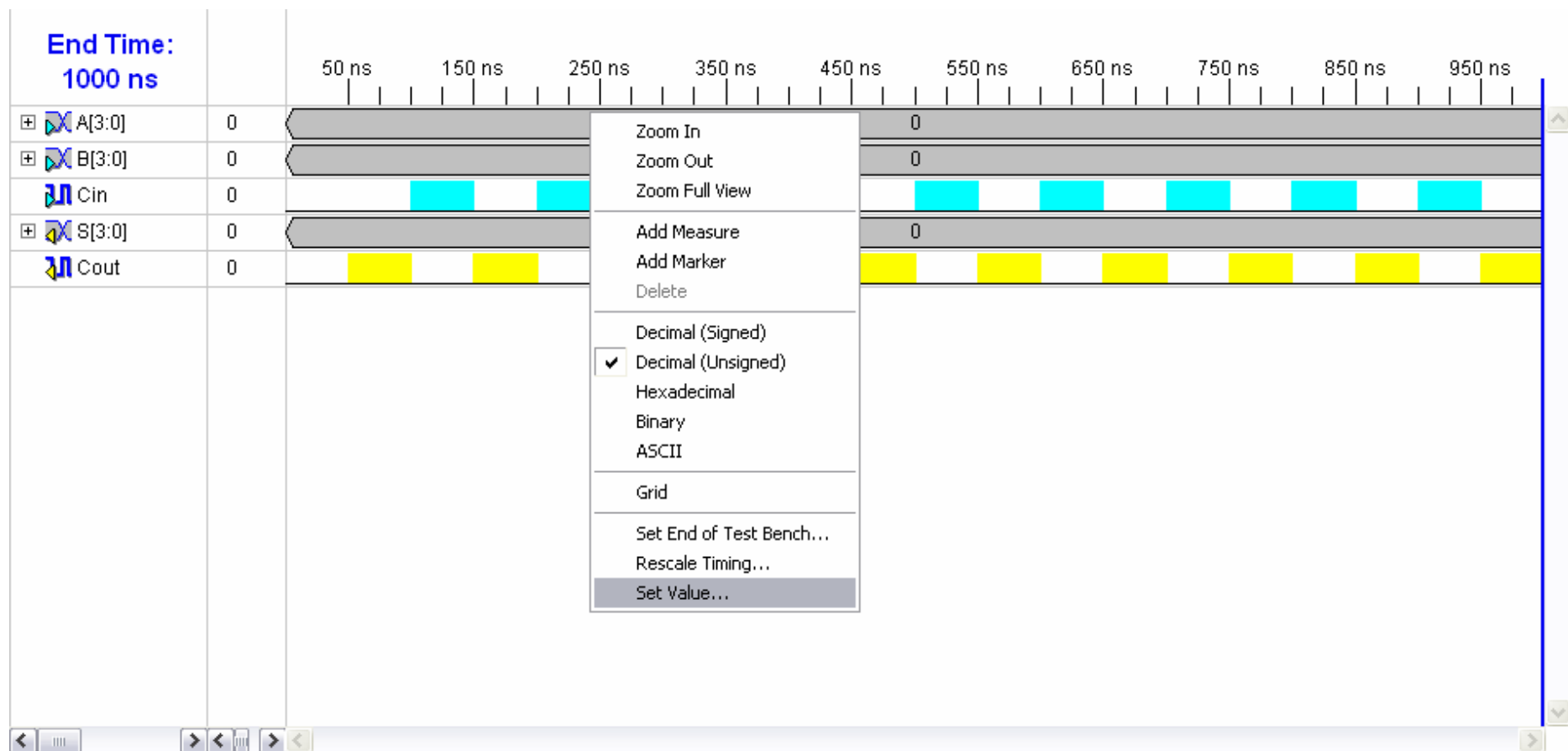To verify a bus tap, double click the bus tap, an object properties window will pop up. Check the names of connected nets.
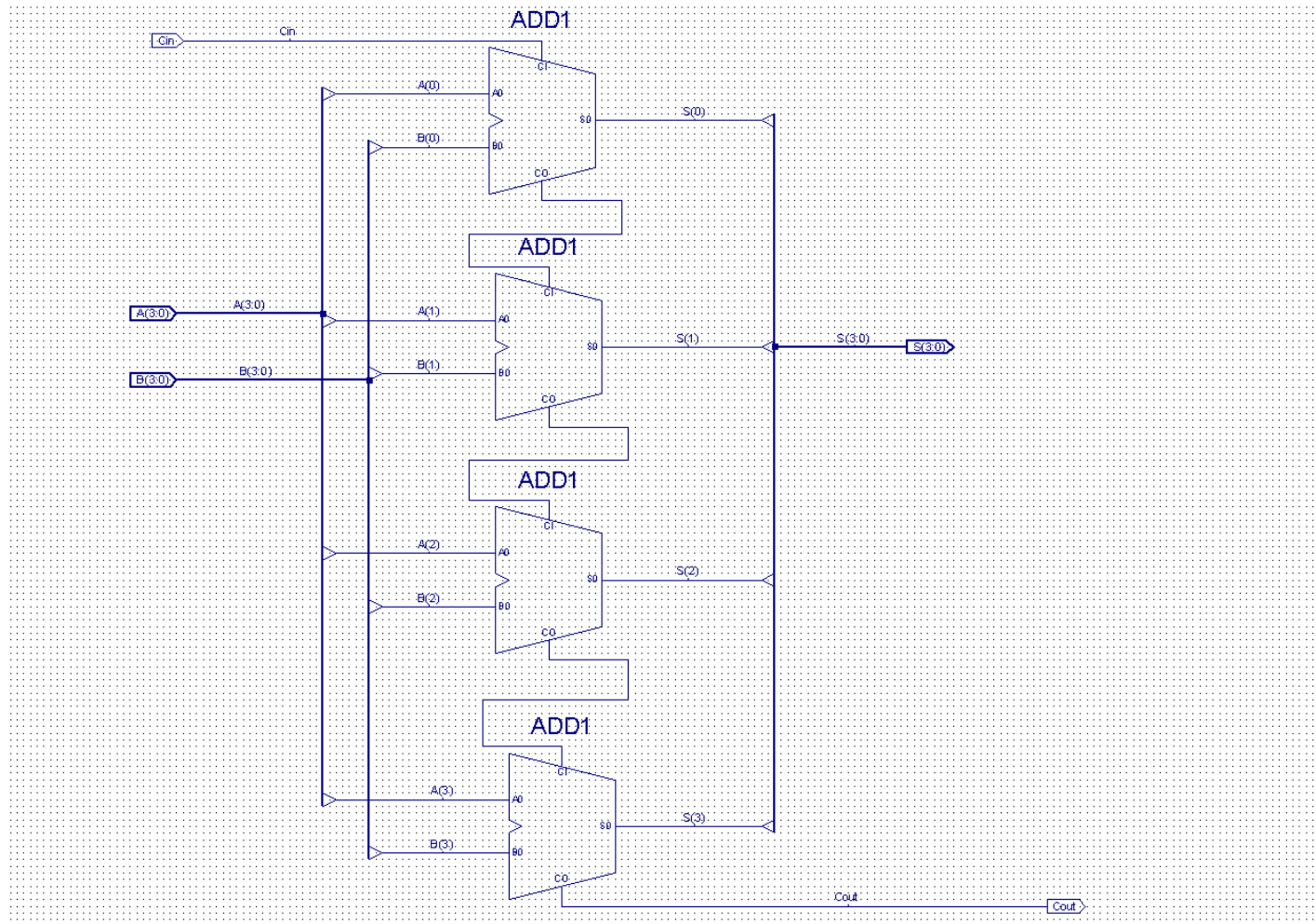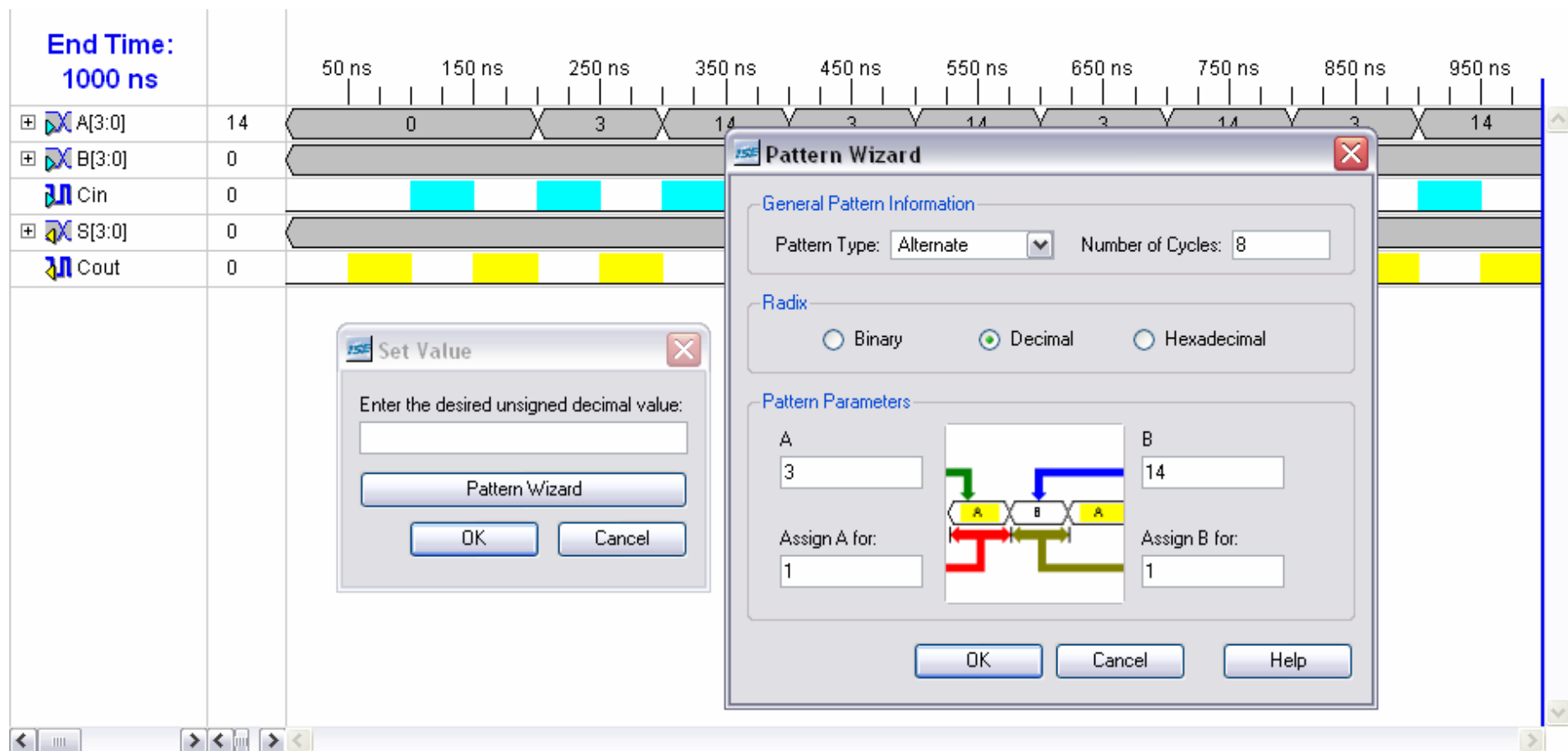
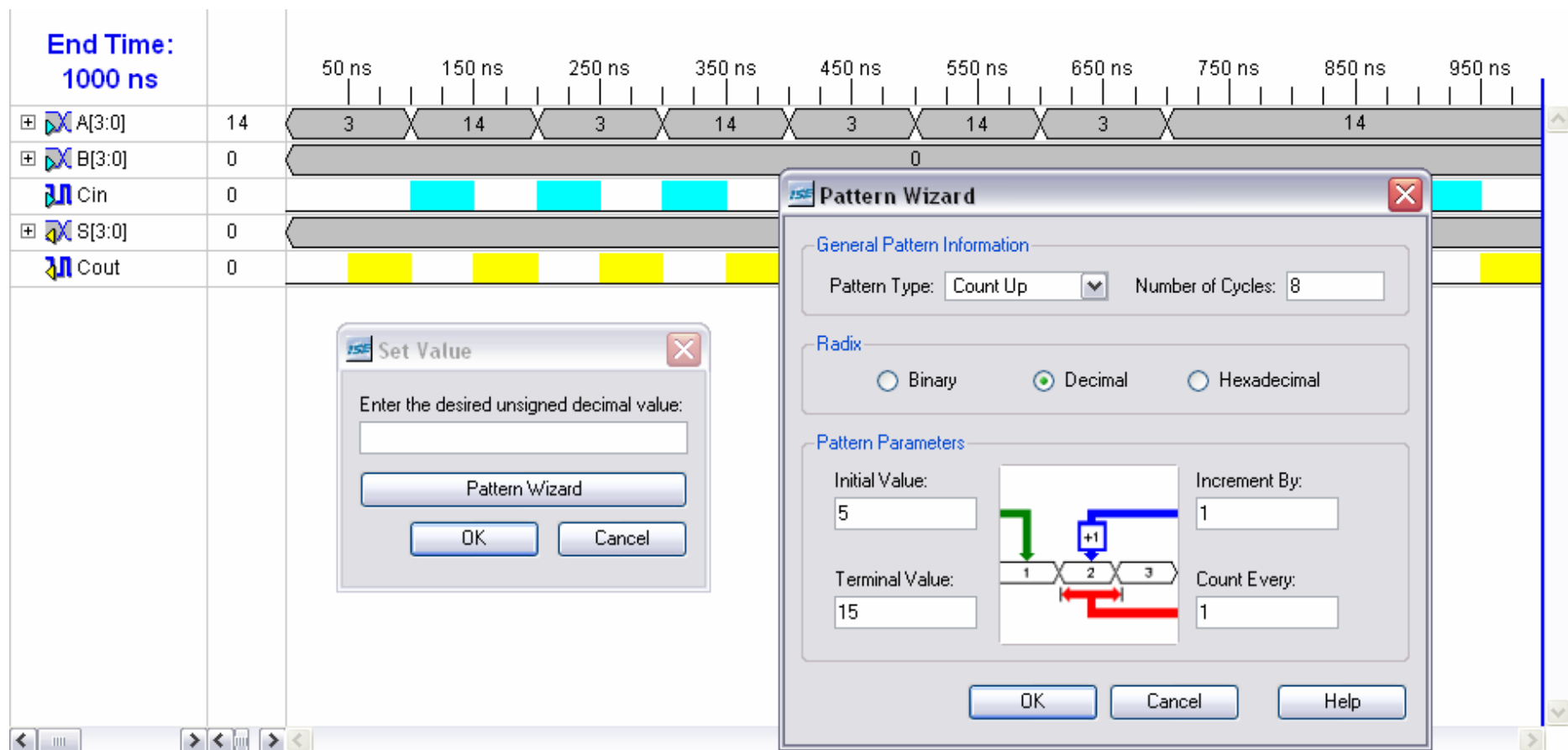Add input and outputs by ⊟. The design of a 4-bit adder is done.
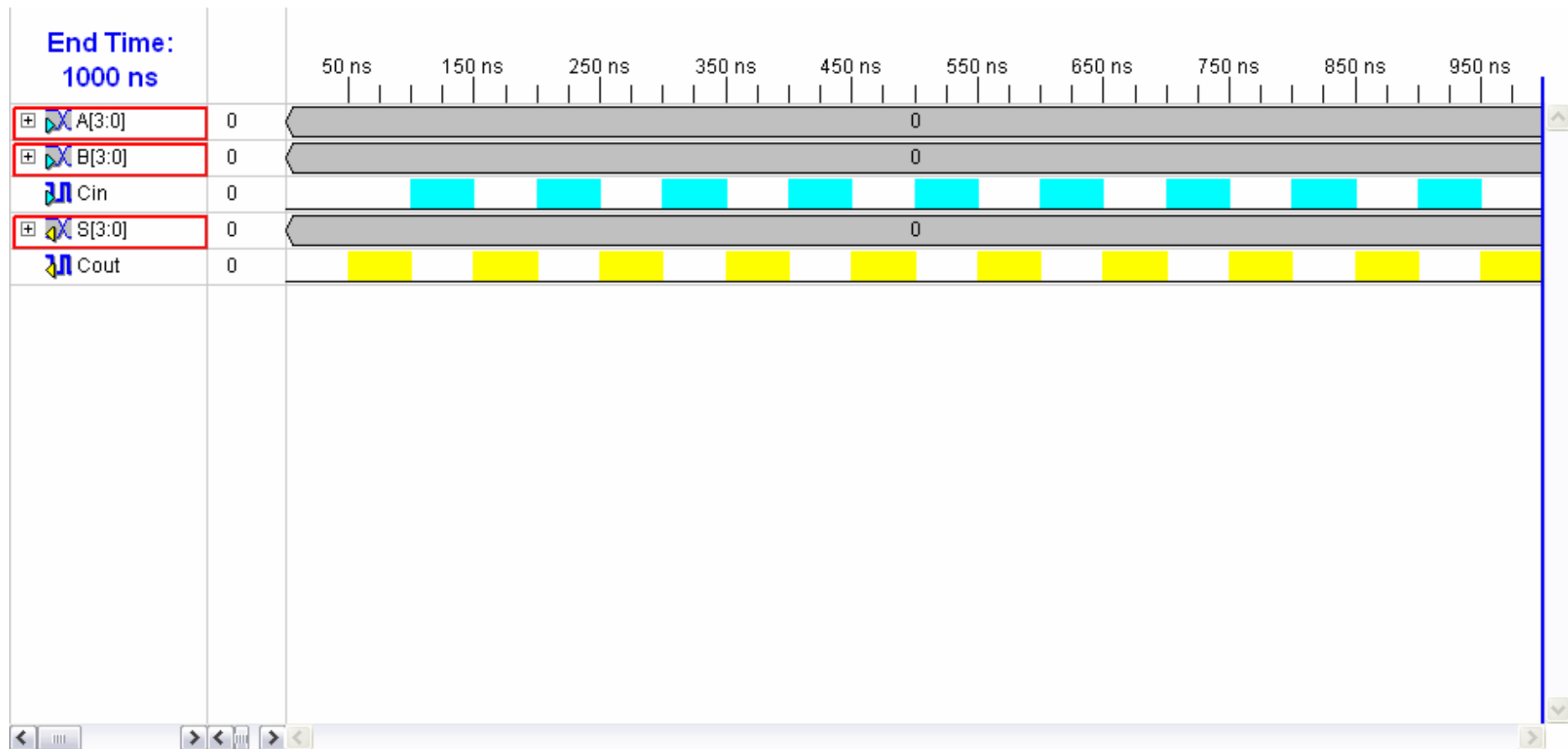
To simulate the 4-bit adder, create a Test Bench Waveform "test.tbw" and add it into the project. You will see bus "A[3:0]", "B[3:0]" and "S[3:0]".

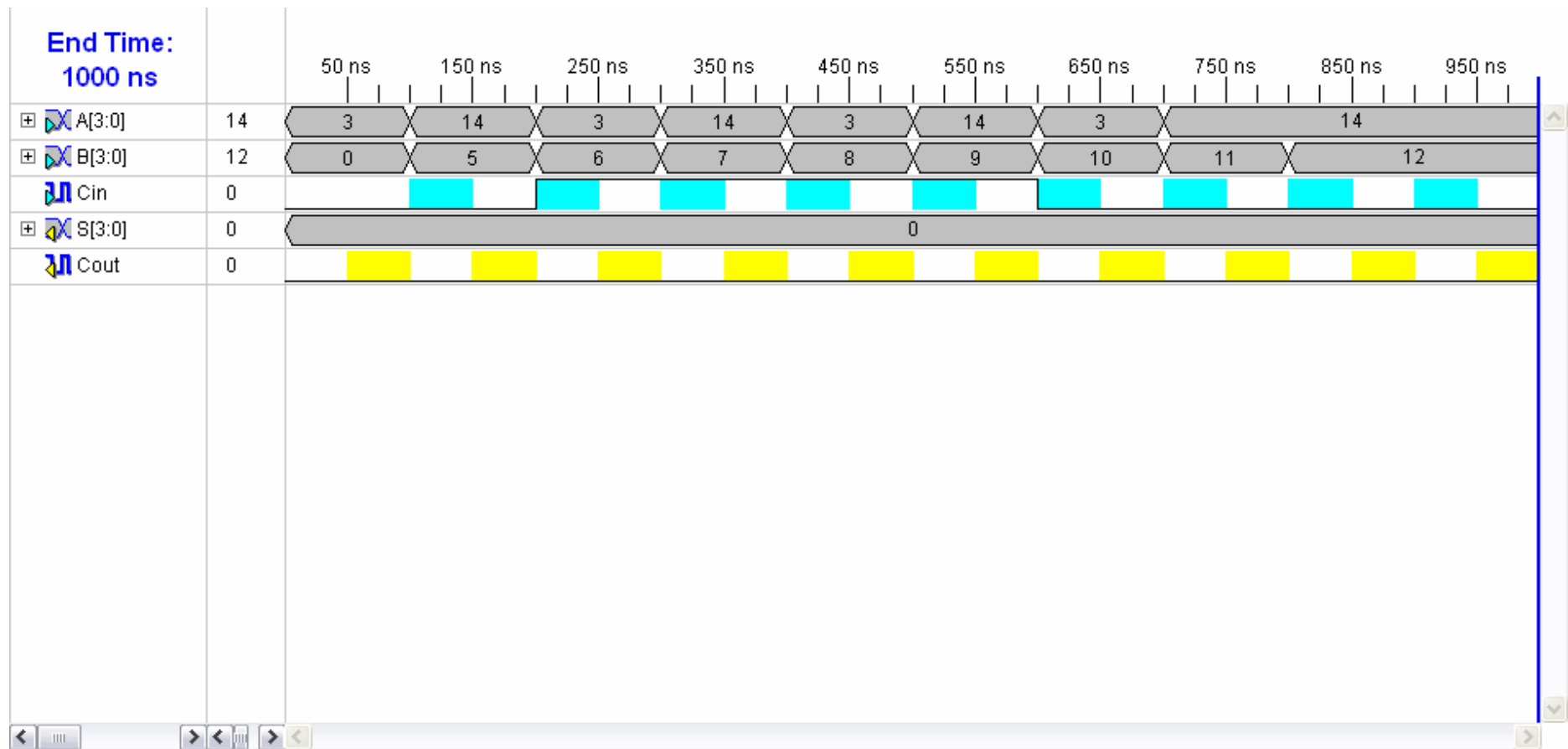All wires in a bus can be assigned as a group. Right click on bus "A", and select "set value…" in the pop-up menu.
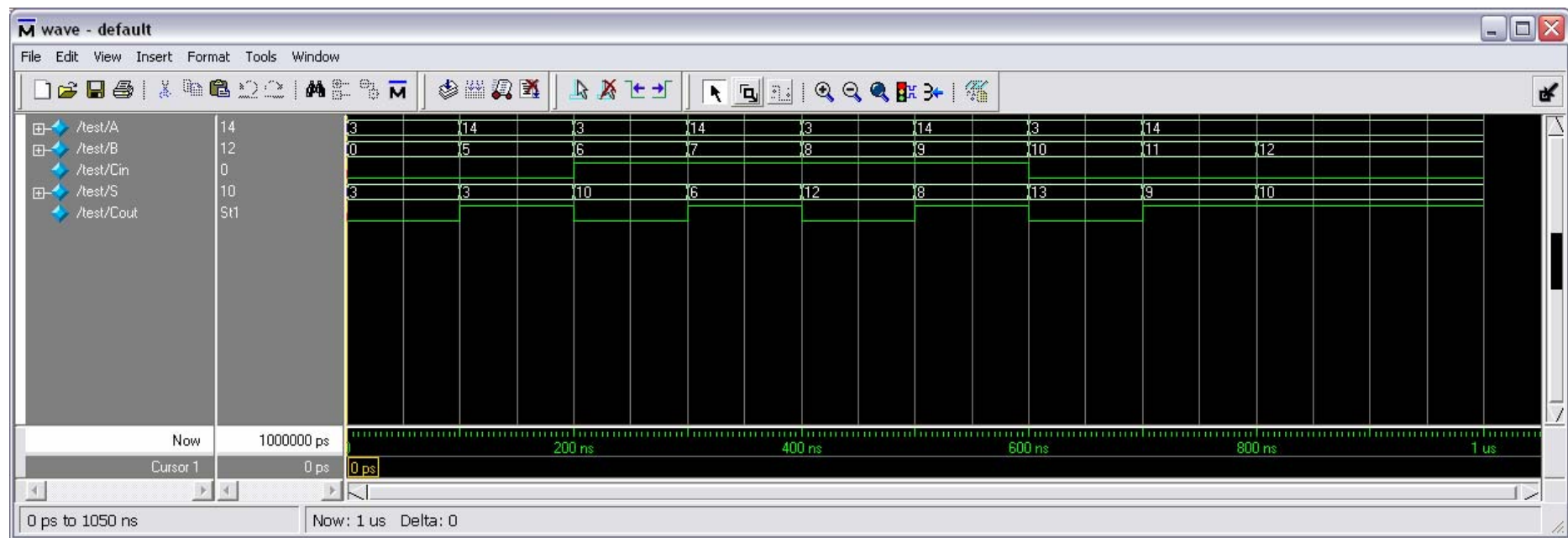
In the "set value" window, click "pattern wizard" button. You will the the "pattern wizard" window. You can set alternate, count, shift and random value to a bus.

At this step, we set bus "A" to alternate, as shown.

We set bus "B" to count up values. And set the single input port "Cin".

		50 ns	150 ns	250 ns	350 ns	450 ns	550 ns	650 ns	750 ns	850 ns	950 ns
A[3:0]	14	3	14	3	14	3	14	3		14	
B[3:0]	12	0	5	6	7	8	9	10	11	12	
Cin	0										
S[3:0]	0					0					
Cout	0										

Now the simulation waveform is completely set up. Save the file.

Here's the behavioral simulation result.