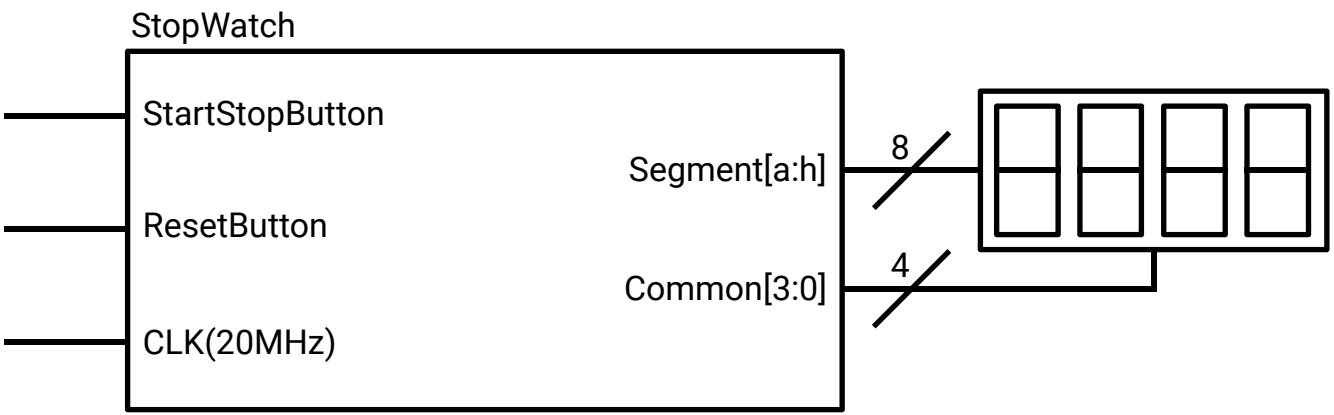
WARNING

The content of this document is intended to be an example only.

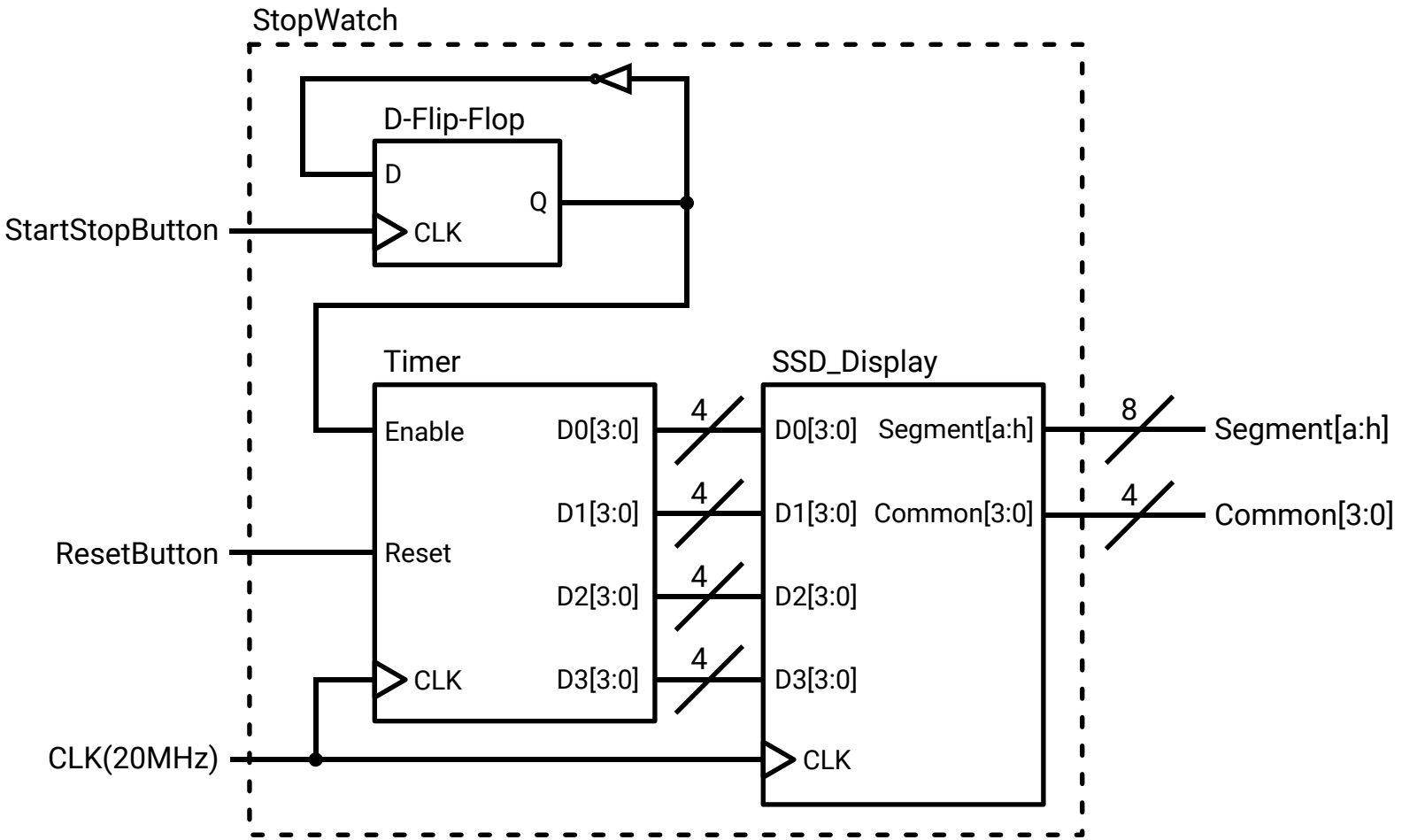
The design in this document is a simplified version made to be easier to draw a top-down design for and does NOT match with the actual implemetation.

This document is NOT verified to be correct by neither any T.A. nor the professor.

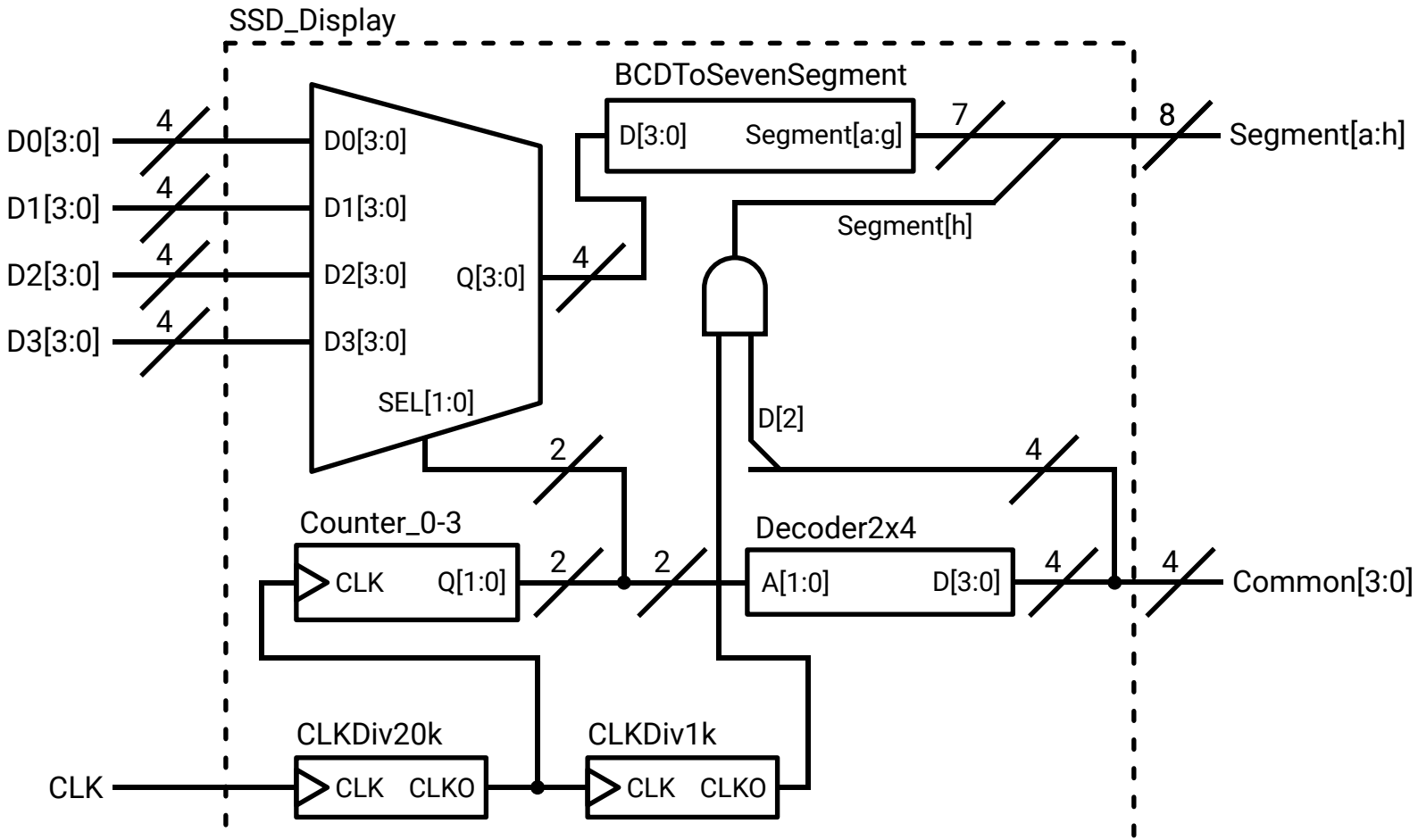
Top Layer


StopWatch
StartStopButton
ResetButton
CLK(20MHz)
Segment[a:h]
Common[3:0]
8
4

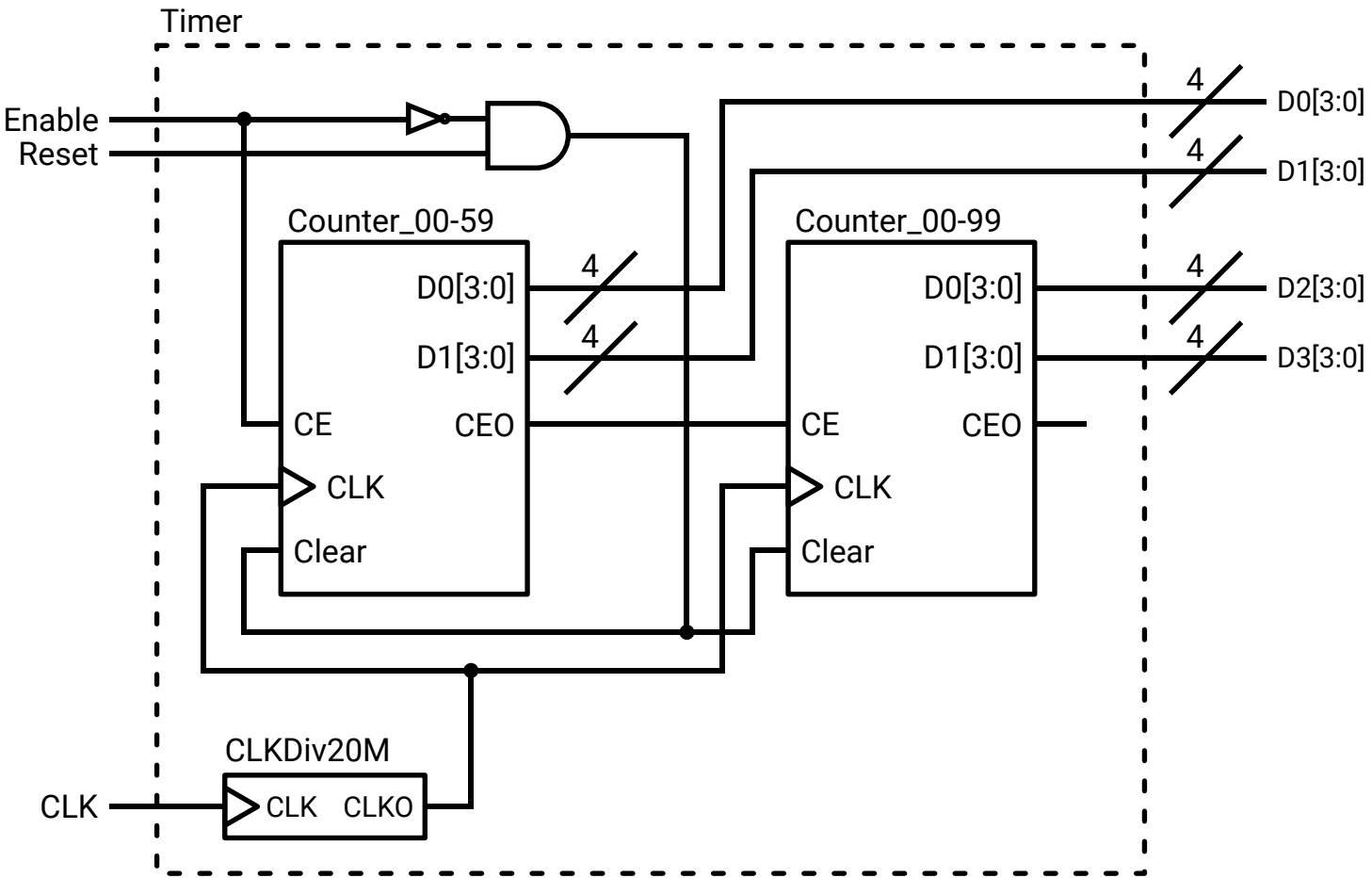
2nd Layer


StopWatch
D-Flip-Flop
D
Q
CLK
StartStopButton
Timer
Enable
Reset
CLK
D0[3:0]
D1[3:0]
D2[3:0]
D3[3:0]
ResetButton
CLK(20MHz)
SSD_Display
D0[3:0]
D1[3:0]
D2[3:0]
D3[3:0]
CLK
Segment[a:h]
Common[3:0]
4
4
4
4
8
4
Segment[a:h]
Common[3:0]

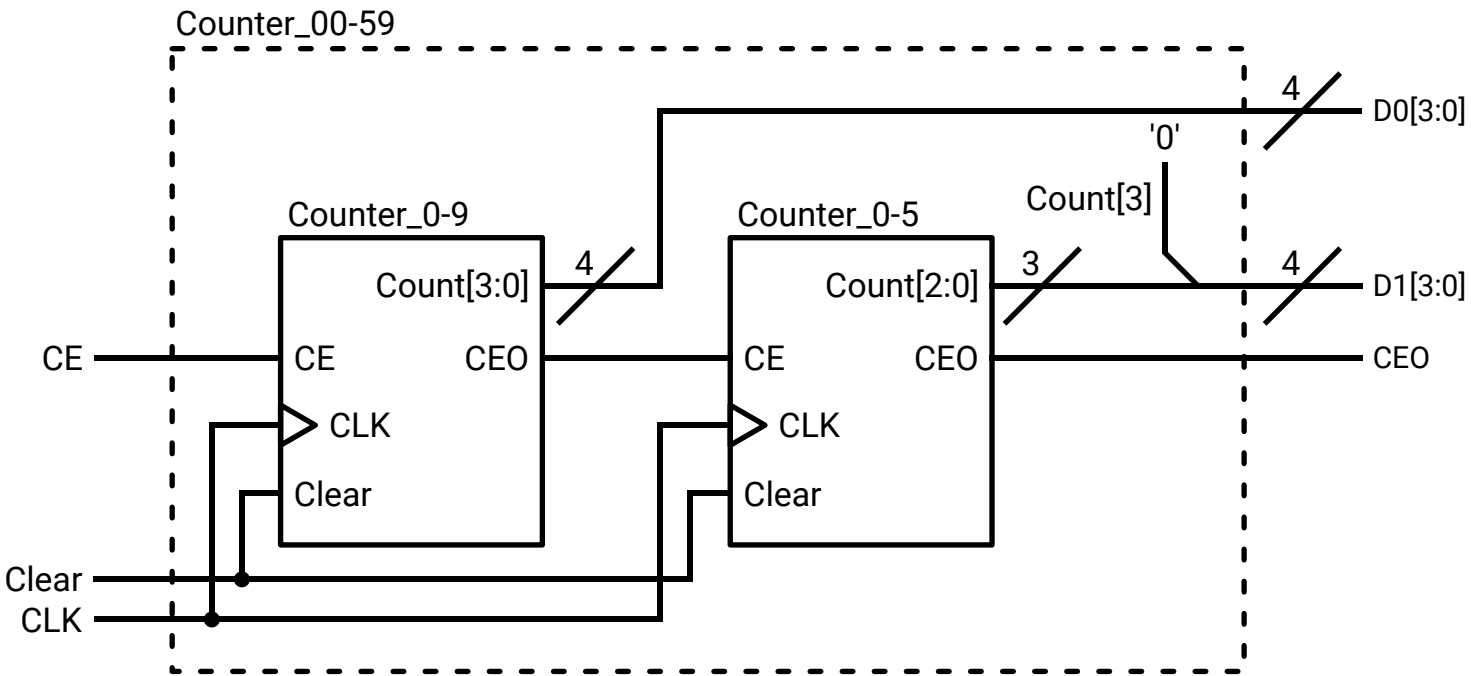
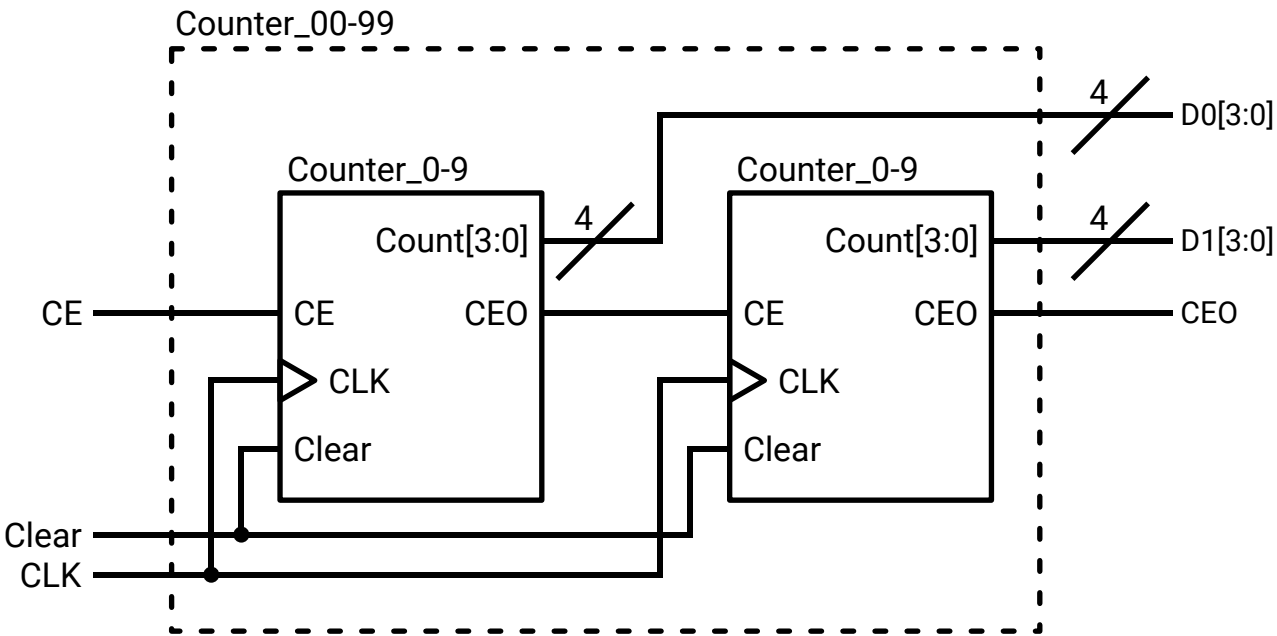
3rd Layer (SSD_Display)



3rd Layer (Timer)



4th Layer (Counter_00-59)



4th Layer (Counter_00-99)