

Universidade Federal de Roraima – DCC
Arquitetura e Organização de Computadores
Professor: Herbert Oliveira Rocha



Aluna: Nataly Almeida

Formato das Instruções

O processador LP possui 16 registradores, nomeados: \$zero, \$highReg, \$lowReg, \$compareReg, \$SO, \$S1, \$S2, \$S3, \$S4, \$S5, \$S6, \$S7, \$TO, \$T1, \$T2 e \$T3.

R

1

5 bits	4 bits	4 bits	3 bits
Opcode 15-11	Registrador 1 10-7	Registrador 2 6-3	Funct 2-0

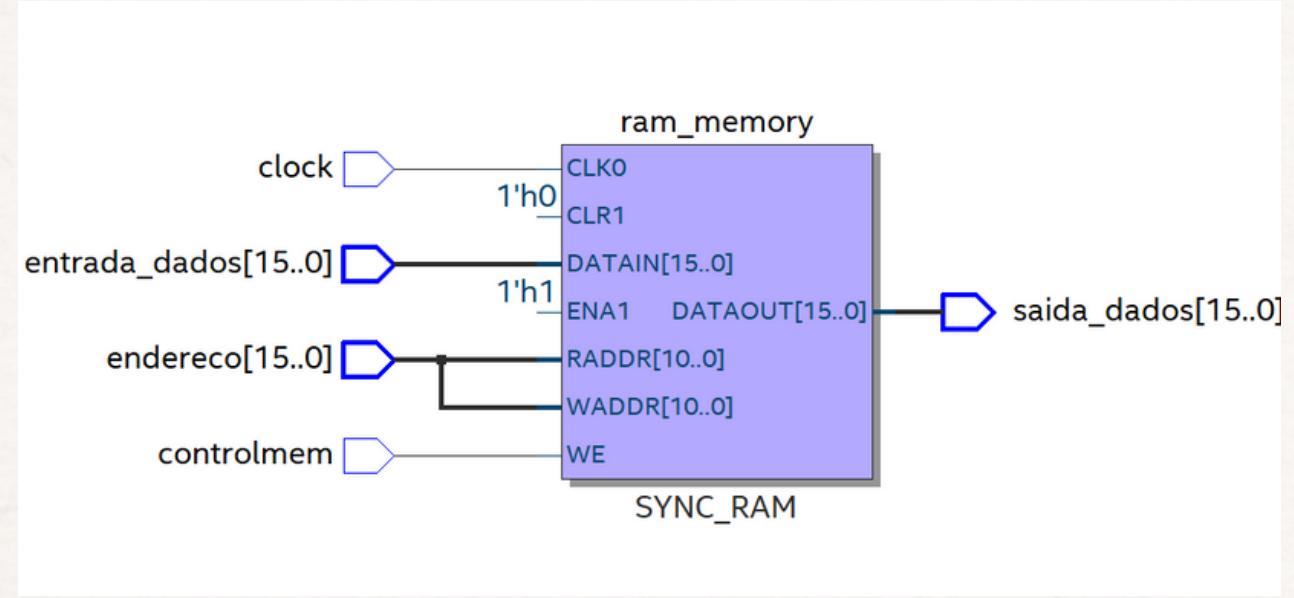
2

5 bits	11 bits
Opcode 15-11	Endereço de Destino 10-0

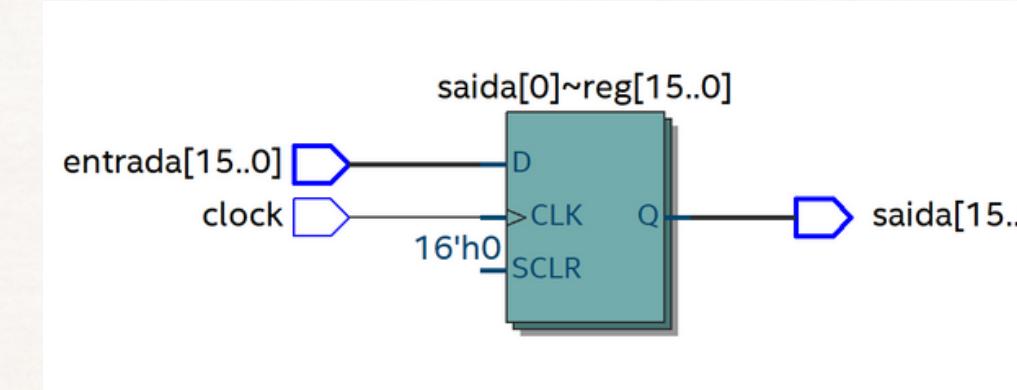
3

Este formato aborda instruções baseadas carregamentos imediatos na memória.

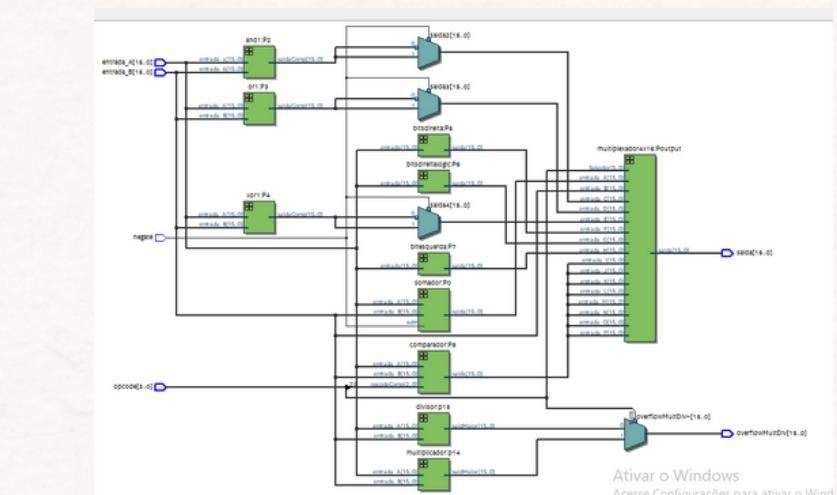
Memória RAM e ROM



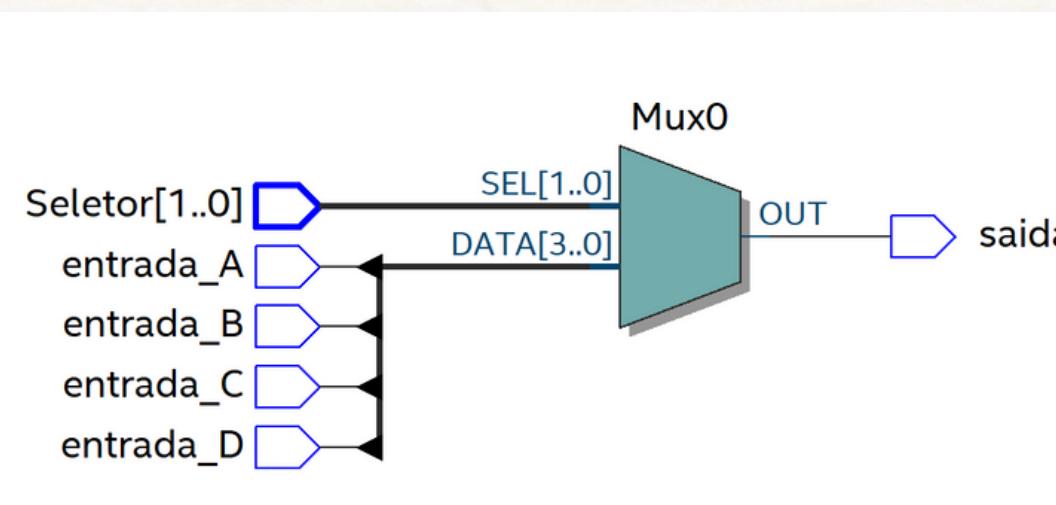
PC



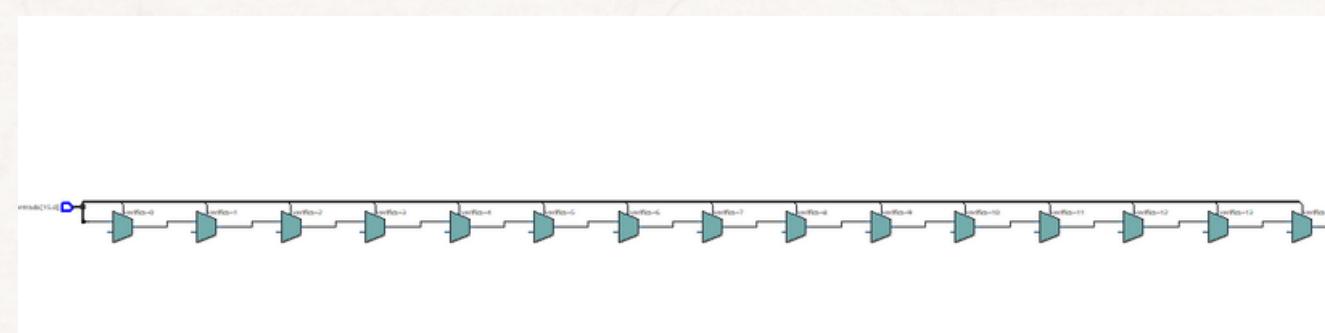
ULA



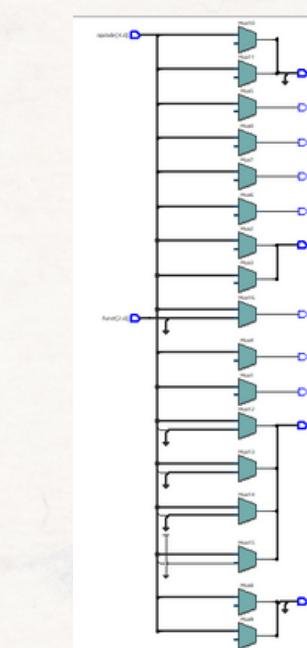
Multiplexadores



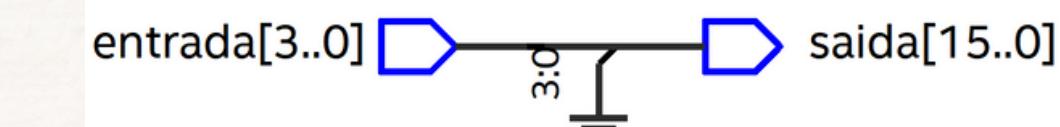
Encurtador



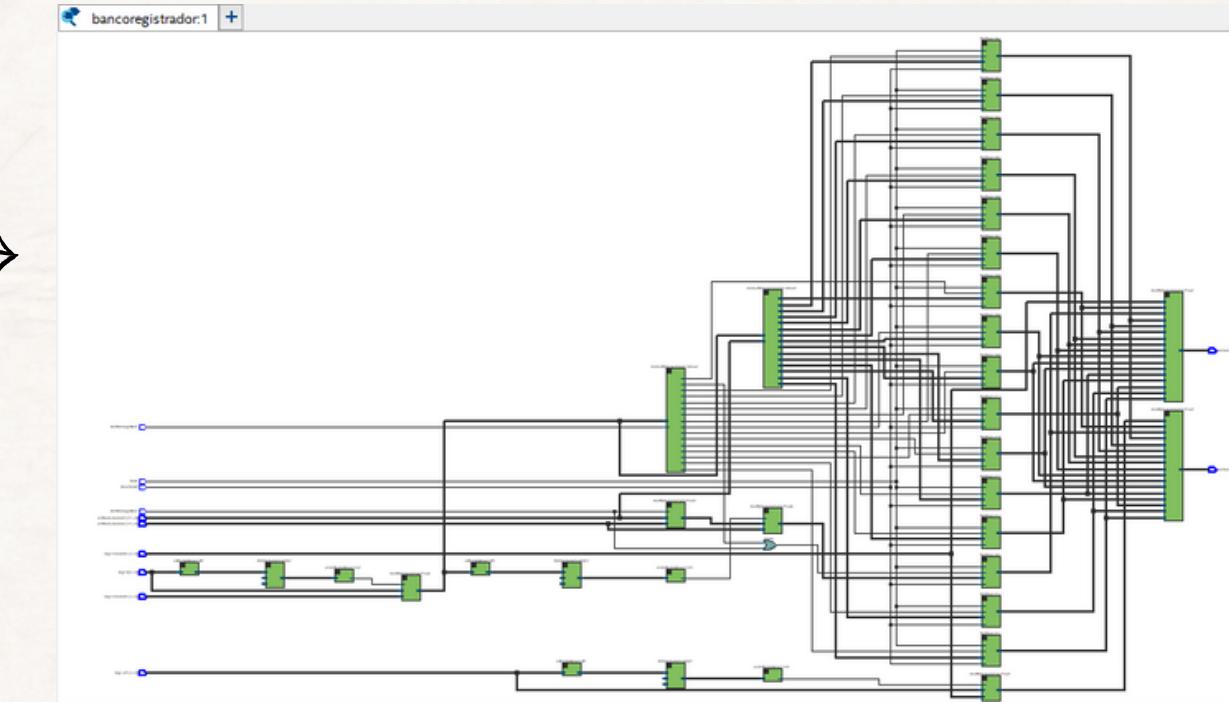
UC



Banco de Registradores



Extensores



Opcodes

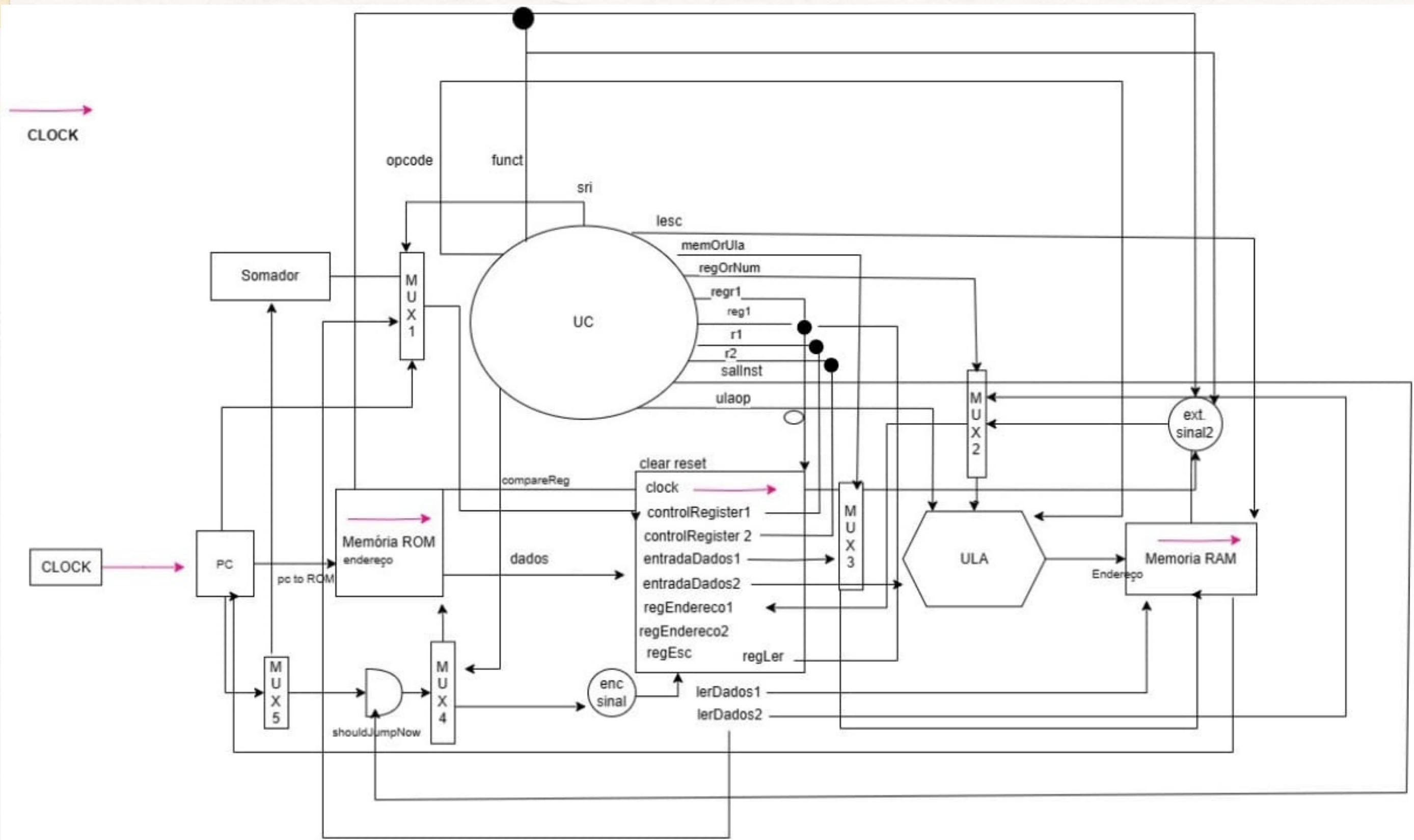
- São disponibilizados 5 bits para Opcode
- 27 Opcodes no total
- Incluindo os imediatos, comparadores, saltos e move

RTL Viewer

Processador LogPose



Datapath

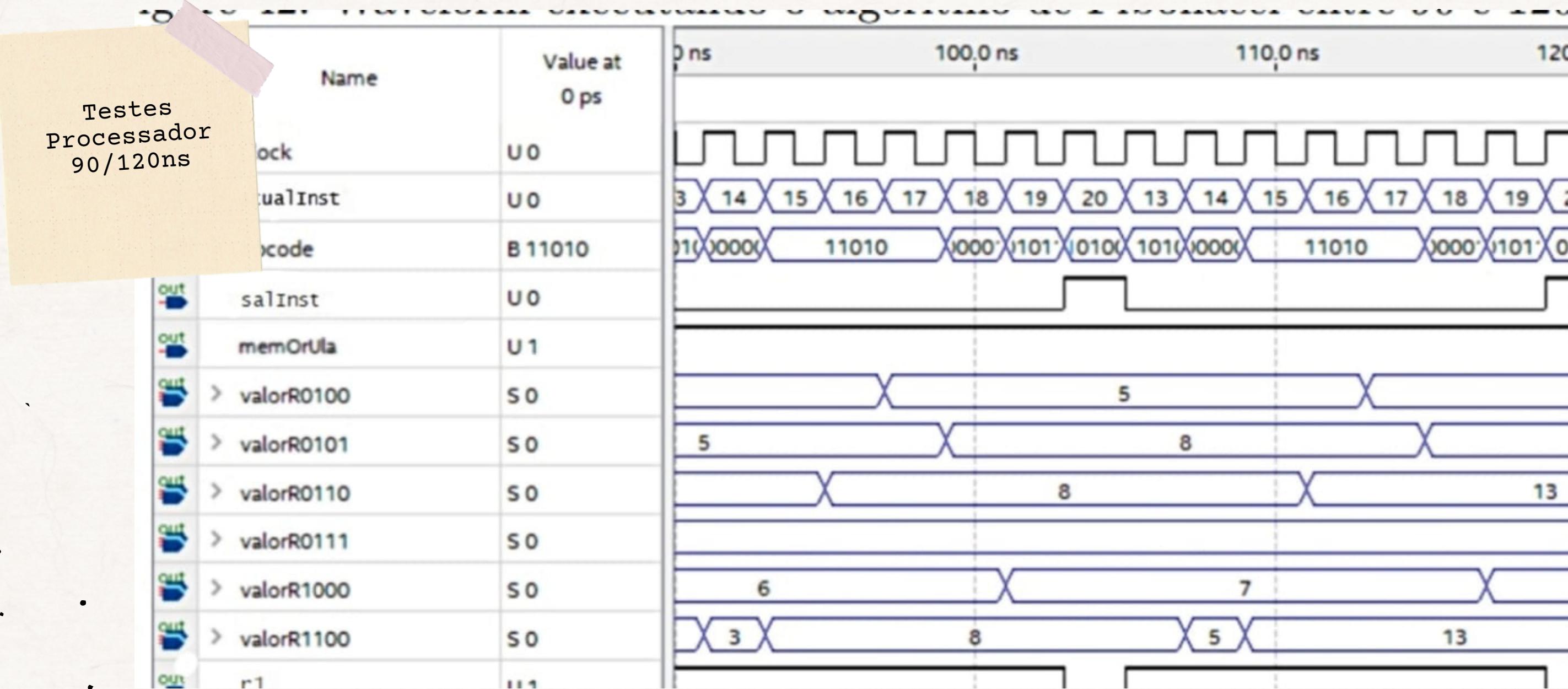


Fibonacci

Código detalhado para realização do Fibonacci

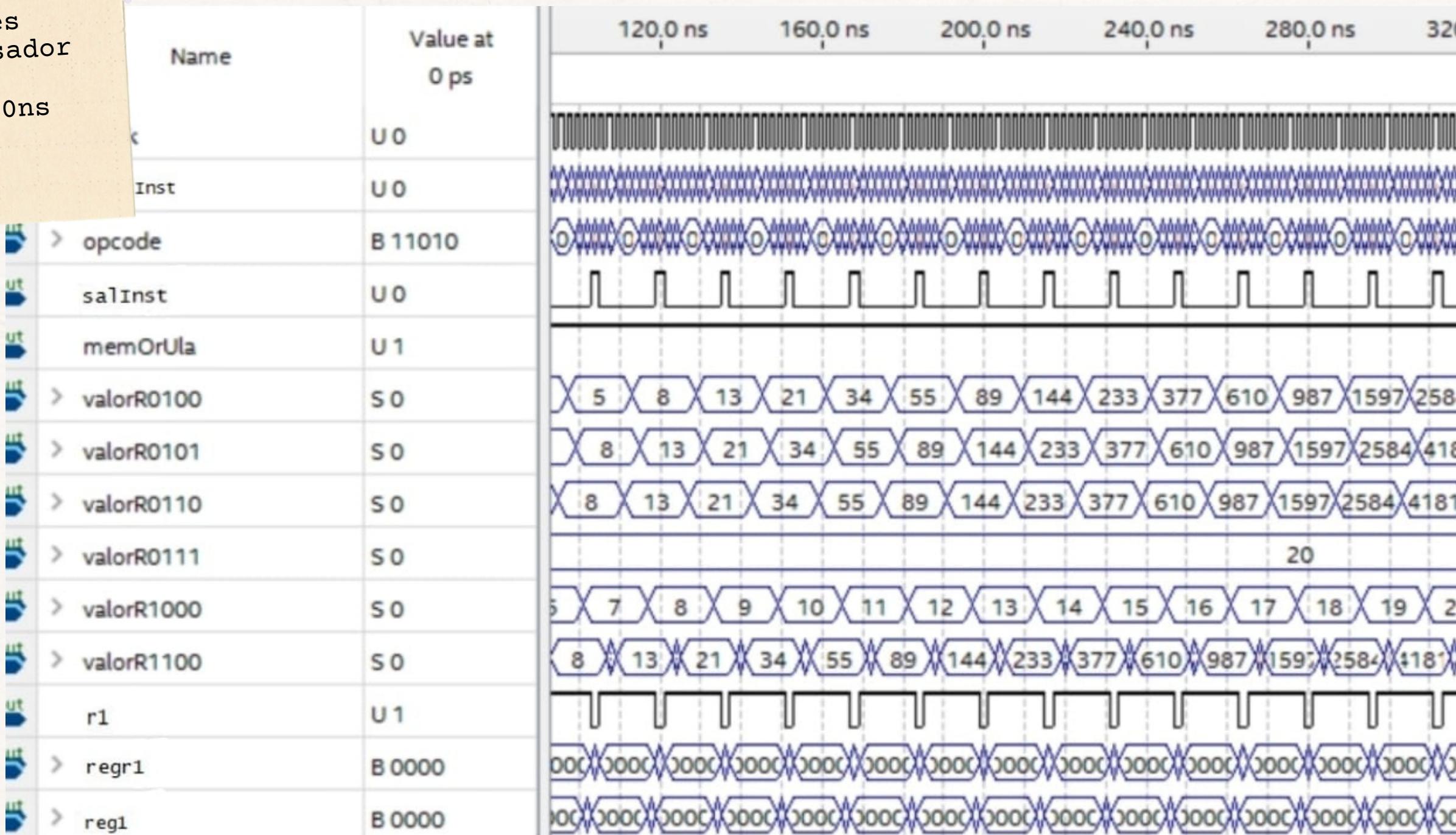
ENDEREÇO	SINTAXE	OPCODE	R1	R2	Instrução
01	main : movi \$s0 , 0;	11010	0100	0000	1101001000000001
02	movi \$s1 , 1;	11010	0101	0001	1101001010001001
03	movi \$s3 , 15;	11010	0111	1111	110100111111001
04	addi \$s3 , 5;	00001	0111	0101	0000101110101000
05	movi \$s4 , 2;	11010	1000	0010	110101000010001
06	smeq \$s3 , \$zero ;	01011	0111	0000	0101101110000000
07	jimbt Endg ;	10100	00000001111	1010000000001111	
08	move \$s2 , \$s0 ;	11010	0110	0100	1101001100100000

Waveform



Waveform

Testes
Processsador
LP
120/320ns



Referências

- PATTERSON, D.; HENNESSY, J. L. **Organização e projeto de computadores: a interface hardware/software.** 3^a Edição. São Paulo: Elsevier, 2005, 484 p.