**Stack Based Calculator Documentation**

**Block Diagram**

**BUS**

**n-reg /tribuf**

**n-reg /tribuf**

**n-reg /tribuf**

**n-reg /tribuf**

**Mem Test**

**Mem Control**

**ADDER/SUB**

**Multiply**

**Divider**

**STACK CONTROL**

**Memory Control Unit Commands**

ENTITY Mem\_Control IS

PORT ( Clk,Rst : IN STD\_LOGIC;

CNTRL : IN STD\_LOGIC\_VECTOR (2 DOWNTO 0);

LIV,RI, RO : IN STD\_LOGIC\_VECTOR (3 DOWNTO 0);

Bus\_In : INOUT STD\_LOGIC\_VECTOR(3 DOWNTO 0);

STATE : OUT STD\_LOGIC\_VECTOR (1 DOWNTO 0);

R : BUFFER STD\_LOGIC)

**Operations:**

Format: CNTRL| RI/RO | RI/RO

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Format: 001 | z,z,z,z, | xxxx | R

Description: move LIV to register Z

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Format: 010 | z1,z1,z1,z1 | z2,z2,z2,z2 | R

Description: Move Z1 register into Z2 register

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011 | z,z,z,z | xxxx | R

MOV Z TO BUS

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100 | z1,z1,z1,z1 | z2,z2,z2,z2 | R

MOV BUS INTO Z

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101 | z1,z1,z1,z1 | z2,z2,z2,z2 | R

CLR REGs

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Notes: R = done bit , State = temp debug , a RST pulse must occur before a command will execute. Command bits must be present until R done bit is asserted.