FYS4220 - Fall 2013 : Lab. Exercise 1

Kévin Zaporogezt and Nathalie Bonatout

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Introduction

This lab exercise is an introduction to the FPGA programmation in the environment Quartus II. Thus, we discovered during this work some of the most useful features provided by Quartus, and the way to do a simulation thanks to the software ModelSim. The exercise too allowed us to learn how to use and connect the board DE2, how to manage its components such as the LEDs or the 7-segment decoder.

1 Getting Started

A - Switches and LEDs

B - 7-segment decoder with functional and timing simulation

We want here to implement a 7-segment decoder displayed on the output HEX0 of the board.

10.

11. We increased the time between the transition on SW from 5 ns to 20 ns. And the outcome of the simulation obviously changed: indeed the whole simulation takes in place in 20 ns. Thus, with a transition of 20 ns, we can see only one of them!

12.

2 4-bit Counter and push Button

11. After pressing KEY0, we can see that the value displayed seems to jump from a value to another, discontinously. We cannot see the counter incrementing smoothly, by step of 1, and this is rather expected. Indeed, the frequency of the clock is 50MHz. This means that the value of the counter changes every 20ns as long as the button KEY0 is pushed.

We could see the value of the counter be incremented by step of 1 by delaying the clock, or by implementing a boolean which would block block the value of the counter after once incrementation, when KEY0 is pressed.

Algorithm 1 Implementation of the blocking boolean

```
counter <= "0000" when reset_n = '1'
else unsigned(std_logic_vector(unsigned(counter) +1))
when rising_edge(clk50) and ext_ena_n = '0'
and (countenable = false);
with ext_ena_n select countenable <= false when '1'
, true when others;
```