Nathan Abebe

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Summary

Highly driven researcher and engineer specializing in critical, low-latency systems. Experienced in scalable FPGA architectures, embedded software development, and all types of real-time systems. Passionate about delivering high-impact solutions that accelerate innovation and system efficiency.

Education

Yale University New Haven, CT

B.S. Computer Science, B.S. Electrical Engineering (ABET) May 2028

- Relevant Coursework: VLSI System Design, FPGA-Based Acceleration, Computer Networks, Operating Systems

Experience

Undergraduate Research Assistant Jun 2025 – Present

Yale University, Advisor: Professor Lin Zhong, Ph.D. New Haven, CT

- Accomplished 80% reduction in development time by engineering a virtual file system for multi-FPGA control, validated by DECONET/HELIOS, a production-grade distributed quantum error code decoder.
- Developed distributed network for server-FPGA communication with custom UDP/TCP protocols, achieving 100% critical packet delivery & <1 minute end-to-end time for FPGA configuration.
- Ported and optimized Micro Blossom quantum error correction software for distributed execution on FPGA-attached ARM cores, achieving the first such implementation with 14× latency reduction.
- Enabled scalable multi-FPGA parallelism by designing file system architecture with support for thousands to millions of FPGA nodes, to be used for high-throughput quantum error code decoding experiments.
- Simplified user experience by developing 5+ Bash scripts & a scripting language, reducing project setup and configuration to 1-2 commands per FPGA.

Projects

Project Liquid: Flight Computer | *Rust, Real-Time Systems, Radio Protocols* Aug 2025 – Present

- Designed PCB integrating Teensy 4.1 and sensors to enable onboard sequencing, improving system reliability.
- Programmed real-time logic for fueling, arming, apogee detection, chute deploy, & comms, for safe mission ops.
- Built TDMA-based radio protocol with CRC & ACKs achieving <100ms end-to-end latency.
- Offloaded non-critical compute to coprocessor, reducing comms latency by 30% & improving system reliability.

Project Liquid: EGSE | *C++, Sensor Integration, LTspice, HIL Testing* Oct 2024 – Present

- Programmed Teensy 4.1 firmware for GPIO valve control to automate 10+ ethane & nitrous valves.
- Developed C++ drivers for NAT 8252 pressure sensors with ±1% measurement accuracy.
- Simulated 20+ circuits in LTspice to verify signal integrity & fail-safes, reducing hardware faults during testing.
- Executed HIL validation tests with 99.9% uptime during hotfire campaigns, ensuring robustness in real conditions.

Graphics Research: Wavefront (.obj) Parser | *C++, SIMD, Multithreading, Optimization* Jul 2025 – Present

- Implemented fast .obj parser with file chunking parallelism and SIMD instructions, reducing parse times 7× compared to industry standard.
- Used profiling tools to optimize code iteratively, resulting in 500x speedup after a month of optimizations.

NES Emulator | *Rust, Computer Architecture, Debugging* Mar 2025 – Present

- Built 5K+ LoC cycle-accurate NES emulator with full CPU and PPU timing support for precise game emulation.
- Crafted egui debugger with live stepping and visualization to accelerate development and debugging.

Technical Skills

Languages: Rust, C, C++, Python, D, SystemVerilog, Golang, x86 Assembly, TypeScript, JavaScript, C#
Embedded: FPGA design, STM32, Linux, RTOS, Yocto, bare-metal, PCB design
Tools: Git, GDB, Valgrind, Vivado Design Suite, Oscilloscope, Altium Designer, LTspice
Protocols: UDP, TCP, UART, SPI, I^2C, BGP, IS-IS, TDMA, CSMA, CRC