2309 EIE131 Course Outline

Subject Code : **EIE131**
Subject Title : Digital Circuits Laboratory
Level : 2
Credits : 3
Teaching : Lecture 12 hours
Activity : Lab 33 hours
Prerequisite : N/A

Class Schedule :

Class	Time		Classroom	Date
D1	Tue	15:30-18:20	B401	4/9/2023-17/12/2023

Instructor : Dr. KinTak U
Contact Number : (853)8897-2249
Email Address : ktu@must.edu.mo
Office : C403
Office hours : Tue. 13:30-15:30; Wed. 15:20-18:20
Thur. 15:20-18:20; Fri. 13:30-15:30

Course Description

This subject aims to make the students familiar with the basic analysis and design method of the digital circuit through some practical exercises and experiments. Topics including the analysis and design of combinational logic circuit, arithmetic function, sequential logic circuit with Programmable Logic Device (PLD) will be conducted and studied.
The circuit design tool and hardware description language will be introduced to lead the students to learn how to implement and design the digital circuit with some given design requirements in PLD. In this way, the students' understanding of theoretical knowledge is enhanced and their independent problem–solving ability is also developed. Experiments should be finished by students to verify their practical abilities on circuit designing thus enhancing their skills on it.

Textbook(s)

No recommended textbook, but the learning materials will be provided to students during the classes

References

Book title：Digital Design: International Editions
Author/Editor：M. Morris Mano, Michael D. Ciletti.
Edition：5
ISBN：9780273764526
Publisher：Pearson, Prentice Hall
Date：2012

INTENDED LEARNING OUTCOMES

Upon successful completion of this subject, students will be able to:
1. Design the digital circuit diagram with its test vector to do function simulation under PLD IDE.
2. Construct and test some typical combinational logic circuits such as half adder, full adder and ripple carry adder with hardware description language under PLD IDE.
3. Construct and test some typical sequential logic circuits such as D-flip flop and sequence generator with hardware description language under PLD IDE.
4. Construct and test some serial-input logic circuits such as serial adder with hardware description language under PLD IDE
5. Write the technical reports based on the experimental results.

Schedule

Index	Topic	Hours	Teaching Method
1	Introduction to PLD Design and Simple Practice	6	Lecture
2		1+5	Lecture+Lab
3	Experiment I : 4-bit Full Adder Design	1+5	Lecture+Lab
4	Experiment II : Sequence Generator Design	1+5	Lecture+Lab
5	Review	1+2	Lecture+Lab
6	Mid-term Exam.	3	Lab
7	Experiment III : 4-bit Serial Adder Design	1+5	Lecture+Lab
8	Experiment III : 4-bit Serial Adder Design	3	Lab
9	Review	1+2	Lecture+Lab
10	Final Exam.	3	Lab

ASSESSMENT APPROACH

Assessment method	Percentage %
1. Exercise	**10**
2. Experiment	**30**
3. Mid-term Exam.	**30**
4. Final Exam.	**30**
Total	**100 %**

Guideline for Letter Grade:

Marks	Grade
93 - 100	A+
88 - 92	A
83 - 87	A-
78 - 82	B+
72 - 77	B
68 - 71	B-
63 - 67	C+
58 - 62	C
53 - 57	C-
48 - 52	D+
43 - 47	D
0 - 42	F

Notes:
Exercises are designed to help the students to learn the analyzing and optimizing method of digital circuits and the design ability with PLD. The experiments are graded by comprehensiveness and effectiveness in solving the analyzing and designing problems given and written skill in the reports. All experiments should be finished in laboratory. The experiment reports should be submitted on time and a delay submission will lead to score penalty (50% of their original marks) no matter how many days of their delay.