

2309 SE130 Course Outline

Subject Code : **SE130**
Subject Title : Digital Logic
Level : 2
Credits : 3
Teaching : Lecture 45 hours
Activity :
Prerequisite : N/A

Class Schedule :

| Class | Time | | Classroom | Date |
|-------|------|-------------|-----------|----------------------------|
| D1 | Tue | 15:30-18:20 | C309 | 2023/09/04 - 2023/12/17 |

Instructor : Dr. Xiaonan Fang
Contact :
Number
Email Address : xnfang@must.edu.mo
Office : A307b
Office hours : Mon. 10:00-12:00; Tue. 09:00-12:00;
Wed. 14:30-17:30; Thur. 10:00-12:00

Course Description

This subject aims to make the students familiar with the basic principles, analysis, and design methods of the digital circuit through some practical exercises. Topics including number systems, Boolean algebra, combinational logic circuits, arithmetic functions, sequential logic circuits, and hardware description languages will be conducted and studied.

In the lecture part, the students can understand and learn the principles of number system and Boolean algebra, the analysis and design methods of the combinational logic circuit, arithmetic function, the sequential logic circuit, and hardware description languages.

Typical exercises and assignments are used to help the students understand and practice the circuit analysis and design methods manually.

Textbook(s)

Book title: Logic and Computer Design Fundamentals: International Editions

Author/Editor: M. Morris Mano, Charles R. Kime.

Edition: 5/6

ISBN: 9781292096070

Publisher: Pearson, Prentice Hall

Date: 2015

References

Book title: Digital Design: International Editions

Author/Editor: M. Morris Mano, Michael D. Ciletti.

Edition : 5

ISBN : 9780273764526

Publisher: Pearson, Prentice Hall

Date : 2012

Book title: 數字電子技術基礎

Author: 閻石

Edition: 6

ISBN: 9787040444933

Publisher: 高等教育出版社

Date: 2016

INTENDED LEARNING OUTCOMES

Upon successful completion of this subject, students will be able to:

1. Represent Boolean functions in standard forms, optimize them, and implement them as combinational logic circuits.
2. Analyze the behavior of digital circuits.
3. Construct some typical combinational logic circuits, including various “functional blocks” such as decoders, multiplexers, encoders, and tri-state buffers.
4. Design and implement arithmetic logic circuits.
5. Analyze, design, and implement the sequential circuits.

Schedule

| Index | Topic | Hours | Teaching Method |
|-------|--|-------|-----------------|
| 1 | Digital System and Information (Number System and its operations) | 5 | Lecture |
| 2 | Combinational Logic Circuits Part I: Gate Circuits and Boolean Equations | 4 | Lecture |
| 3 | Combinational Logic Circuits Part II: Circuit Optimization | 5 | Lecture |
| 4 | Combinational Logic Circuits Part III: Additional Gates and Circuits | 3 | Lecture |
| 5 | Combinational Logic Design Part I: Design Procedure. Part II: Combinational Logic | 6 | Lecture |
| 6 | Review | 1 | Lecture |
| 7 | Mid-term Exam. | 3 | |
| 8 | Arithmetic Functions | 4 | Lecture |
| 9 | Sequential Circuits Part I: Storage Elements and Analysis Part II: Sequential Circuit Design | 8 | Lecture |
| 10 | Hardware Description Languages | 3 | Lecture |
| 11 | Review. | 3 | Lecture |

ASSESSMENT APPROACH

| Assessment method | Percentage % |
|--------------------------|--------------|
| 1. Exercise | 10 |
| 2. Assignment | 20 |
| 3. Mid-term Exam. | 30 |
| 4. Final Exam. | 40 |
| Total | 100 % |

Guideline for Letter Grade:

| Marks | Grade |
|----------|-------|
| 93 - 100 | A+ |
| 88 - 92 | A |
| 83 - 87 | A- |
| 78 - 82 | B+ |
| 72 - 77 | B |
| 68 - 71 | B- |
| 63 - 67 | C+ |
| 58 - 62 | C |
| 53 - 57 | C- |
| 48 - 52 | D+ |
| 43 - 47 | D |
| 0 - 42 | F |

Notes:

Exercises are designed to help the students to learn the analyzing and optimizing method of digital circuits. Assignments are graded by comprehensiveness and effectiveness in solving the analyzing and designing problems given. The assignments should be submitted on time and a delayed submission will lead to a score penalty (50% of their original marks) no matter how many days of their delays.