# Baseline Benchmark using NF (Fetch Size) = 4, NI (Instruction Queue Size) = 8, NW = 4 (Issue Limit Per Cycle), NR = 16 (ROB Size), and NB = 4 (CDB Bus Width).

Files	Total Cycles	Total Commit in Thread 1	Total Commit in Thread 2	Stalls due to ROB 1	Stalls due to ROB 2	Stalls due to Reservation Table
1.dat	20	21	0	0	0	11
2.dat	19	15	0	0	0	10
3.dat	64	41	0	0	0	0
4.dat	1213	1416	0	0	0	1202
5.dat	1310	1014	0	0	0	8
1/2.dat	26	21	15	0	0	31
2/1.dat	28	15	21	0	0	35
4/5.dat	1521	1416	1014	0	0	3105
5/4.dat	1524	1014	1416	0	0	924

According to the table below, it seems that when you run 4.dat and 5.dat in a SMT fashion, the order you assigned them will heavily impacts the amount of stalls you receive due to reservation table. However, since we have a big enough Bus Width as well as a ROB, the total amount of cycles isn't heavily impacted.

#### Benchmark using NF (Fetch Size) = 4, NI (Instruction Queue Size) = 8, NW = 2 (Issue Limit Per Cycle), NR = 16 (ROB Size), and NB = 2 (CDB Bus Width).

Files	Total Cycles	Total Commit in Thread 1	Total Commit in Thread 2	Stalls due to ROB 1	Stalls due to ROB 2	Stalls due to Reservation Table
1.dat	25	21	0	0	0	9
2.dat	21	15	0	0	0	8
3.dat	64	41	0	0	0	0

4.dat	1420	1416	0	995	0	12
5.dat	1514	1014	0	0	0	8
1/2.dat	40	21	15	6	5	32
2/1.dat	40	15	21	0	0	23
4/5.dat	2434	1416	1014	1523	1164	157
5/4.dat	3028	1014	1416	0	0	25

Overall, it seems that when you decrease both the issue limit per cycle and the CDB, the total number of cycles went up and the number of stalls due to ROBs being full went up as well. With the number of issues per cycle going down and the CDB bus width going down, it is somewhat expected that the reservation table will receive less stalls since all the stalls are now coming from ROBs. The instructions being committed to the Register File couldn't keep up with the number of items being issued and thus the reason why we see such a high number in stalls due to ROB. Since the ROBs are being stalled, that means the instruction queue will soon hit max capacity and no instructions would be fetched and issued. As a result, we would need more cycles in order to complete the program.

# Benchmark using NF (Fetch Size) = 4, NI (Instruction Queue Size) = 4, NW = 4 (Issue Limit Per Cycle), NR = 16 (ROB Size), and NB = 4 (CDB Bus Width).

Files	Total Cycles	Total Commit in Thread 1	Total Commit in Thread 2	Stalls due to ROB 1	Stalls due to ROB 2	Stalls due to Reservation Table
1.dat	20	21	0	0	0	9
2.dat	19	15	0	0	0	9
3.dat	64	41	0	0	0	0
4.dat	1213	1416	0	0	0	1200
5.dat	1310	1014	0	0	0	8
1/2.dat	26	21	15	0	0	31
2/1.dat	28	15	21	0	0	35
4/5.dat	1521	1416	1014	0	0	2860

5/4.dat	1524	1014	1416	0	0	773

With the Instruction Queue Size going down, the number of stalls due to Reservation Table went down slightly (as compared to benchmark 1). Because the instruction queue is capped out, no further instructions could be fetched and thus it stalls.

# Benchmark using NF (Fetch Size) = 4, NI (Instruction Queue Size) = 10, NW = 4 (Issue Limit Per Cycle), NR = 16 (ROB Size), and NB = 4 (CDB Bus Width).

Files	Total Cycles	Total Commit in Thread 1	Total Commit in Thread 2	Stalls due to ROB 1	Stalls due to ROB 2	Stalls due to Reservation Table
1.dat	20	21	0	0	0	11
2.dat	19	15	0	0	0	10
3.dat	64	41	0	0	0	0
4.dat	1213	1416	0	0	0	1202
5.dat	1310	1014	0	0	0	8
1/2.dat	26	21	15	0	0	31
2/1.dat	28	15	21	0	0	35
4/5.dat	1520	1416	1014	0	0	3109
5/4.dat	1524	1014	1416	0	0	924

With the Instruction Queue Size going up, the number of stalls due to Reservation Table remains the same (as compared to benchmark 1). The Instruction Queue Size really doesn't make much difference given these test files.

# Benchmark using NF (Fetch Size) = 4, NI (Instruction Queue Size) = 10, NW = 4 (Issue Limit Per Cycle), NR = 4 (ROB Size), and NB = 4 (CDB Bus Width).

Files	Total Cycles	Total Commit in Thread 1	Total Commit in Thread 2	Stalls due to ROB 1	Stalls due to ROB 2	Stalls due to Reservation Table
1.dat	23	21	0	19	0	6

2.dat	25	15	0	17	0	4
3.dat	64	41	0	0	0	0
4.dat	1518	1416	0	1509	0	102
5.dat	1819	1014	0	1214	0	4
1/2.dat	30	21	15	14	14	25
2/1.dat	32	15	21	15	23	25
4/5.dat	1903	1416	1014	1568	1542	68
5/4.dat	1908	1014	1416	1243	2176	42

With NR being set to 4, we see more stalls due to the ROB (which is obvious). It is also pretty obvious that because you have more stalls due to ROB, your total cycle count would go up. Please note that this is being compared to the baseline benchmark.

Benchmark using NF (Fetch Size) = 4, NI (Instruction Queue Size) = 10, NW = 4 (Issue Limit Per Cycle), NR = 8 (ROB Size), and NB = 4 (CDB Bus Width).

Files	Total Cycles	Total Commit in Thread 1	Total Commit in Thread 2	Stalls due to ROB 1	Stalls due to ROB 2	Stalls due to Reservation Table
1.dat	20	21	0	6	0	10
2.dat	19	15	0	9	0	8
3.dat	64	41	0	0	0	0
4.dat	1213	1416	0	501	0	1201
5.dat	1314	1014	0	408	0	6
1/2.dat	26	21	15	5	8	32
2/1.dat	28	15	21	9	8	35
4/5.dat	1519	1416	1014	197	259	3004
5/4.dat	1524	1014	1416	250	262	826

With NR being set to 8 and comparing it to NR = 4, the total number of stalls in ROB decreases but the total number of stalls due to the reservation table increases. The cycle count also decreases.

Benchmark using NF (Fetch Size) = 4, NI (Instruction Queue Size) = 10, NW = 4 (Issue Limit Per Cycle), NR = 32 (ROB Size), and NB = 4 (CDB Bus Width).

Files	Total Cycles	Total Commit in Thread 1	Total Commit in Thread 2	Stalls due to ROB 1	Stalls due to ROB 2	Stalls due to Reservation Table
1.dat	20	21	0	6	0	11
2.dat	19	15	0	9	0	10
3.dat	64	41	0	0	0	0
4.dat	1213	1416	0	501	0	1202
5.dat	1310	1014	0	408	0	8
1/2.dat	26	21	15	0	0	32
2/1.dat	28	15	21	0	0	35
4/5.dat	1520	1416	1014	0	0	3109
5/4.dat	1524	1014	1416	0	0	924

With NR being set to 32 and comparing it to NR = 8, the total number of stalls in ROBs decreases to none in SMT architecture. The number of stalls due to reservation table remains the same as compared to NR = 4. The Cycle time remains relatively the same compared to NR = 8 as well. Overall, with bigger ROB size, it seems that the biggest improvement is on the SMT architecture (although the stalls due to reservation table increased).