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Problem Title : Bayesian Optimization for Analog Circuit Sizing and Performance Estimation

Problem Description: This project aims to use **Bayesian Optimization (BO)** to optimize transistor sizing and bias conditions in an **operational amplifier (OpAmp)** circuit. The goal is to efficiently find the best design parameters that maximize **gain** while minimizing **power consumption**, reducing reliance on expensive brute-force simulations. I will also be utilizing different surrogate models like **GP, NN** to speed up the evaluation process.

Current evaluation methods involve manual inputs or exhaustive grid searches to find an optimized parameter which is very cost ineffective. I will use **BO** to optimize the circuits with fewer simulations. **Surrogate models** will further reduce the number of simulations needed while maintaining accuracy.

How does this relate to the course material? : This project idea has been built on inspiration from the sample " BO in chip design idea" and uses BO, the main topic of this course to optimize the circuit size. It perfectly aligns with my interests of integrating Machine Learning in VLSI, a grad school research area I am interested in.

Evaluation Criteria:

1) **Optimization efficiency** - Number of SPICE simulations needed to reach optimal design. Naturally, we expect BO to have fewer simulations than grid design/random searches.
2) **Circuit Performance**: Achieve gain-power tradeoff compared to baseline methods. Success if BO outperforms or matches best grid search result with fewer iterations.
3) **Generalization**: Apply BO to another OpAmp and check if BO works effectively on other circuits as well.
4) **Surrogate Model Accuracy**: Compare GP/BNN predictions against actual SPICE results. If the surrogate model accurately predicts circuit performance with low error, success.

Subtasks:

1) Simulate a **two-stage CMOS operational amplifier** as the test circuit using LTSpice. I have never used this technology before, but will be learning it for this project.
2) The input parameters are transistor widths, lengths, bias currents and capacitor values.
3) The optimization targets are maximizing the gain, minimizing power consumption and maintaining a bandwidth threshold.
4) Test this on the baseline methods and then using BO.
5) Train the surrogate model to predict the performance values and then compare them with the actual SPICE values.

Note: I brainstormed with ChatGPT. I am fairly new to VLSI, but I am fairly certain that I will succeed in this project.