SYSC 4101A
Lab 7
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Exercise 1
Question 1

$TS_s = [T_1, T_4, T_6]$

	Steps in test path		
	T_1	T_4	T_6
Source state	Ø	X	Y
Input	a	a	b
Output	0	0	1
Destination state	X	Y	Z

Question 2

$TS_T = [T_1, T_2, T_5, T_6, T_{10}, T_7, T_3, T_9, T_8, T_4]$

	Steps in test path									
	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9	T_{10}
Source state	Ø	X	Y	X	Y	Y	Z	Z	X	Z
Input	a	b	a	a	c	b	c	b	c	a
Output	0	1	1	0	1	1	0	0	0	1
Destination state	X	Y	X	Y	Y	Z	Y	X	Z	Z

Question 3

TS_{TT} :
$TS_{TT1} = [T_1, T_2, T_5]$
$TS_{TT2} = [T_1, T_2, T_3]$
$TS_{TT3} = [T_1, T_2, T_6]$
$TS_{TT4} = [T_1, T_4, T_6]$
$TS_{TT5} = [T_1, T_4, T_3]$
$TS_{TT6} = [T_1, T_4, T_5]$
$TS_{TT7} = [T_1, T_9, T_7]$
$TS_{TT7} = [T_1, T_9, T_8]$
$TS_{TT9} = [T_1, T_9, T_{10}]$

TS_{TT1}	**Steps in test path**		
	T_1	T_2	T_5
Source state	Ø	X	Y
Input	a	b	c
Output	0	1	1
Destination state	X	Y	Y

TS_{TT2}	**Steps in test path**		
	T_1	T_2	T_3
Source state	Ø	X	Y
Input	a	b	a
Output	0	1	1
Destination state	X	Y	X

TS_{TT3}	**Steps in test path**		
	T_1	T_2	T_6
Source state	Ø	X	Y
Input	a	b	b
Output	0	1	1
Destination state	X	Y	Z

TS_{TT4}	**Steps in test path**		
	T_1	T_4	T_6
Source state	Ø	X	Y
Input	a	a	b
Output	0	0	1
Destination state	X	Y	Z

TS_{TT5}	**Steps in test path**		
	T_1	T_4	T_3
Source state	Ø	X	Y
Input	a	a	a
Output	0	0	1
Destination state	X	Y	X

TS_{TT6}	**Steps in test path**		
	T_1	T_4	T_5
Source state	Ø	X	Y
Input	a	a	c
Output	0	0	1
Destination state	X	Y	Y

TS_{TT7}	**Steps in test path**		
	T_1	T_9	T_7
Source state	Ø	X	Z
Input	a	c	c
Output	0	0	0
Destination state	X	Z	Y

TS_{TT8}	**Steps in test path**		
	T_1	T_9	T_8
Source state	Ø	X	Z
Input	a	c	b
Output	0	0	0
Destination state	X	Z	X

TS_{TT9}	**Steps in test path**		
	T_1	T_9	T_{10}
Source state	Ø	X	Z
Input	a	c	a
Output	0	0	1
Destination state	X	Z	Z

Exercise 2

Question 1

My TS_s = $[T_1, T_4, T_6]$ does not reveal this fault as mine transitions from state Y to state Z and the fault is transitioning from state Z to state Y.

Question 2

My TS_T = $[T_1, T_2, T_5, T_6, T_{10}, T_7, T_3, T_9, T_8, T_4]$ does reveal this fault as T_{10} and T_7 would be doing the same transition. My test suite goes directly from state Z to state Z using T_{10} and outputting 1, then goes from state Z to state Y using T_7 and outputting 0. Because the code implements T_{10} and T_7 as the same transition from state Z to state Y, my test path will expect output 1 when running T_{10} and then be able to run T_7 or T_8, but it cannot as T_{10} and T_7 both transition to the state Y result in the next T_3 to give a fault.

Question 3

My TS_{TT7} will not reveal the fault as the test paths are too short. While running tests, you are judging the correctness of the system based on the outputs. Since T_{10} and T_7 give the correct outputs but end up in the wrong states and have no transitions afterward, there is no way to tell if the system is in the correct state based on how short the paths are.

Exercise 3

Question 1

My TS_s = $[T_1, T_4, T_6]$ would not detect the fault as it would not be in state Z and receive an input of c as it ends at state Z coming from Y.

Question 2

My TS_T = $[T_1, T_2, T_5, T_6, T_{10}, T_7, T_3, T_9, T_8, T_4]$ will not detect the fault because when it tries to run T_8, although it will now transition to state T, it will still run transition T_4 with input a and output 1, but it will remain in state T. Since the test path ends there, it will not detect that it is in the wrong state as the input values resulted in the correct output values.

Question 3

My TS_{TT} will not detect the fault as all the paths will result in the same output given the same input.

Exercise 4

	Steps in test path									
	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9	T_{10}
Source state	Ø	X	Y	X	Y	Y	Z	Z	X	Z
Input	a	b	a	a	c	b	c	b	c	a
Output	0	1	1	0	1	1	0	0	0	1
Destination state	X	Y	X	Y	Y	Z	Y	X	Z	Z

Based on the above table, {a} is not a characterization sequence as the output while in state Y and Z when given a as input will both result in 1. {b} is not a characterization sequence either as the output while in state X and Y with input b will also both give 1. {b, a} is not a characterization sequence either as the output while in state X or Z with input b then input a will result in 1 then 1 respectively. However, {a, b} is a characterization sequence as no states that are given input a then input b result in the same input.

Exercise 5

Question 1

TS_s = $[T_1, T_4, T_6, T_{10}, T_8]$

My test suite will detect the fault as T_{10} is now the same as T_7, so instead of transitioning back to Z, it transitions to Y. The old output would be 1 then 0, but now the output will be 1 then 1, revealing the fault.

Question 2

TS_T = [$T_1, T_2, T_5, T_6, T_{10}, T_7, T_3, T_9, T_8, T_4, T_3, T_2$]

My test suite will still detect the fault as it detects it when transitioning from $T_{10}\ to\ T_7$. It will be the exact same as Exercise 2 as the program will break and detect the fault before it gets to the appended {a, b} input transitions.

Question 3

TS_{TT} :
TS_{TT1} = [T_1, T_2, T_5, T_3, T_2]
TS_{TT2} = [T_1, T_2, T_3, T_4, T_6]
TS_{TT3} = [$T_1, T_2, T_6, T_{10}, T_8$]
TS_{TT4} = [$T_1, T_4, T_6, T_{10}, T_8$]
TS_{TT5} = [T_1, T_4, T_3, T_4, T_6]
TS_{TT6} = [T_1, T_4, T_5, T_3, T_2]
TS_{TT7} = [T_1, T_9, T_7, T_3, T_2]
TS_{TT7} = [T_1, T_9, T_8, T_4, T_6]
TS_{TT9} = [$T_1, T_9, T_{10}, T_{10}, T_8$]

My test suite will detect the fault as TS_{TT3} for example will receive the correct output 1 with input a on transition T_{10}. However, when given input b, it will expect 0 as the output as it expects to be coming from state Z, but it will return 1 as it is coming from state Y instead.

Exercise 6

For all parts in Exercise 6, T_8 now goes from state Z to state T.

Question 1

TS_s = [$T_1, T_4, T_6, T_{10}, T_8$]

My test suite will not detect the fault as the outputs would be the same as the original. If we added inputs {a, b, c} in addition to the added {a, b}, it would detect the fault.

Question 2

TS_T = [$T_1, T_2, T_5, T_6, T_{10}, T_7, T_3, T_9, T_8, T_4, T_3, T_2$]

My suite will detect the fault on the transition from T_4 to T_3 as at this point it will be in state T. When a is passed, it should be in state Y and expect 1 as the output, but since it is in state T, it outputs 0, revealing the fault.

Question 3

TS_{TT} :
TS_{TT1} = $[T_1, T_2, T_5, T_3, T_2]$
TS_{TT2} = $[T_1, T_2, T_3, T_4, T_6]$
TS_{TT3} = $[T_1, T_2, T_6, T_{10}, T_8]$
TS_{TT4} = $[T_1, T_4, T_6, T_{10}, T_8]$
TS_{TT5} = $[T_1, T_4, T_3, T_4, T_6]$
TS_{TT6} = $[T_1, T_4, T_5, T_3, T_2]$
TS_{TT7} = $[T_1, T_9, T_7, T_3, T_2]$
TS_{TT7} = $[T_1, T_9, T_8, T_4, T_6]$
TS_{TT9} = $[T_1, T_9, T_{10}, T_{10}, T_8]$

My test suite will not detect the fault as we need to run a test path that runs through transition T_8 as at that point it will be in state T. Since none of them have any input past T_8, the program finishes at state T.