library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.NUMERIC\_STD.ALL;

entity BIN\_2\_DEC is

Port (

A : in STD\_LOGIC\_VECTOR (4 downto 0);

SEG\_0 : out STD\_LOGIC\_VECTOR (3 downto 0);

SEG\_1 : out STD\_LOGIC\_VECTOR (3 downto 0)

);

end BIN\_2\_DEC;

architecture BIN\_2\_DEC\_arch of BIN\_2\_DEC is

begin

SEG\_0 <=std\_logic\_vector(to\_unsigned(to\_integer(unsigned(A)) mod 10,4));

SEG\_1 <=std\_logic\_vector(to\_unsigned((to\_integer(unsigned(A))-(to\_integer(unsigned(A)) mod 10))/10,4));

end BIN\_2\_DEC\_arch;