library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity CompletLab4 is

Port (

SEL : in STD\_LOGIC;

A : in STD\_LOGIC\_VECTOR (4 downto 0);

CLK : IN STD\_LOGIC;

AN : OUT STD\_LOGIC\_VECTOR(7 downto 0);

CA : OUT STD\_LOGIC;

CB : OUT STD\_LOGIC;

CC : OUT STD\_LOGIC;

CD : OUT STD\_LOGIC;

CE : OUT STD\_LOGIC;

CF : OUT STD\_LOGIC;

CG : OUT STD\_LOGIC;

DP : OUT STD\_LOGIC

);

end CompletLab4;

architecture Complet\_arch of CompletLab4 is

signal S\_MOD : STD\_LOGIC\_VECTOR (4 downto 0);

signal S\_MULT : STD\_LOGIC\_VECTOR (4 downto 0);

signal S\_MUX : STD\_LOGIC\_VECTOR (4 downto 0);

signal S\_UNITE : STD\_LOGIC\_VECTOR (3 downto 0);

signal S\_DIZAINE : STD\_LOGIC\_VECTOR (3 downto 0);

component MOD\_5

port(

A : in STD\_LOGIC\_VECTOR (4 downto 0);

S : out STD\_LOGIC\_VECTOR (4 downto 0)

);

end component;

component MULT\_2

port(

A : in STD\_LOGIC\_VECTOR (4 downto 0);

S : out STD\_LOGIC\_VECTOR (4 downto 0)

);

end component;

component MUX\_2\_1

port(

A : in STD\_LOGIC\_VECTOR (4 downto 0);

B : in STD\_LOGIC\_VECTOR (4 downto 0);

SEL : in STD\_LOGIC;

S : out STD\_LOGIC\_VECTOR (4 downto 0)

);

end component;

component BIN\_2\_DEC

port(

A : in STD\_LOGIC\_VECTOR (4 downto 0);

SEG\_0 : out STD\_LOGIC\_VECTOR (3 downto 0);

SEG\_1 : out STD\_LOGIC\_VECTOR (3 downto 0)

);

end component;

component DISP\_7\_SEG\_LAB4

port(

SEG\_0 : in STD\_LOGIC\_VECTOR (3 downto 0);

SEG\_1 : in STD\_LOGIC\_VECTOR (3 downto 0);

CLK : IN STD\_LOGIC;

AN : OUT STD\_LOGIC\_VECTOR (7 downto 0);

CA : OUT STD\_LOGIC;

CB : OUT STD\_LOGIC;

CC : OUT STD\_LOGIC;

CD : OUT STD\_LOGIC;

CE : OUT STD\_LOGIC;

CF : OUT STD\_LOGIC;

CG : OUT STD\_LOGIC;

DP : OUT STD\_LOGIC

);

end component;

begin

U0 :

MOD\_5 port map(

A=>A,

S=>S\_MOD

);

U1 :

MULT\_2 port map(

A=>A,

S=>S\_MULT

);

U2 :

MUX\_2\_1 port map(

A=>S\_MOD,

B=>S\_MULT,

SEL=>SEL,

S=>S\_MUX

);

U3 :

BIN\_2\_DEC port map(

A=>S\_MUX,

SEG\_0=>S\_UNITE,

SEG\_1=>S\_DIZAINE

);

U4 :

DISP\_7\_SEG\_LAB4 port map(

SEG\_0=>S\_UNITE,

SEG\_1=>S\_DIZAINE,

CLK=>CLK,

AN=>AN,

CA=>CA,

CB=>CB,

CC=>CC,

CD=>CD,

CE=>CE,

CF=>CF,

CG=>CG,

DP=>DP

);