library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.NUMERIC\_STD.all;

use IEEE.STD\_LOGIC\_ARITH.all;

use IEEE.STD\_LOGIC\_UNSIGNED.all;

entity MOD\_5 is

Port (

A : in STD\_LOGIC\_VECTOR (4 downto 0);

S : out STD\_LOGIC\_VECTOR (4 downto 0)

);

end MOD\_5;

architecture MOD\_5\_arch of MOD\_5 is

begin

with A select

S <= "00001" when "00001" | "00110" | "01011" | "10000" | "10101" | "11010" | "11111",

"00010" when "00010" | "00111" | "01100" | "10001" | "10110" | "11011",

"00011" when "00011" | "01000" | "01101" | "10010" | "10111" | "11100",

"00100" when "00100" | "01001" | "01110" | "10011" | "11000" | "11101",

"00000" when others;

end MOD\_5\_arch;