library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity MULT\_2 is

Port (

A : in STD\_LOGIC\_VECTOR (4 downto 0);

S : out STD\_LOGIC\_VECTOR (4 downto 0)

);

end MULT\_2;

architecture MULT\_2\_arch of MULT\_2 is

begin

S(0)<='0';

S(1)<=A(0);

S(2)<=A(1);

S(3)<=A(2);

S(4)<=A(3);

end MULT\_2\_arch;