library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity MUX\_2\_1 is

Port (

A : in STD\_LOGIC\_VECTOR (4 downto 0);

B : in STD\_LOGIC\_VECTOR (4 downto 0);

SEL : in STD\_LOGIC;

S : out STD\_LOGIC\_VECTOR (4 downto 0)

);

end MUX\_2\_1;

architecture MUX\_2\_1\_arch of MUX\_2\_1 is

begin

with SEL select

S <= A when '0',

B when others;

end MUX\_2\_1\_arch;