library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

entity CompletFeu is

Port (

CLK : IN STD\_LOGIC;

RST : IN STD\_LOGIC;

START : IN STD\_LOGIC;

AN : OUT STD\_LOGIC\_VECTOR(7 downto 0);

CA : OUT STD\_LOGIC;

CB : OUT STD\_LOGIC;

CC : OUT STD\_LOGIC;

CD : OUT STD\_LOGIC;

CE : OUT STD\_LOGIC;

CF : OUT STD\_LOGIC;

CG : OUT STD\_LOGIC;

DP : OUT STD\_LOGIC

);

end CompletFeu;

architecture Behavioral of CompletFeu is

signal S0\_DEBOUNCE : STD\_LOGIC;

signal S1\_DEBOUNCE : STD\_LOGIC;

signal S\_PULSE : STD\_LOGIC;

signal S0\_TRAFIC : STD\_LOGIC\_VECTOR (7 downto 0);

signal S1\_TRAFIC : STD\_LOGIC\_VECTOR (7 downto 0);

signal S2\_TRAFIC : STD\_LOGIC\_VECTOR (7 downto 0);

signal S3\_TRAFIC : STD\_LOGIC\_VECTOR (7 downto 0);

signal S4\_TRAFIC : STD\_LOGIC\_VECTOR (7 downto 0);

signal S5\_TRAFIC : STD\_LOGIC\_VECTOR (7 downto 0);

signal S6\_TRAFIC : STD\_LOGIC\_VECTOR (7 downto 0);

signal S7\_TRAFIC : STD\_LOGIC\_VECTOR (7 downto 0);

component DEBOUNCE

GENERIC(

counter\_size : INTEGER := 19); --counter size (19 bits gives 10.5ms with 50MHz clock)

PORT(

CLK : IN STD\_LOGIC; --input clock

BUTTON : IN STD\_LOGIC; --input signal to be debounced

RESULT : OUT STD\_LOGIC); --debounced signal

end component;

component PULSE\_GEN

port(

CLK: in STD\_LOGIC;

RST: in STD\_LOGIC;

VIN: in STD\_LOGIC;

VOUT: out STD\_LOGIC

);

end component;

component TRAFIC\_LIGHT

port(

CLK : IN STD\_LOGIC;

RST : IN STD\_LOGIC;

START : IN STD\_LOGIC;

SEG\_0 : OUT STD\_LOGIC\_VECTOR (7 DOWNTO 0);

SEG\_1 : OUT STD\_LOGIC\_VECTOR (7 DOWNTO 0);

SEG\_2 : OUT STD\_LOGIC\_VECTOR (7 DOWNTO 0);

SEG\_3 : OUT STD\_LOGIC\_VECTOR (7 DOWNTO 0);

SEG\_4 : OUT STD\_LOGIC\_VECTOR (7 DOWNTO 0);

SEG\_5 : OUT STD\_LOGIC\_VECTOR (7 DOWNTO 0);

SEG\_6 : OUT STD\_LOGIC\_VECTOR (7 DOWNTO 0);

SEG\_7 : OUT STD\_LOGIC\_VECTOR (7 DOWNTO 0)

);

end component;

component DISP\_7SEG

port(

SEG\_0 : IN STD\_LOGIC\_VECTOR(7 DOWNTO 0);

SEG\_1 : IN STD\_LOGIC\_VECTOR(7 DOWNTO 0);

SEG\_2 : IN STD\_LOGIC\_VECTOR(7 DOWNTO 0);

SEG\_3 : IN STD\_LOGIC\_VECTOR(7 DOWNTO 0);

SEG\_4 : IN STD\_LOGIC\_VECTOR(7 DOWNTO 0);

SEG\_5 : IN STD\_LOGIC\_VECTOR(7 DOWNTO 0);

SEG\_6 : IN STD\_LOGIC\_VECTOR(7 DOWNTO 0);

SEG\_7 : IN STD\_LOGIC\_VECTOR(7 DOWNTO 0);

CLK : IN STD\_LOGIC;

AN : OUT STD\_LOGIC\_VECTOR(7 DOWNTO 0);

CA : OUT STD\_LOGIC;

CB : OUT STD\_LOGIC;

CC : OUT STD\_LOGIC;

CD : OUT STD\_LOGIC;

CE : OUT STD\_LOGIC;

CF : OUT STD\_LOGIC;

CG : OUT STD\_LOGIC;

DP : OUT STD\_LOGIC

);

end component;

begin

U0 :

DEBOUNCE port map(

CLK => CLK,

BUTTON => RST,

RESULT => S0\_DEBOUNCE

);

U1 :

DEBOUNCE port map(

CLK => CLK,

BUTTON => START,

RESULT => S1\_DEBOUNCE

);

U2 :

PULSE\_GEN port map(

CLK => CLK,

RST => S0\_DEBOUNCE,

VIN => S1\_DEBOUNCE,

VOUT => S\_PULSE

);

U3 :

TRAFIC\_LIGHT port map(

CLK => CLK,

RST => S0\_DEBOUNCE,

START => S\_PULSE,

SEG\_0 => S0\_TRAFIC,

SEG\_1 => S1\_TRAFIC,

SEG\_2 => S2\_TRAFIC,

SEG\_3 => S3\_TRAFIC,

SEG\_4 => S4\_TRAFIC,

SEG\_5 => S5\_TRAFIC,

SEG\_6 => S6\_TRAFIC,

SEG\_7 => S7\_TRAFIC

);

U4 :

DISP\_7SEG port map(

SEG\_0 => S0\_TRAFIC,

SEG\_1 => S1\_TRAFIC,

SEG\_2 => S2\_TRAFIC,

SEG\_3 => S3\_TRAFIC,

SEG\_4 => S4\_TRAFIC,

SEG\_5 => S5\_TRAFIC,

SEG\_6 => S6\_TRAFIC,

SEG\_7 => S7\_TRAFIC,

CLK => CLK,

AN => AN,

CA => CA,

CB => CB,

CC => CC,

CD => CD,

CE => CE,

CF => CF,

CG => CG,

DP => DP

);

end Behavioral;