LIBRARY IEEE;

USE IEEE.STD\_LOGIC\_1164.ALL;

ENTITY PULSE\_GEN IS

port(CLK: in STD\_LOGIC;

RST: in STD\_LOGIC;

VIN: in STD\_LOGIC;

VOUT: out STD\_LOGIC);

END PULSE\_GEN;

ARCHITECTURE BEHAVE OF PULSE\_GEN IS

TYPE STATE IS (IDLE, PULSE, FILTER);

SIGNAL CSTATE: STATE := IDLE;

BEGIN

SEQ\_PROC: PROCESS(CLK, RST)

BEGIN

IF(RST = '1') THEN

CSTATE <= IDLE;

ELSIF(RISING\_EDGE(CLK)) THEN

CASE CSTATE is

when IDLE =>

VOUT <= '0';

IF(VIN = '1') THEN

CSTATE <= PULSE;

END IF;

when PULSE =>

VOUT <= '1';

IF(VIN = '1') THEN

CSTATE <= FILTER;

ELSE

CSTATE <= IDLE;

END IF;

when FILTER =>

VOUT <= '0';

IF(VIN = '0') THEN

CSTATE <= IDLE;

END IF;

WHEN OTHERS =>

VOUT <= '0';

CSTATE <= IDLE;

END CASE;

END IF;

END process;

END BEHAVE;