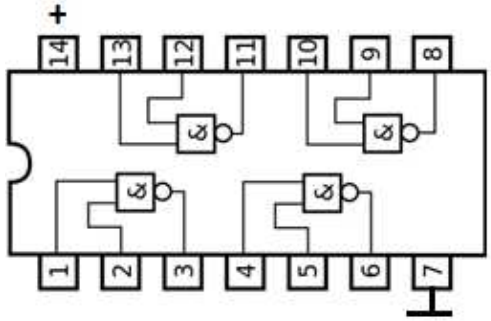
BROCHAGE des CIRCUITS INTEGRES TTL – PeiP 1

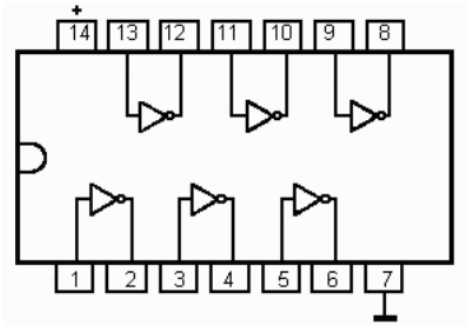
7400 $Y = \overline{AB}$

4 x NAND 2 entrées



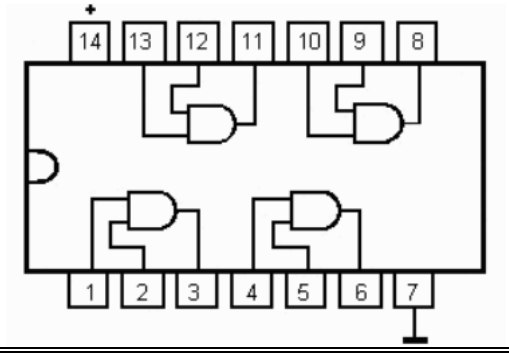
7404 $Y = \bar{A}$

6 x INVERSEURS



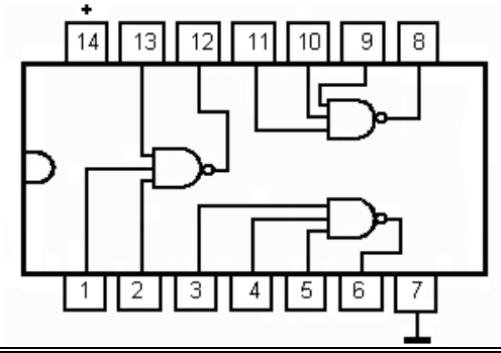
7408 $Y = AB$

4 x AND 2 entrées



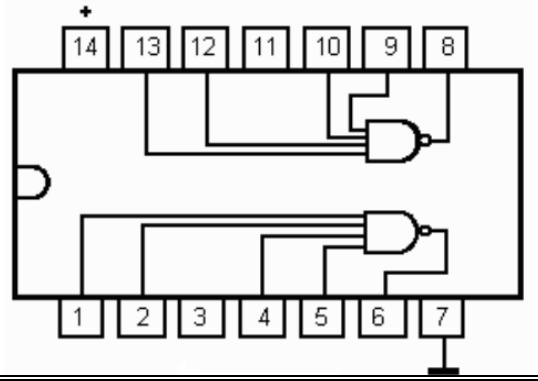
7410 $Y = \overline{ABC}$

3 x NAND 3 entrées



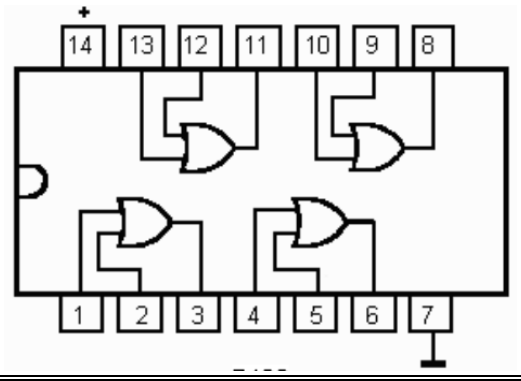
7420 $Y = \overline{ABCD}$

2 x NAND 4 entrées



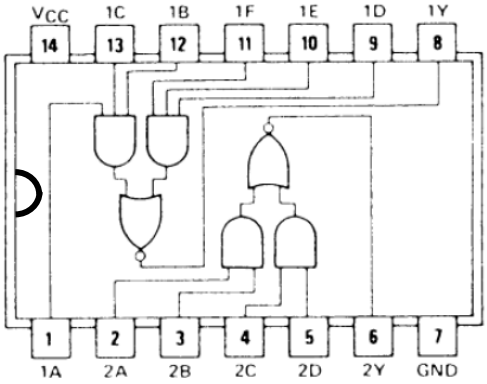
7432 $Y = A + B$

4 x OR 2 entrées



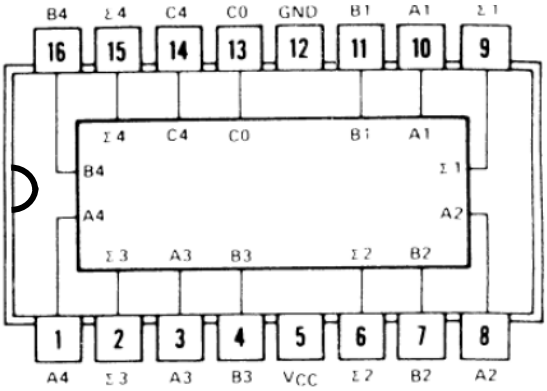
7451 $1Y = \overline{AB + CD}$

2 x NAND 4 entrées



7483

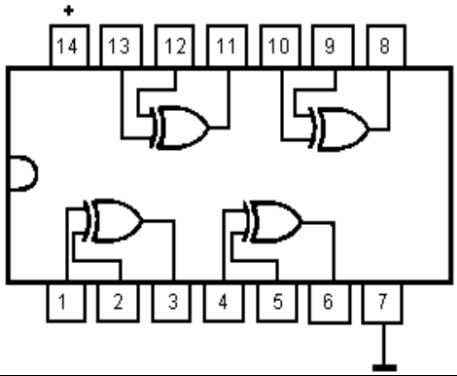
Additionneur 4 bits



BROCHAGE des CIRCUITS INTEGRES TTL – PeiP 1

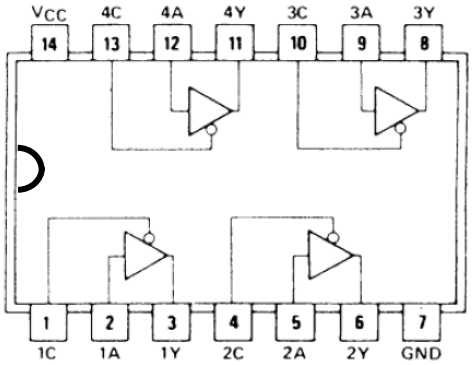
7486 $Y = A \oplus B$

4 x XOR 2 entrées



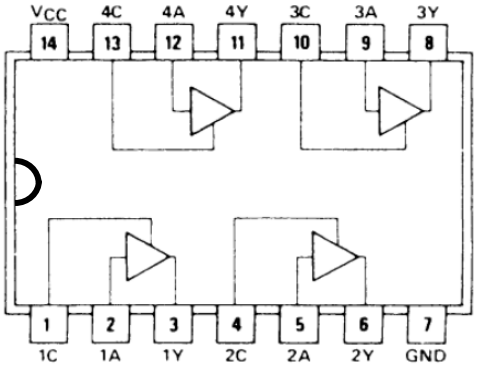
74125 *$Y = A$ lorsque C=0*

4 x buffers trois états (tristates)



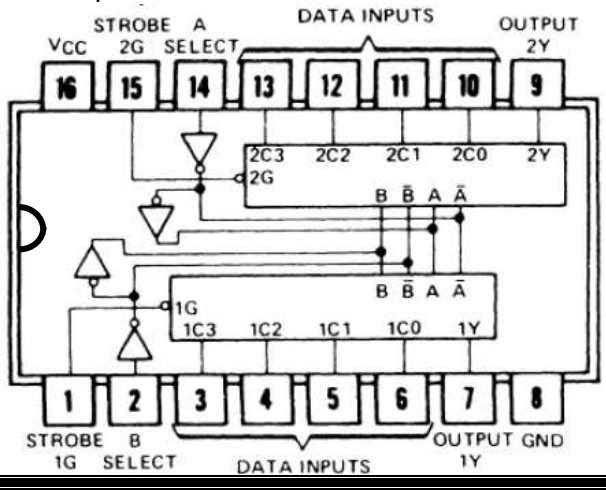
74126 *$Y = A$ lorsque C=1*

4 x buffers trois états (tristates)



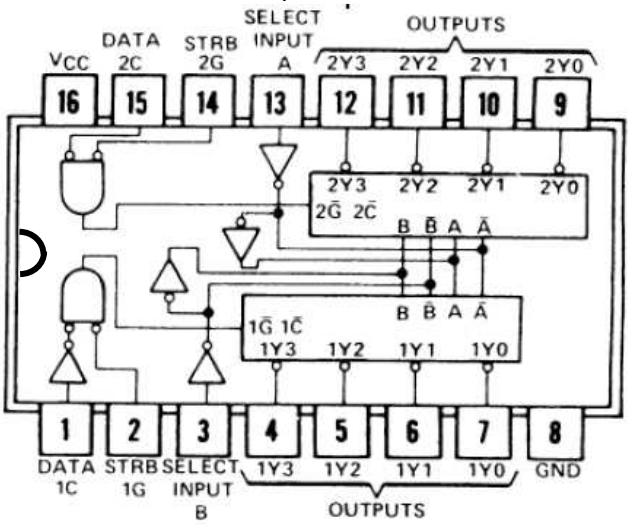
74153

2 x multiplexeurs 4→1



74155

2 x décodeurs/démultiplexeurs 1→4



74157

2 x multiplexeurs 2→1