Ryerson University

Department of Electrical & Computer Engineering
Faculty of Engineering & Architectural Science

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Semester/Year (e.g. F2016)	**W2024**

Instructor:	**Prof. Fei Yuan**

Assignment/Lab Number:	**Project**
Assignment/Lab Title:	**Amplifier Design Project**

Submission Date:	**April 6, 2024**
Due Date:	**April 7, 2024**

Student LAST Name	Student FIRST Name	Student Number	Section	Signature*
Recto	**Nathaniel**	**501162644**	**16**	Nathaniel

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Introduction:

The report for the amplifier design project is presented here. This design project gathers all of the course material on Bipolar Junction Transistors (BJT), testing a multi-stage amplifier that can meet a set of requirements. The appendix contains all hand calculations, and the circuit was analyzed using Multisim.

Objectives:

The main purpose of this design project is to design and construct a BJT amplifier with these specific requirements below:

- Power supply: +10 V relative to the ground;
- Quiescent current drawn from the power supply: no larger than 10 mA;
- No-load voltage gain (at 1 kHz): |Avo| = 50 (± 10%);
- Maximum no-load output voltage swing (at 1 kHz): no smaller than 8 V peak to peak;
- Loaded voltage gain (at 1 kHz and with RL = 1 kΩ): no smaller than 90% of the no-load voltage gain;
- Maximum loaded output voltage swing (at 1 kHz and RL = 1 kΩ): no smaller than 4 V peak to peak;
- Input resistance (at 1 kHz): no smaller than 20 kΩ;
- Amplifier type: inverting or non-inverting;
- Frequency response: 20 Hz to 50 kHz (−3dB response);
- Type of transistors: BJT;
- Number of transistors (stages): no more than 3;
- Resistances permitted: values smaller than 220 kΩ from the E24 series;
- Capacitors permitted: 0. 1 μF, 1. 0 μF, 2. 2 μF, 4. 7 μF, 10 μF, 47 μF, 100 μF, 220 μF;
- Other components (BJTs, diodes, Zener diodes, etc.): only from your ELE404 lab kit;
- The output voltage must be free from distortions (clipping, etc.) under all test conditions'
- The source resistance, Rs, must be 600Ω under all test conditions;

Graphs:

I have created 2 characteristic graphs and load lines for each of them. The graphs plot the collector current that passed through the BJT against the collector to emitter voltage drop. These graphs were created by a testing circuit that was designed and using DC sweep analysis in Multisim.

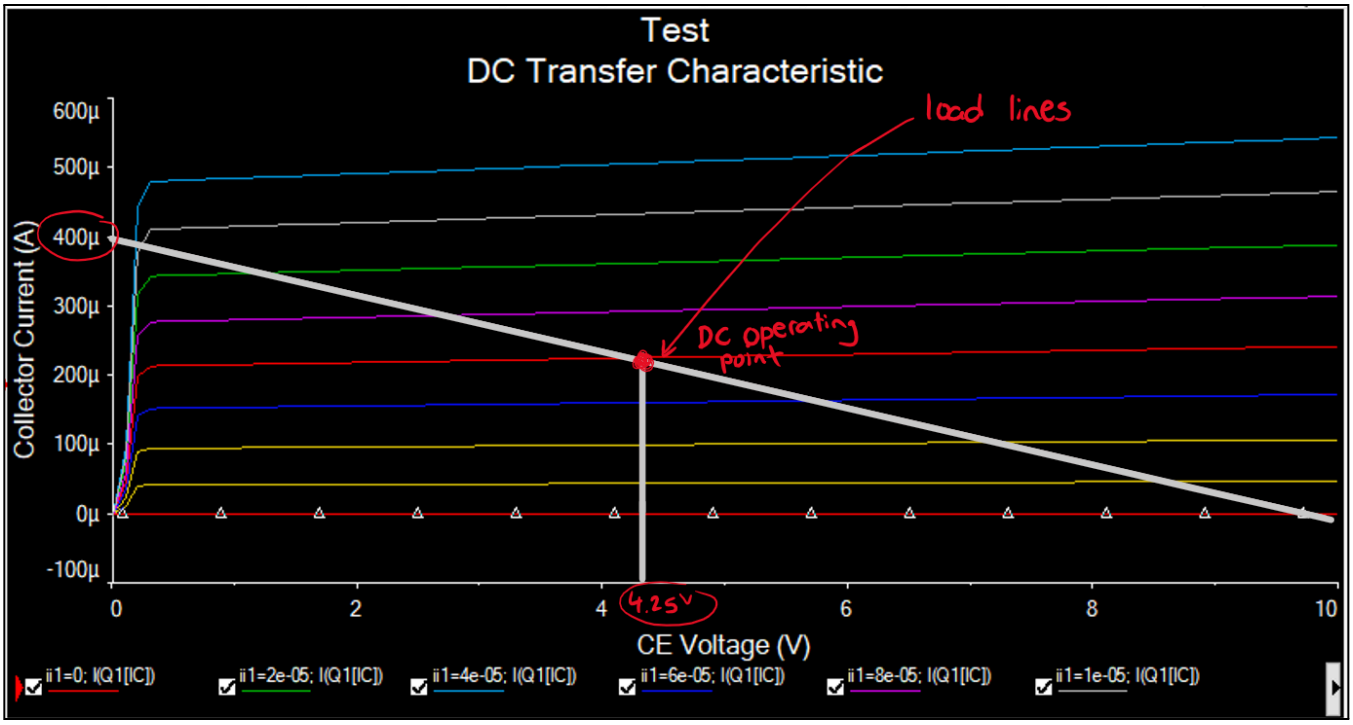


Figure 1: DC Characteristic Graph of CE 2N3904 BJT with a load line.

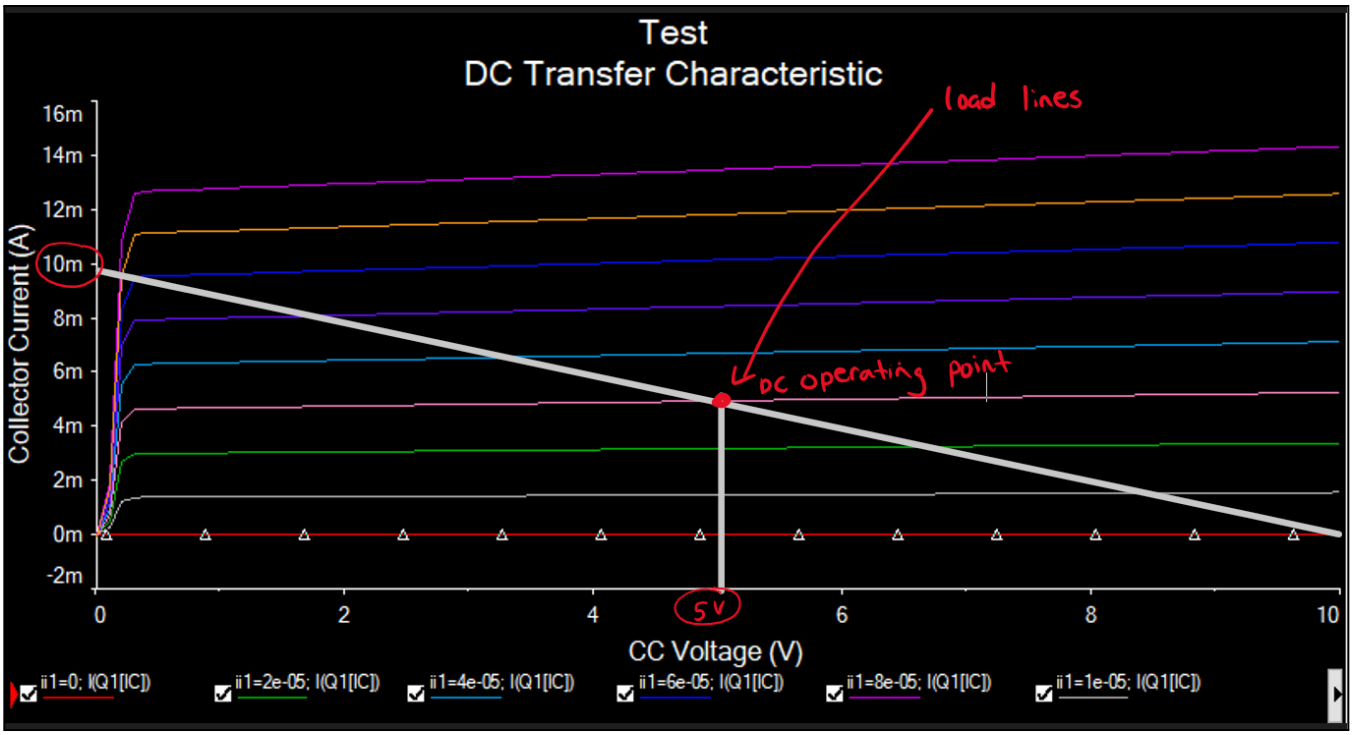


Figure 2: DC Characteristic Graph of CC 2N3904 BJT with a load line.

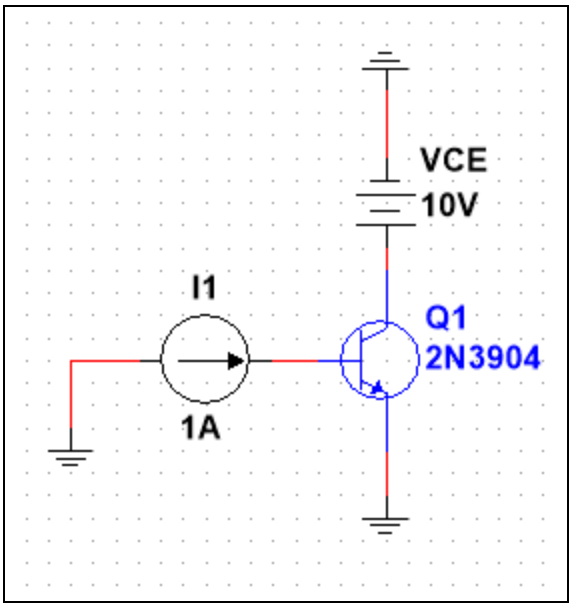


Figure 3: circuit for BJT characteristic graph.

Calculation and Analysis:

All of these values are referenced from the manual calculations, through the Appendix section.

Table P1: Biasing Resistor Values

R_1	R_2	R_3	R_4	R_5	R_6
91 kΩ	68 kΩ	91 kΩ	68 kΩ	91 kΩ	200 kΩ

Table P2: Collector and Emitter Resistor Values

R_{C1}	R_{E1}	R_{C2}	R_{E2}	R_{E3}	R_{E4}	R_{E5}	R_L
15 kΩ	15 kΩ	13 kΩ	1.5 kΩ	15kΩ	1.3kΩ	1 kΩ	1kΩ

Table P3: Critical Values of CE (Stage 1 & 2)

I_B	$I_{B,DC}$	I_C	β	V_B	g_m
3.5 µA	2 µA	400 µA	114.3	4.25 V	0.0154 S

Table P4: Critical Values of CC (Stage 3)

I_B	$I_{B,DC}$	I_C	β	V_B	g_m
65 mA	30 µA	10 mA	153.8	5 V	0.385 S

Table P5: Capacitor Values

C_1	C_2	C_3	C_4	C_5	C_6
10µF	100µF	10µF	100µF	10µF	100µF

Process for Design:

To get a 50 dB gain with Rin ≥ 20 kΩ, a 3-stage amplifier was selected. One CC (common collector) stage and two CE (common emitter) stages are incorporated in the design. In order to make the computations simpler, I calculated the square root of 50, which is around 7.1. If I were to multiply the gains from stages 1 and 2, making them equal to -7.1 each, the result would be roughly 50. The third stage's gain will be around one because the final step is a CC. Because stages 1 and 2 have equal gains, this guarantees that the voltage gain may be around 50V/V and that neither will affect the other's working conditions. The testing circuit was simulated in Multisim (Figure 3) using DC sweep to produce the characteristic graph, which allowed the further calculations to begin. Due to the limited power supply current constraint, a load line was manually built and a low collector current of 400 μA was selected for both CEs. Also, this was done for the CC stage. The manual computations began with the selection of an operational point based on the graphs. The calculations were performed starting at the final stage (CC) and working its way backward to the first stage. The CC emitter resistor was selected in order to guarantee that there would be no noticeable changes when the load (RL) is added or withdrawn, as RL was needed to be 1 kΩ. From this point on, the CC's input resistance was determined and utilized in the CE stage 2 calculations. By assuming that one of the biasing resistors is sufficiently large to cause the divider current to be noticeably bigger than the base current, and then using KCL at the node to solve for the other resistor, the biasing resistors for each step were determined. This KCL calculation uses the base current, voltage, and DC operating point current from the graphs. The same calculation process was done in stage 1 using the input resistance of the second stage since the gains of stages 1 and 2 were made equal.

The selection of resistors varied based on the specific area. First, the current and the next stage input resistance were used to determine the emitter and collector resistors. The emitter resistor of the CC stage, RE5 = 1 kΩ, was considered to have a resistance that would not significantly affect the circuit's loading effect when the load is added or eliminated. Second, the amount of required gain for each stage was taken into consideration while selecting the emitter degeneration resistors. Since RE equaled the parallel combination of the emitter resistor and emitter degeneration resistor, it was possible to solve for it by rearranging the gain equation. Finally, in order to ensure sufficient current, the remaining biasing resistors were selected to be as big as possible. There would be a huge loading impact on the circuit if the biasing resistors were too small since the input resistance would drop dramatically.

The assumptions for each capacitor were tested by calculations. The values of the capacitors would vary based on the location and operating frequency. Since the input resistances of the amplifier stages are mainly large, C1, C3, and C5 were all 10 μF coupling capacitors. This is because a major change in resistance would be required to significantly change the overall circuit characteristic. On the other hand, since C2, C4, and C6 have been connected to the emitter degeneration resistors, they all have a value of 100 μF. Because little adjustments to the emitter degeneration resistor can have a significant impact on the gain, a high capacitance is required to guarantee that resistance does not fluctuate substantially.

Circuit Under Test:

Figure 4 depicts the design of a three-stage BJT amplifier. There are six electrolytic capacitors, fourteen resistors, and three 2N3904 BJTs in the circuit. The sinusoidal signal source Vs drives the Vcc source, which has a voltage of 10V.

Figure 5 displays the screenshot of the Multisim software environment used for the simulation of the circuit in **Figure 4.** The amplitude of the signal source is about *50 mVp.*

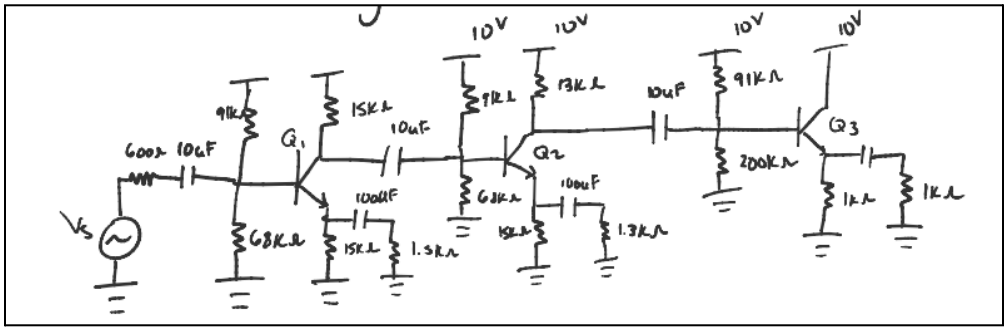


Figure 4: Design of the 3-stage BJT amplifier.

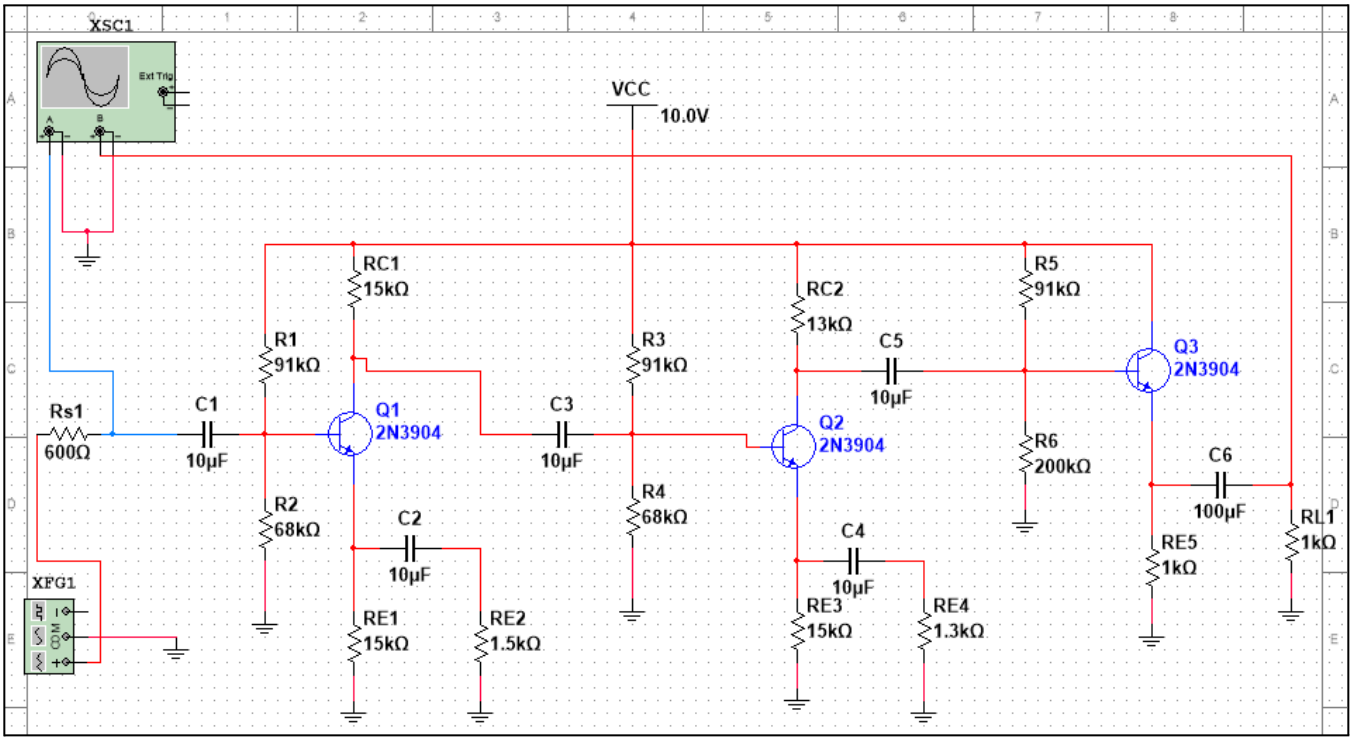


Figure 5: Multisim schematic circuit of Figure 4.

Experimental Results:

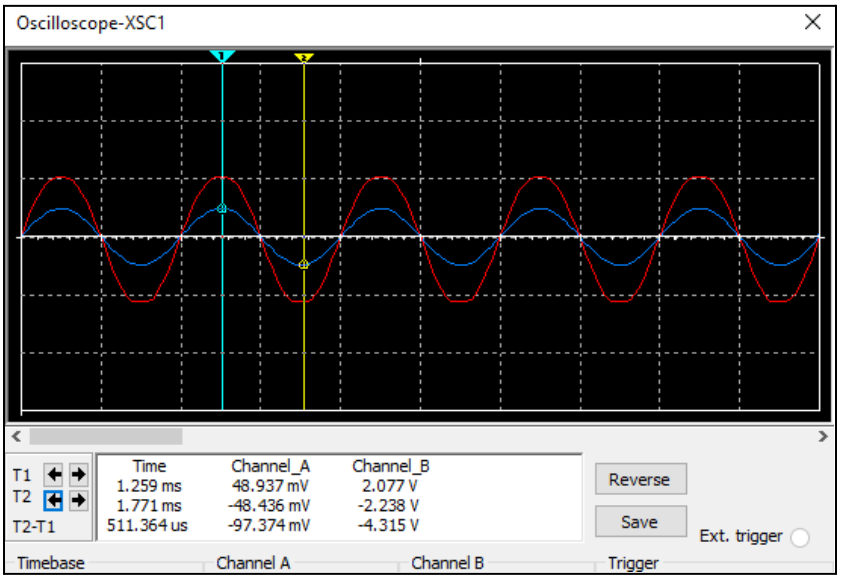


Figure E1: Waveform of the input voltage (blue) and output voltage (red) of Figure 5 (R_L = 1kΩ).

Table E1: Values of input voltage, output voltage and loaded voltage gain (R_L = 1kΩ)

$V_{I, P-P}$ [mV]	$V_{O, P-P}$ [V]	A_V [V/V]
97.37	4.32	44.31

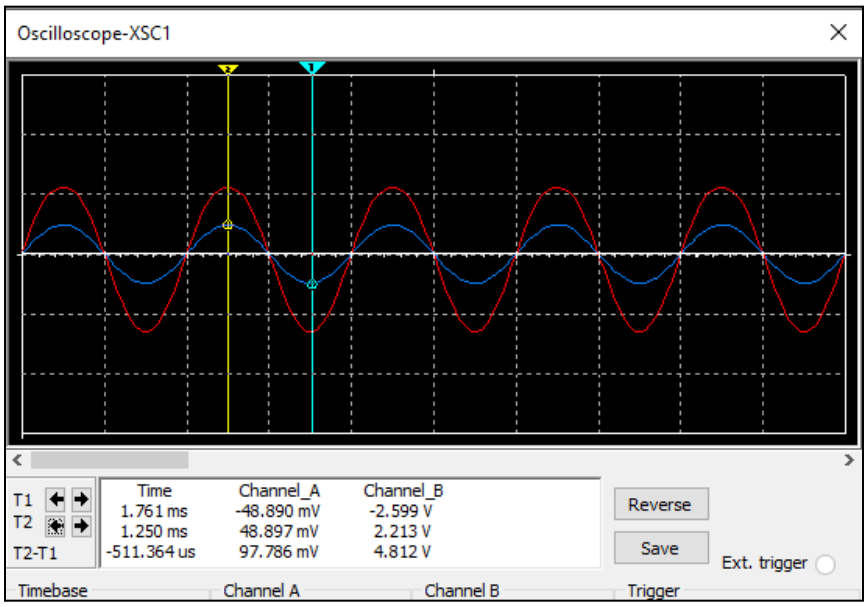


Figure E2: Waveform of the input voltage (blue) and output voltage (red) of Figure 5 (R_L = ∞).

Table E2: Values of input voltage, output voltage and no-loaded voltage gain (R_L = ∞)

$V_{I, P-P}$ [mV]	$V_{O, P-P}$ [V]	A_V [V/V]
97.79	4.81	49.21

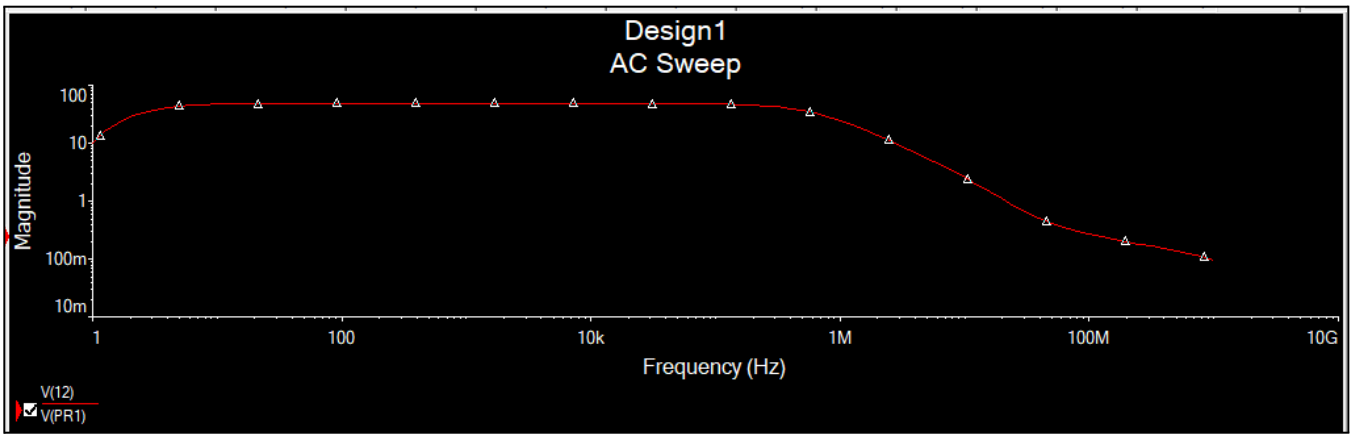


Figure E3: Frequency Response Graph of Figure 5.

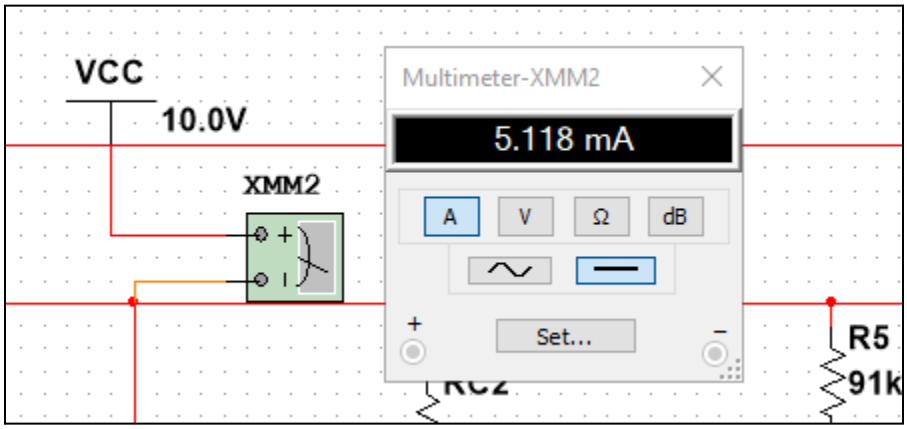


Figure E4: Quiescent current drawn from the power supply.

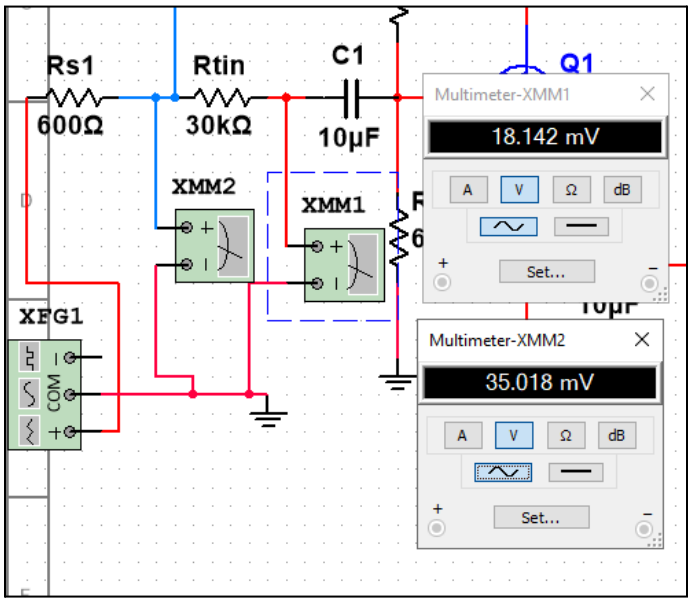


Figure E5: Values of V_t and V_i with $R_{t,in}$ (30kΩ).

$$R_i = R_{t,in}\left(\frac{v_i}{v_t - v_i}\right)$$

Table E2: Parameters of the amplifier for determining its input resistance

$R_{t,\,in}$ [kΩ]	V_t [Vrms]	V_i [Vrms]	R_i [kΩ]
30	35.02 mV	18.14 mV	32.25

Conclusion and Remarks

$$e\% = \frac{calculated\ value - measured\ value}{measured\ value} \times 100$$

Requirements	Calculated Values	Experimental Values	Error Percentage
Quiescent current ≤ 10mA	5.23 mA	5.12 mA	2.19%
$\lvert A_{VO}\rvert$ = 50 (±10%)	50.41	49.21	2.44%
Maximum no-load output voltage swing	8 V	4.81 V	66.25%
Loaded voltage gain: no smaller than 90% of A_{VO}	47.57	44.31	7.37%
Maximum loaded output voltage swing	4 V	4.32 V	7.30%
Input resistance: no smaller than 20 kΩ	31.2 kΩ	32.25kΩ	3.26%
Frequency Response: 20 Hz to 50 kHz	—	**Figure E3**	N/A

Besides the value of the maximum no-load output voltage swing, all the necessary requirements for the design were satisfied with minor discrepancies of less than 10%. The Multisim simulation shows that this is not the case, despite the human calculations indicating that this would be possible. This inaccuracy is most likely the result of biasing or the operating point selection based on the load line graphs. Ultimately, even with this error of the maximum no-load output voltage swing, the circuit's properties remained unaffected since the voltage gain, input resistance, and frequency response and three other critical specifications were all satisfied. The rounding that occurs in manual calculations and any assumptions drawn from the load line graphs are probably the causes of the low % inaccuracies for the other measures. Since everything, including the manual calculations and the Multisim testing, went well, the 3-stage circuit design did well for achieving most of the project's goals.

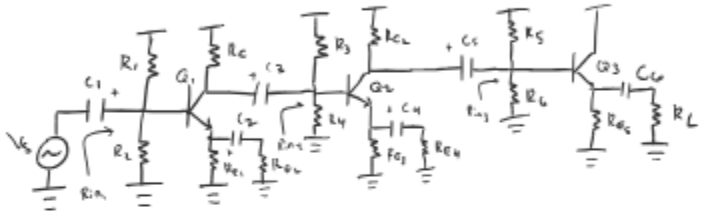
Appendix: Manual Calculations

ELE404 - Design Project

Nathaniel Recto
501162644
Section 16

Manual Calculations:

Schematic idea Design:



$V_{cc} = 10V$
$I_{DC} \leq 10mA$
$A_{vo} = 50$
$V_o \geq 8\ V_{pp}$
$V_L \geq 4\ V_{pp}$
$R_{in} \geq 20\ k\Omega$

For a CC, the gain is close to one, therefore $A_{v_3} = \frac{V_5}{V_4} \approx 1$

Since the final A_v (gain) should be approximately 50, we have $A_{v_o} = A_{v_{o1}} \times A_{v_{o2}} \times A_{v_{o3}}$

$50 = A_{v_{o1}} \times A_{v_{o2}} \times 1$

To make it easier, $A_{v_{o1}}$ & $A_{v_{o2}}$ can have the same amplification

$\sqrt{50} = 7.1$
$7.1 \times 7.1 = 50.41$

$A_{v_{o1}} = \frac{V_2}{V_1} = -7.1$
$A_{v_{o2}} = \frac{V_4}{V_3} = -7.1$

Both are -7.1 because they are CE and should become non-inverting at the end.

Starting with Stage 1 & 2:

Since $A_{v_{o1}} = A_{v_{o2}}$, I_C for both CE's will be 400uA according to the load line (from the graph)

$g_m = \frac{I_c}{V_t} = \frac{400\ uA}{26mV} = 0.0154\ s$

$I_B = 3.5\ uA$
$\beta = \frac{400}{3.5} = 114.3$

$I_{B,DC} = 2.\ uA$ (operating point / quiescent)

Stage 3: Assume $R_{E_3} = 1k\Omega$, close to the R_L value

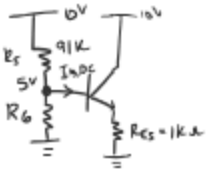
$I_C = 10mA$ (from load line) $\quad \beta = \frac{I_C}{I_B} = \frac{10m}{65u} = 153.8$

$I_B = 65mA$ (from load line) $\quad I_{B,DC} = 30uA$ (operating point / quiescent)

To avoid excessive voltage changes at the base, the divider current should be greater than I_B. According to E_{24} series, we will assume $R_5 = 91k\Omega$ since we want biasing resistors to be high.

Also, $g_m = \frac{10mA}{26mV} = 0.385\ S$ (for Stage 3)

KCL @ Vs:



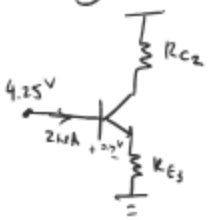
$$\frac{5-10}{91K} + \frac{5}{R_6} + 30uA = 0$$

$$R_6 = 200K\Omega$$

5V is approximated as the voltage where Q (operating point) is from the graph.

Assume $R_{E_3} = 1k\Omega$ due to loading effect.

Stage 2 (CE):



KVL:

$$-4.25V + 0.7 + I_E(R_{E_3}) = 0$$

$$-4.25V + 0.7 + (\beta+1)I_B(R_{E_3}) = 0$$

$$R_{E_3} = \frac{3.55}{(1+114.3)(2uA)} = 15k\Omega$$

$$I_{C,DC} = \frac{V_{CC}}{R_C + R_E}$$

$$R_C + R_{E_3} = \frac{10V}{400uA} = 25k\Omega$$

$$R_C = 25k - R_{E_3}$$

$$R_C = 25k - 15k = 10k\Omega$$

$R_C = 25k - 15k = \underline{10k\Omega}$

To find R_{C_2}, we need R_{in_3}:

R_{C_2}: $\frac{1}{10k} = \frac{1}{R_{C_2}} + \frac{1}{44.57k}$

$\boxed{R_{C_2} = 13k\Omega}$

$R_{in_3} = R_5 // R_6 // \frac{\beta}{gm} + (\beta+1)R_{E_3}$

$= 91k // 200k // \frac{153.8}{0.385} + (154.8)(1k)$

$= \underline{44.57k\Omega}$

} From Stage 3

We can now find R_E using the gain equation. Since stage 1 & 2 are both CE and have the same amplification, they will have the same biasing resistors, and the calculations will be equivalent.

$$A_{V_{O_2}} = \frac{V_3}{V_2} = \frac{-g_{m_2}(R_{C_2} // R_{in_3})}{1 + g_{m_2} R_E}$$

$$-7.1 = \frac{-0.0154\,(13k // 44.57k)}{1 + 0.0154\,(R_E)}$$

$$\underline{R_E = 1350\,\Omega}$$

From this, the A_{V_2} can be found (w/ load)

$R_{in_{L3}} = 91k // 200k // \frac{153.8}{0.385} + (154.8)(506)$

$= \underline{34.7\,k\Omega}$

} From Stage 3, the resistance changed from 1k to 506 when R_L is now used.

$$A_{V_2\,(w/\,load)} = \frac{-0.0154\,(13k // 34.7k)}{1 + 0.0154\,(1350\,\Omega)}$$

$\boxed{A_{V_2} = -6.7}$

Next is finding R_{E_4} for Stage 2:

$R_E = 1350\,\Omega$

$= 1.3k\Omega$

$1.3k\Omega = \frac{1}{\frac{1}{R_{E_3}} + \frac{1}{R_{E_4}}}$

$\frac{1}{1.3k} = \frac{1}{15k} + \frac{1}{R_{E_4}}$

$R_{E4} = 1.4k\Omega$

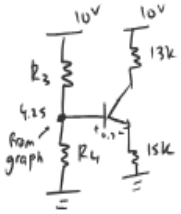
$R_{E4} \approx 1.3k\Omega$ ← E_{24} series

$R_E \downarrow \rightarrow$ gain $\uparrow$

Biasing Resistors:

Similar to stage 3, we require large resistors so that the divider current exceeds I_B. This is important for CE's since a low divider current can damage V_s.

Assume $R_3 = 91k\Omega$



KCL @ V_3:

$$\frac{4.25-10}{91k} + \frac{4.25}{R_4} + 2uA = 0$$

$R_4 = 69k\Omega$

$R_4 \approx 68k\Omega$

Next, $R_{in_2} = R_3 // R_4 // \frac{\beta}{g_m} + (\beta+1) R_E$

$= 91k // 68k // \frac{114.3}{0.0154} + (115.3)(1350)$

$= 31.4k\Omega$

Finally, we have Stage 1 (CE)

$I_{C,DC} = \frac{V_{CC}}{R_{C_1} + R_{E_1}}$

$R_{C_1} + R_{E_1} = \frac{10V}{400uA}$

$= 25k\Omega$

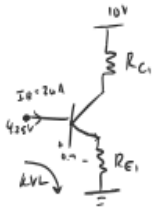
KVL:

$-4.25 + 0.7 + I_E(R_{E_1}) = 0$

$3.55 = (1+\beta) I_B R_{E_1}$

$R_{E_1} = \frac{3.55}{(115.3)(2uA)}$

$R_{E_1} = 15k\Omega$



$25k = R_C + R_{E_1}$

$R_C = 25k - 10k$

$R_C = 10k\Omega$

$R_{C_1}: R_C = R_{E_1} // R_{in_2}$

$10k = \frac{1}{\frac{1}{R_{E_1}} + \frac{1}{31.4k}}$

$R_{E_1} = 15k\Omega$

We can now find R_E using the gain equation:

$A_{V_1} = \frac{-g_m (R_{C_1} // R_{in_2})}{1 + g_m R_E}$

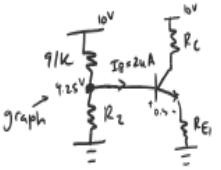
$-7.1 = \frac{-0.0154 (15k // 31.4k)}{1 + (0.0154) R_E}$

$R_E = 1.3k\Omega$

$R_{E_2}: R_E = R_{E_1} // R_{E_2}$

$1.3k = \frac{1}{\frac{1}{15k} + \frac{1}{R_{E_2}}}$

$R_{E_2} \approx 1.5k\Omega$ ← rounded to nearest E_{24} series



KCL;

$$\frac{4.25-10}{91k} + \frac{4.25}{R_2} + 2uA = 0$$

$R_2 \approx 68k\Omega$

$R_{in_1} = 91k // 68k // \frac{\beta}{g_m} + (\beta+1) R_E$

$= 91k // 68k // \frac{114.3}{0.0154} (115.3)(1.3k)$

$R_{in_1} = 31.2k\Omega$

Capacitor Values can now be determined.

The quiescent current can therefore be calculated as the last valid calculation, in addition to the overall gain.

It should be noted that emitter degeneration resistance is vital for maintaining the CE stages' gain.

C_2, C_4 and C_6 are expected to have a large value. On the other hand, the values of R_{in_1}, R_{in_2}, & R_{in_3} are already pretty high, therefore C_1, C_3, & C_5 should be less large.

The frequency range is 20Hz - 50kHz.

The average case we will use is 1kHz.

The capacitors used to test this will have sample of 100uF and 10uF (according to E_{24} series)

$C_2, C_4, C_6 = 100uF$

$Z = \frac{1}{2\pi f C} = \frac{1}{2\pi (1kHz)(100uF)} = 1.6\Omega$

$C_1, C_3, C_5 = 10uF$

$$Z = \frac{1}{2\pi fC} = \frac{1}{2\pi(1kHz)(10uF)} = 16\,\Omega$$

∴ These test values should allow the circuit to maintain the gains.

Final Gains:

$$A_{V_0} = -7.1 \times -7.1 \times 1 = 50.41$$

$$A_V = -7.1 \times -6.7 \times 1 = 47.57$$

We presume that the gain in Stage 3 for A_{V_0} & A_V is close to one because it is a cc amplifier. For A_V, it is expected that the first stage will not feel the loading impact of R_L, therefore A_{V_1} would still be -7.1 and A_{V_2} is calculated to be -6.7.

Quiescent current : $I_{dc,total} = I_{C_1} + I_{R_1} + I_{C_2} + I_{R_3} + I_{C_3} + I_{R_5}$

$$= \beta I_{B_1} + \frac{V_{cc}}{R_1 + R_2} + \beta I_{B_2} + \frac{V_{cc}}{R_3 + R_4} + \beta I_{B_3} + \frac{V_{cc}}{R_5 + R_6}$$

$$= 114.3\,(2uA) + \frac{10}{91k + 68k} + (114.3)(2uA) + \frac{10}{91k + 68k} + 153.8\,(30uA) + \frac{10}{200k \times 91k}$$

$$I_{DC,total} = 5.23\,mA$$

Final Circuit Design: