Minnesota State University, Mankato

Electrical and Computer Engineering Department

Final Assignment – Building N- channel MOS

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Name
Nathnael Minuta

EE 303-02 Introduction to Solid State Devices
Dr. Puteri Megat Hamari
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Building N- channel MOS

Abstract

This lab focuses on designing and simulating an NMOS transistor structure using TCAD tools to explore its behavior under various operating conditions, including subthreshold operation and high drain-to-source voltages. Through the simulation, key device characteristics such as threshold voltage (Vt), subthreshold slope (SS), and transconductance (gm) are extracted and analyzed. The experiment examines the effects of substrate doping concentration and applied voltages on drain current, band diagrams, and electron density during conduction. These insights contribute to understanding the interplay between material properties, doping profiles, and device performance, enabling the design of optimized transistors for advanced electronic applications.

Purpose (Objective)

The purpose of this lab is to:

1. **Design and simulate an NMOS transistor structure** with various substrate doping concentrations to study their effects on key electrical characteristics.
2. **Analyze critical parameters** such as threshold voltage (Vt), subthreshold slope (SS), and transconductance (gm) derived from I-V curves to assess device performance.
3. **Investigate the effects of high electric fields** on current conduction, observing band diagrams, electron density profiles, and potential punch-through conditions.
4. **Develop a comprehensive understanding** of how doping concentration and applied voltages influence device operation, using TCAD tools to create visualizations such as I-V plots and band diagrams.
5. **Enhance simulation skills** by constructing a detailed NMOS model, meshing the device, and performing simulations that reveal how material properties and design choices impact device behavior.

Materials

Equipment Needed	**Quantity.**
Sentaurus Workbench	1
Laptop	1

Theory

Sentaurus Workbench

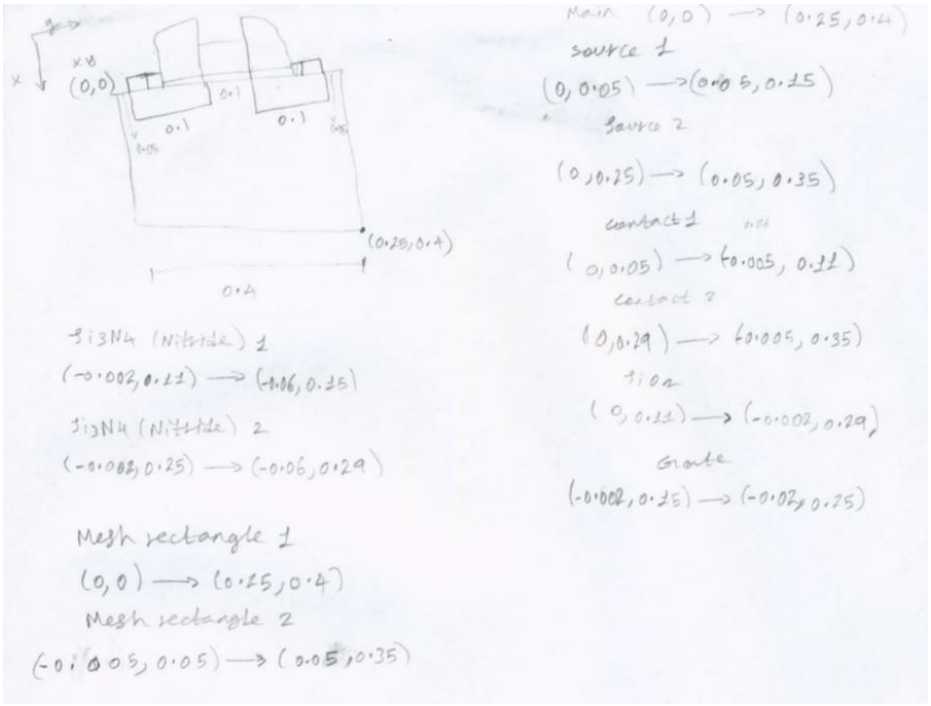
Sentaurus Workbench (SWB) is a simulation environment used to analyze semiconductor devices. In this lab, three primary tools were employed:

- **SDE (Sentaurus Structure Editor):** For defining the NMOS device's geometry, materials, and doping profiles.
- **SDevice:** To simulate electrical characteristics such as I-V behavior, threshold voltage (Vt), and breakdown conditions.
- **SVisual:** For analyzing simulation results, including band diagrams and electron density distributions.

NMOS Transistor

The NMOS transistor, a fundamental building block in modern electronics, is a type of MOSFET that operates by modulating electron flow through a conductive channel formed in a lightly doped p-type substrate. It features three main terminals: the source, drain, and gate, with the gate separated from the substrate by a thin layer of silicon dioxide (SiO_2). When a sufficient voltage is applied to the gate, it creates an electric field that attracts electrons to form a conductive channel, enabling current flow between the source and drain. This ability to switch states quickly and efficiently makes NMOS transistors essential in digital and analog circuits, powering devices ranging from microprocessors to memory systems.

Methods (Procedure, Data Collection, and Analysis)



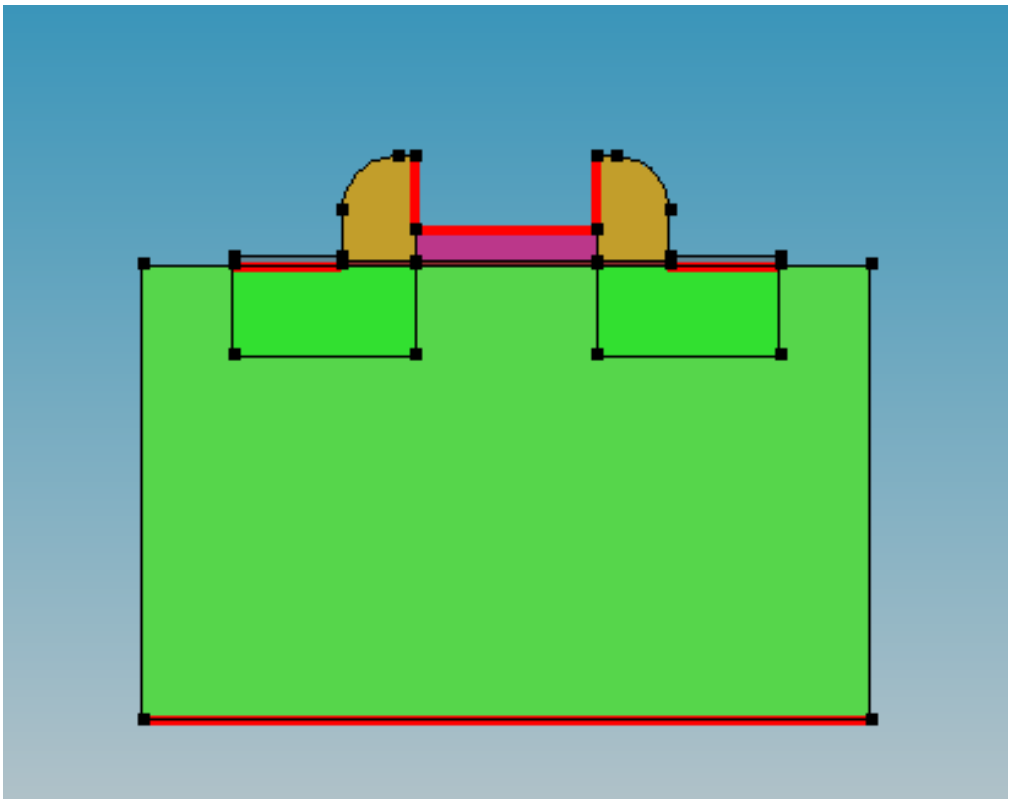


Figure 1: Geometric cross section of NMOS

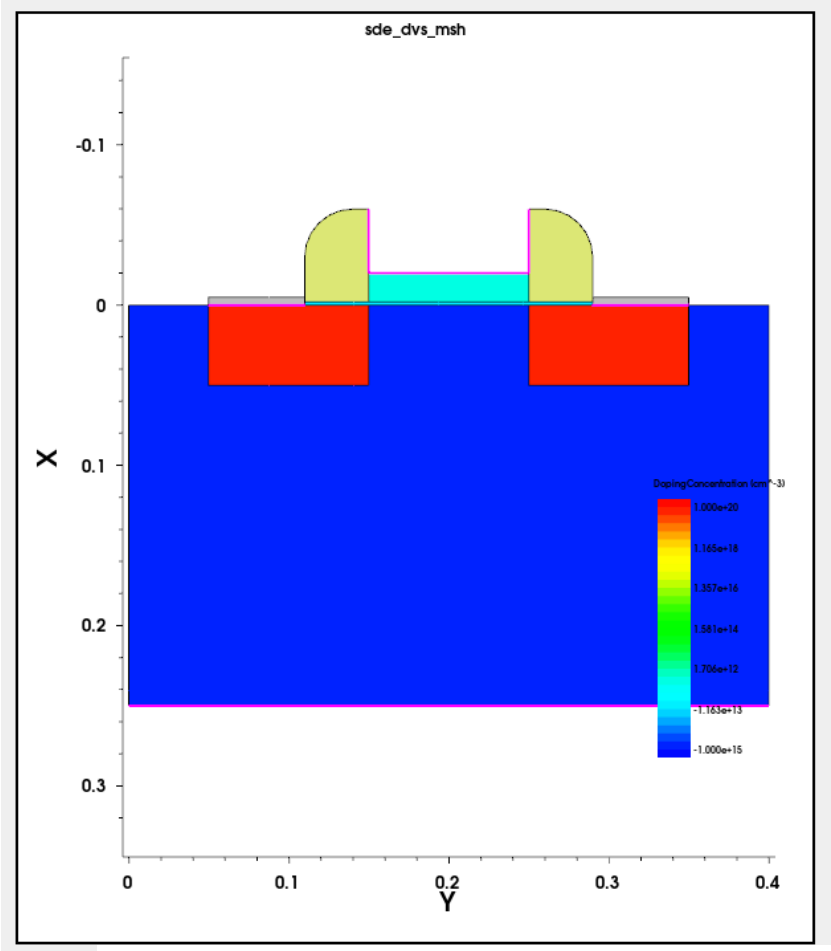


Figure 2: Result from meshing my drawing

Project | Scheduler

	SDE		SDEVICE		SVISUAL				
	sde		sdevice		svisual				
		sub_doping		VD	VG		Vtgm	Id	SS	gm
1	--	1e15	--	2.5	1.5	--	0.550	7.649e-04	3262.651	8.051e-04
2					2.5	--	0.797	1.743e-03	3109.262	1.024e-03
3				5	1.5	--	0.136	1.091e-03	5762.859	7.998e-04
4					2.5	--	0.535	2.093e-03	5435.620	1.065e-03
5		1e17	--	2.5	1.5	--	0.844	5.256e-04	1152.661	8.010e-04
6					2.5	--	1.034	1.501e-03	1160.173	1.024e-03
7				5	1.5	--	0.504	7.955e-04	3246.151	7.986e-04
8					2.5	--	0.817	1.798e-03	3138.717	1.069e-03
9		1e18	--	2.5	1.5	--	1.315	9.821e-05	114.598	5.304e-04
10					2.5	--	1.513	8.857e-04	119.914	8.978e-04
11				5	1.5	--	1.251	1.569e-04	114.839	6.311e-04
12					2.5	--	1.437	1.012e-03	113.098	9.518e-04

Figure 3: My Experimentation tree (Before Punch-Through)

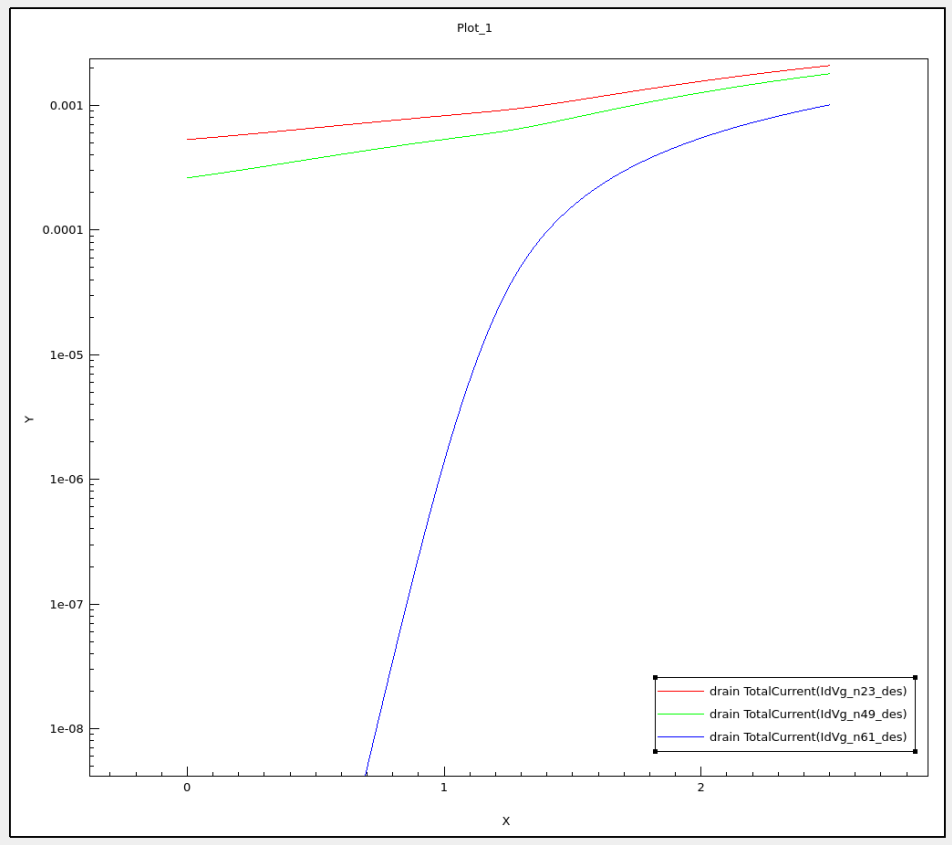


Figure 4 : IdVg.plt for sub_doping 1e15, 1e17, 1e18 at VD=5V, VG=2.5V (after applying log scale to Y1)

Graph Analysis:
The graph illustrates the relationship between **Gate Voltage (VG)** and **Drain Current (Id)** for varying doping concentrations:

- **Key Observation**: Increasing substrate doping concentration (SubDop) leads to a higher **threshold voltage (VTgm)**. This means the transistor requires a larger **VG** to turn on. As a result:
    - Higher doping reduces the drain current (Id) for a given VG.
    - Overall drive capability of the device decreases.

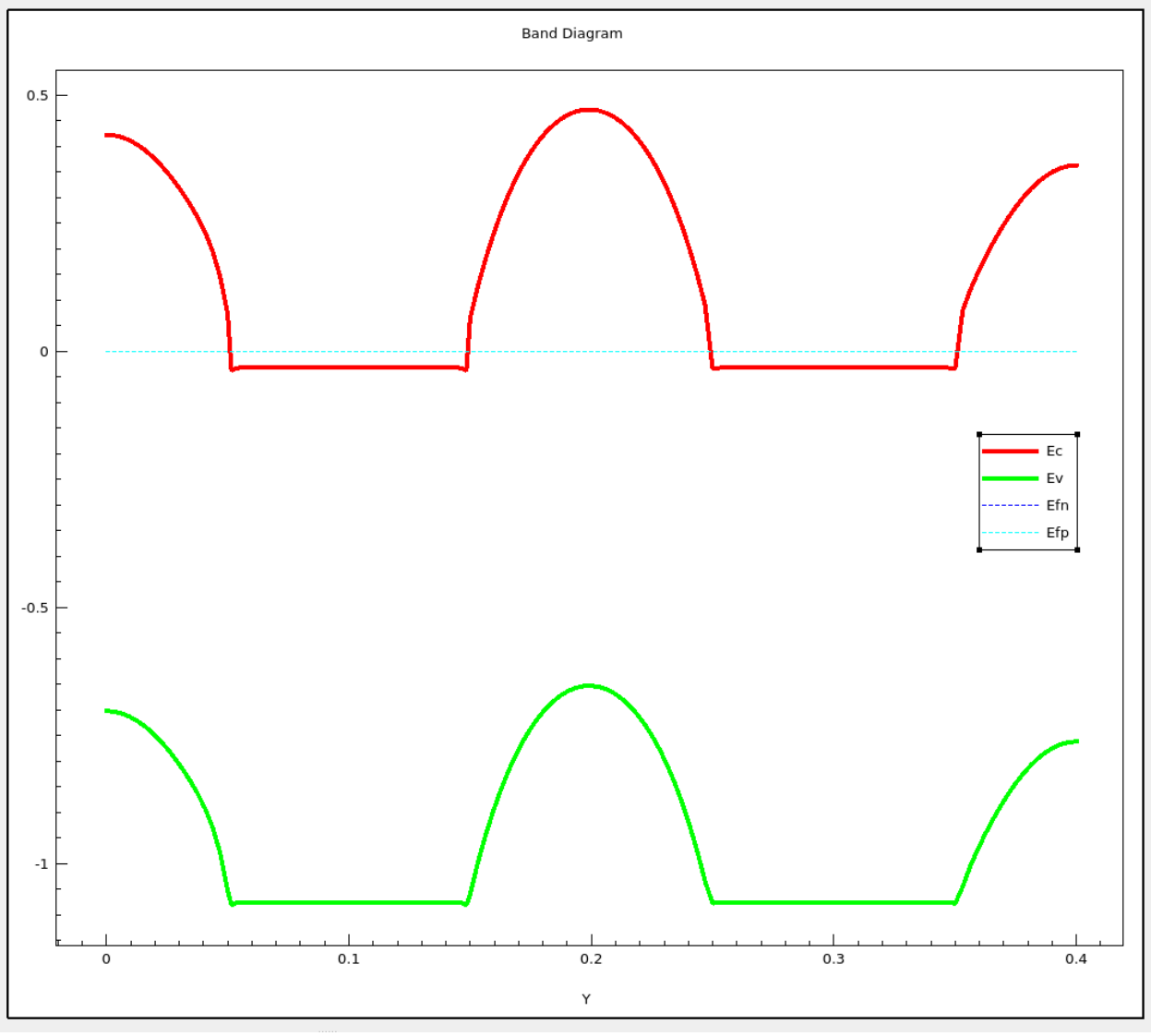


Figure 5: Energy bands at equilibrium (1e17, vd=2.5v, vg=2.5v)

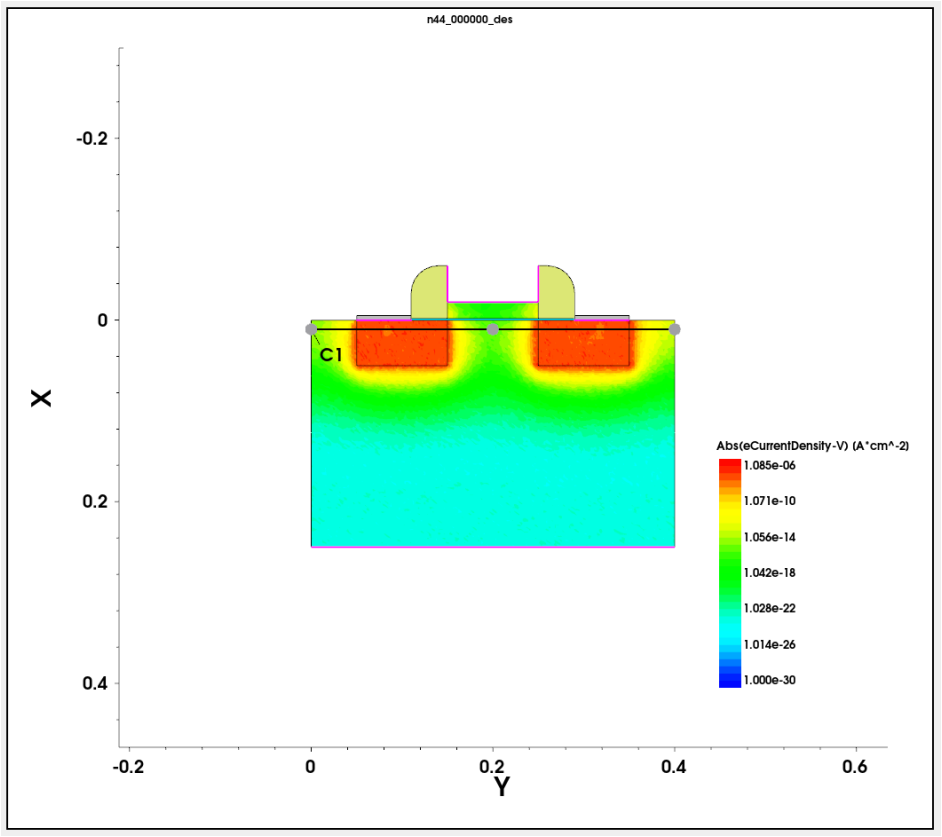


Figure 6: Cross section of node n_000000_des.td (1e17, vd=2.5v, vg=2.5v)

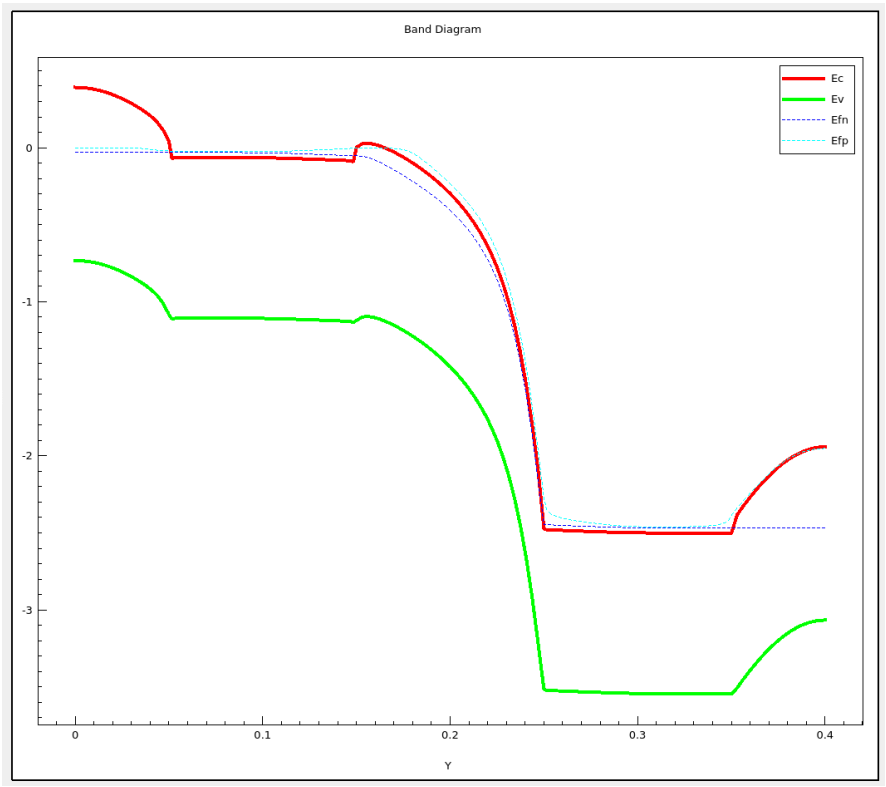


Figure 7: Energy band of n_000003_des.tdr (1e17, vd=2.5v, vg=2.5v)

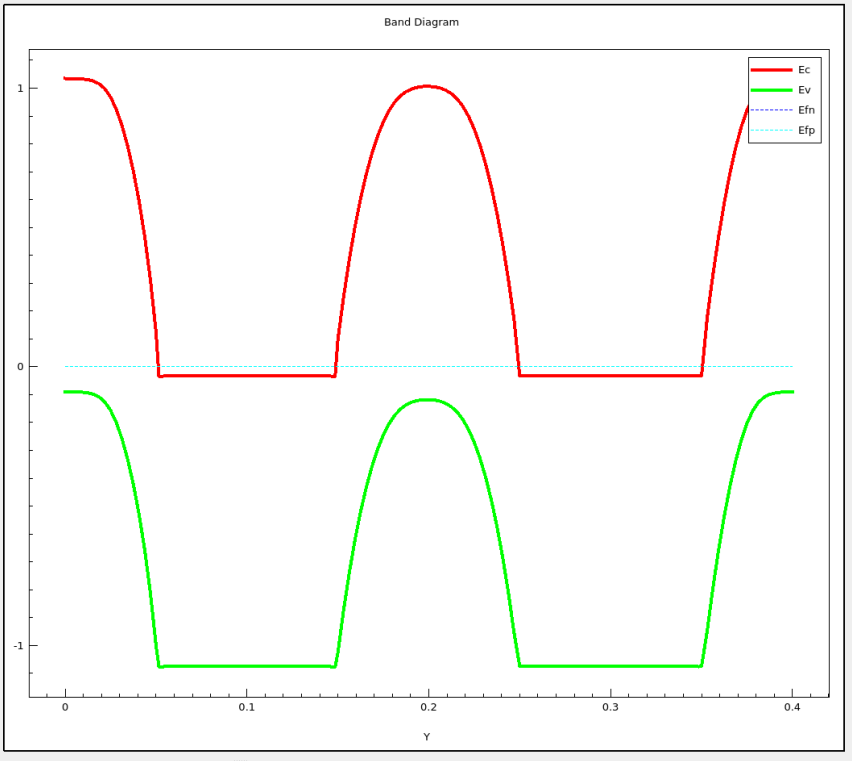


Figure 8: Energy band of n_000003_des.tdr (1e17, vd=2.5v, vg=1.5v)

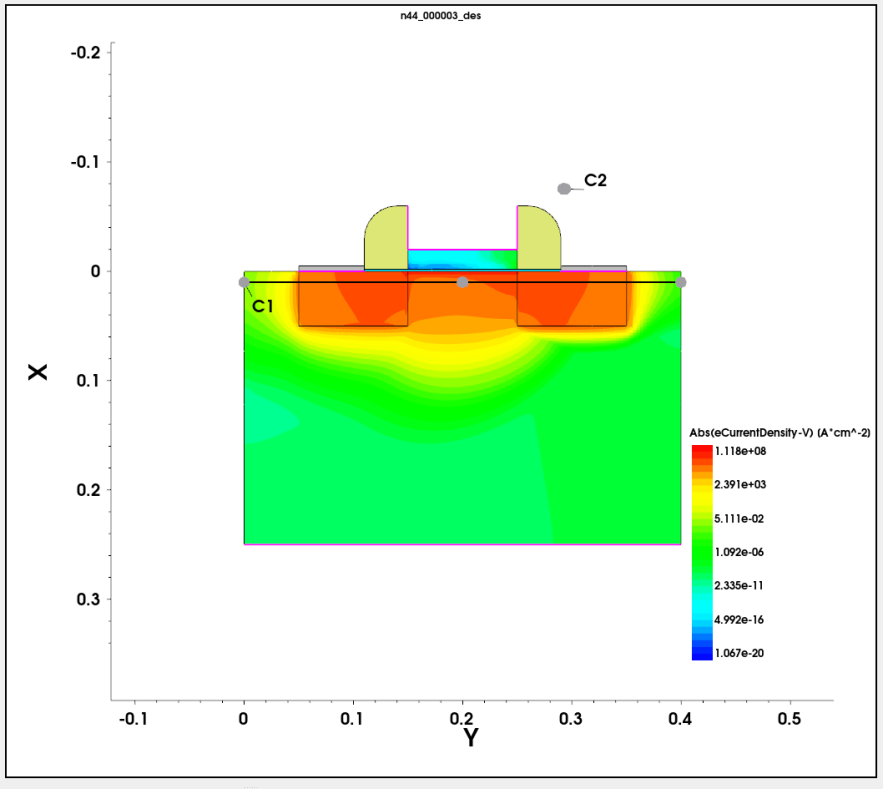


Figure 9: Cross section of node n_000000_des.td (1e17, vd=2.5v, vg=1.5v)

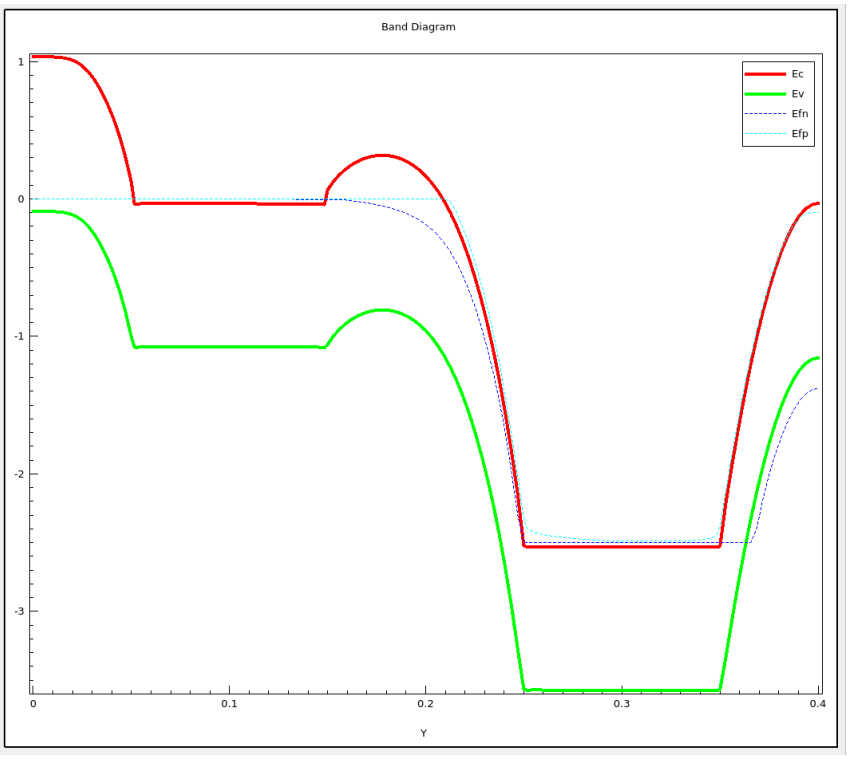


Figure 10: Energy band of n_000003_des.tdr (1e17, vd=2.5v, vg=1.5v)

Key Takeaways:

- The band diagrams reveal that as the gate voltage increases, the energy bands at the gate interface bend more significantly, indicating the formation of a conductive channel between the source and drain. At lower gate voltages (VG = 1.5V), the energy bands are bent upwards, preventing current flow and forming a depletion region. At higher gate voltages (VG = 2.5V), the energy bands bend downward, reducing the potential barrier and allowing electrons to flow, facilitating conduction.
- At VG = 1.5V and VD = 2.5V, no current flows as the energy bands are not bent enough to form a conductive channel, keeping the transistor in the "off" state. At VG = 2.5V and VD = 2.5V, the increased gate voltage reduces the depletion region, forming a conductive channel that allows current to flow, turning the transistor "on."

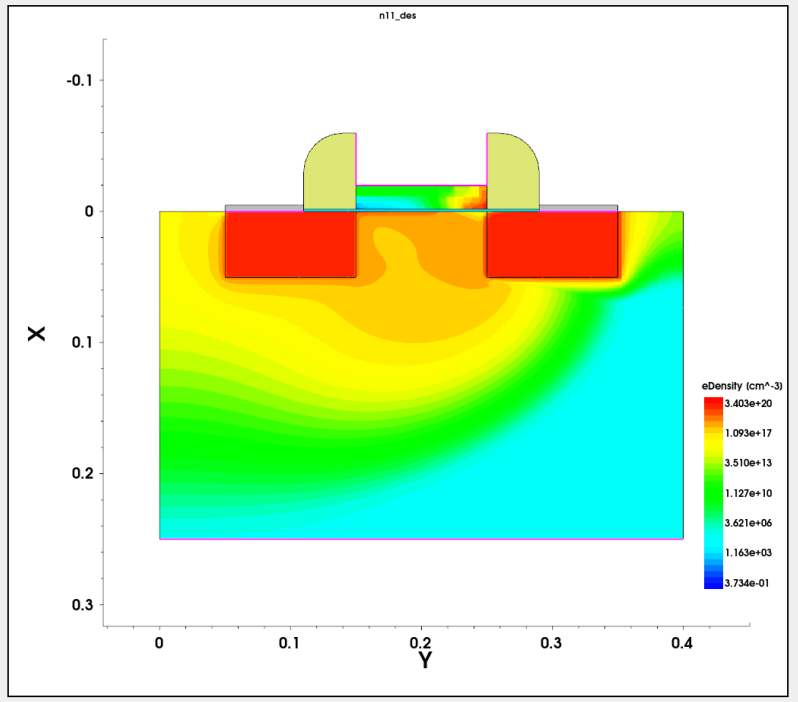


Figure 11: Electron Density (doping= 1e15, VD=5V, VG=1.5V)

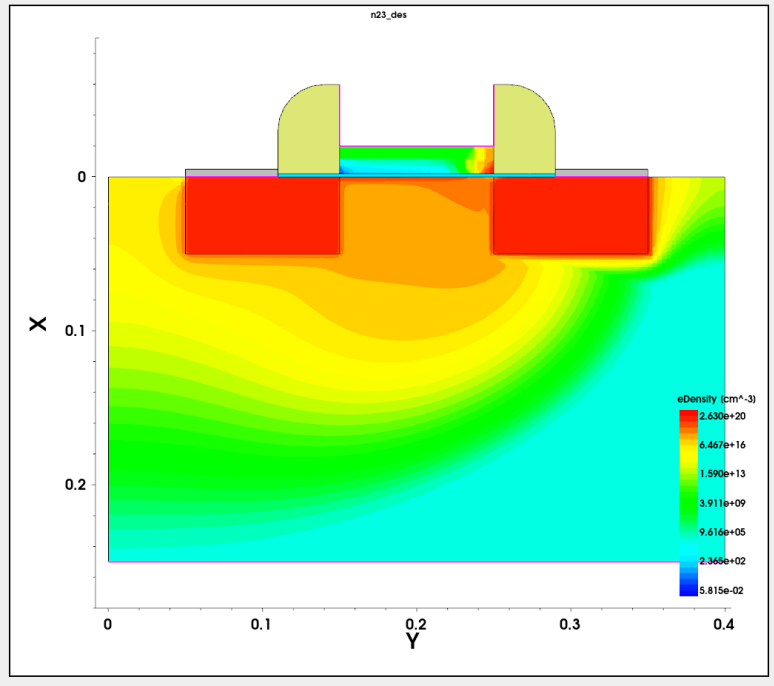


Figure 12: Electron Density (doping= 1e15, VD=5V, VG=2.5V)

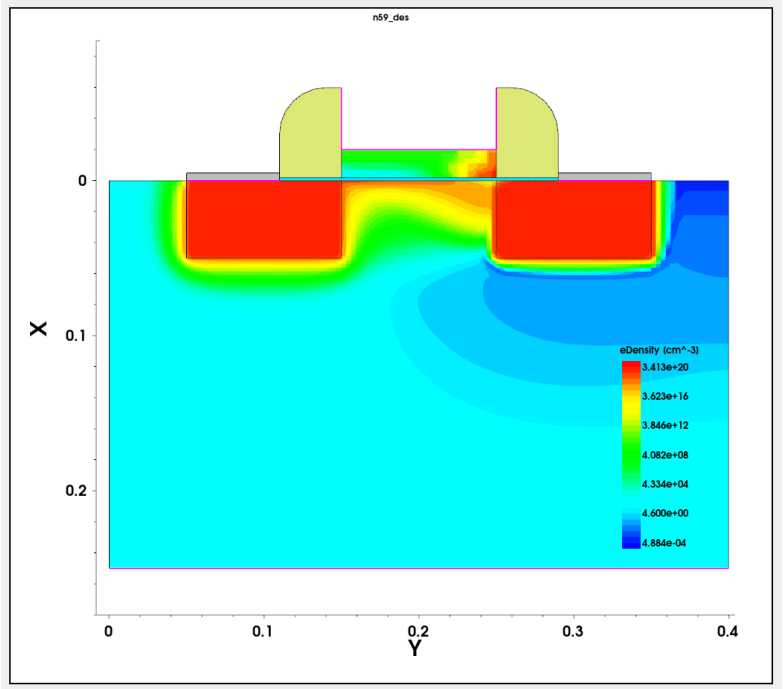


Figure 13: Electron Density (doping= 1e18, VD=5V, VG=1.5V)

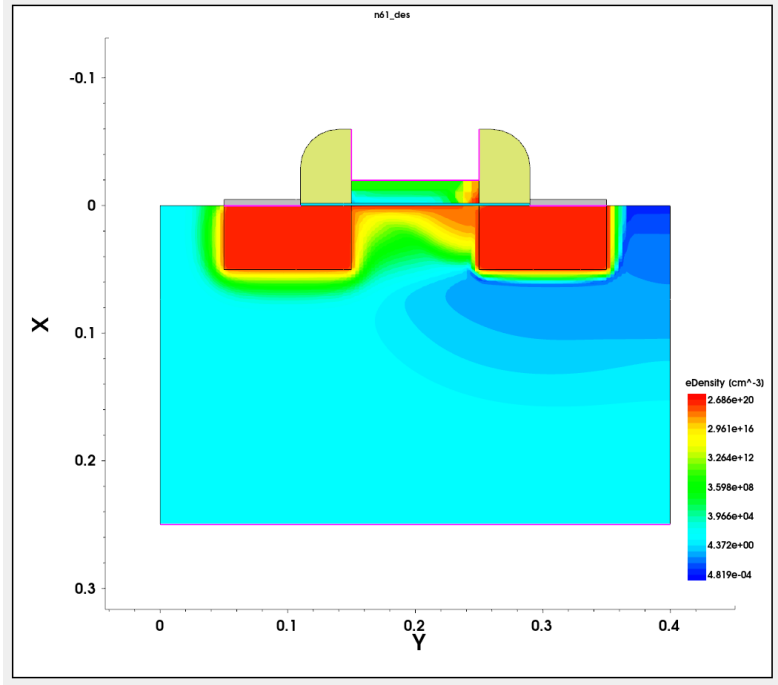


Figure 14: Electron Density (doping= 1e18, VD=5V , VG=2.5V)

Increasing both the gate voltage and doping concentration enhances electron density, which improves the channel's conductivity. This interplay significantly impacts the transistor's performance, as higher gate voltage attracts more electrons, while higher doping concentration provides a greater supply of charge carriers, allowing for more efficient current flow.

Additional Scalar Comparison

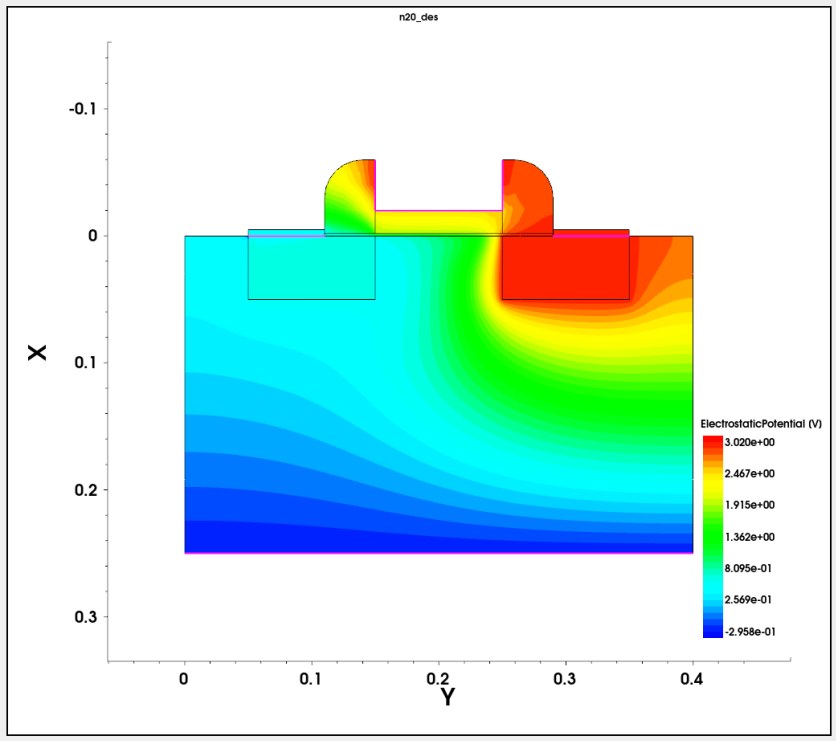


Figure 15: Electrostatic Potential (doping=1e15, VD=2.5V, VG=2.5V)

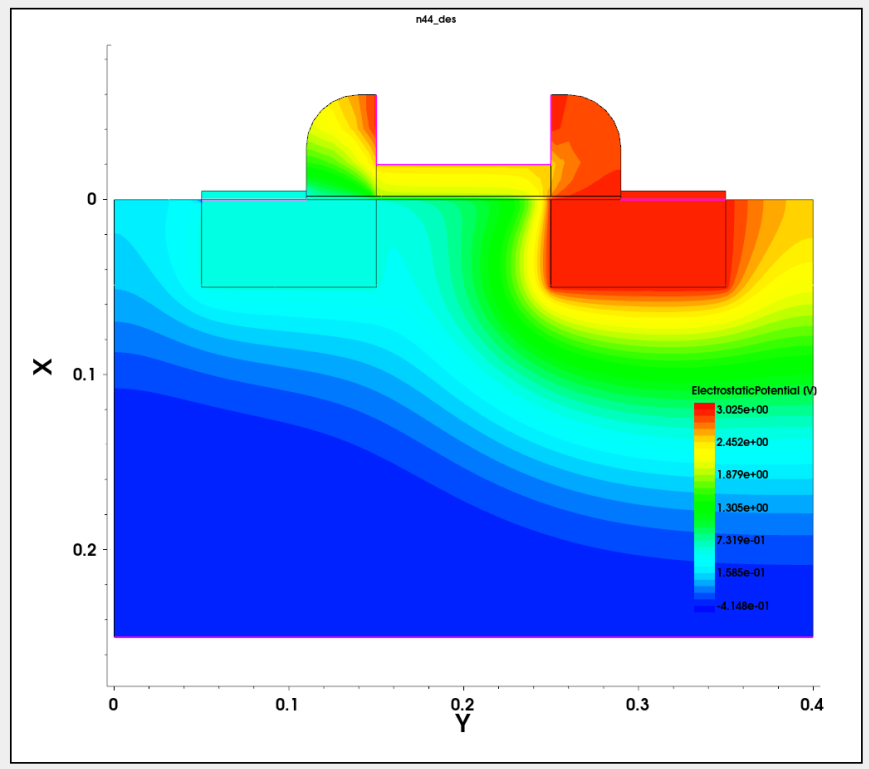


Figure 16: Electrostatic Potential (doping=1e17, VD=2.5V, VG=2.5V)

Discussion for this on page 14

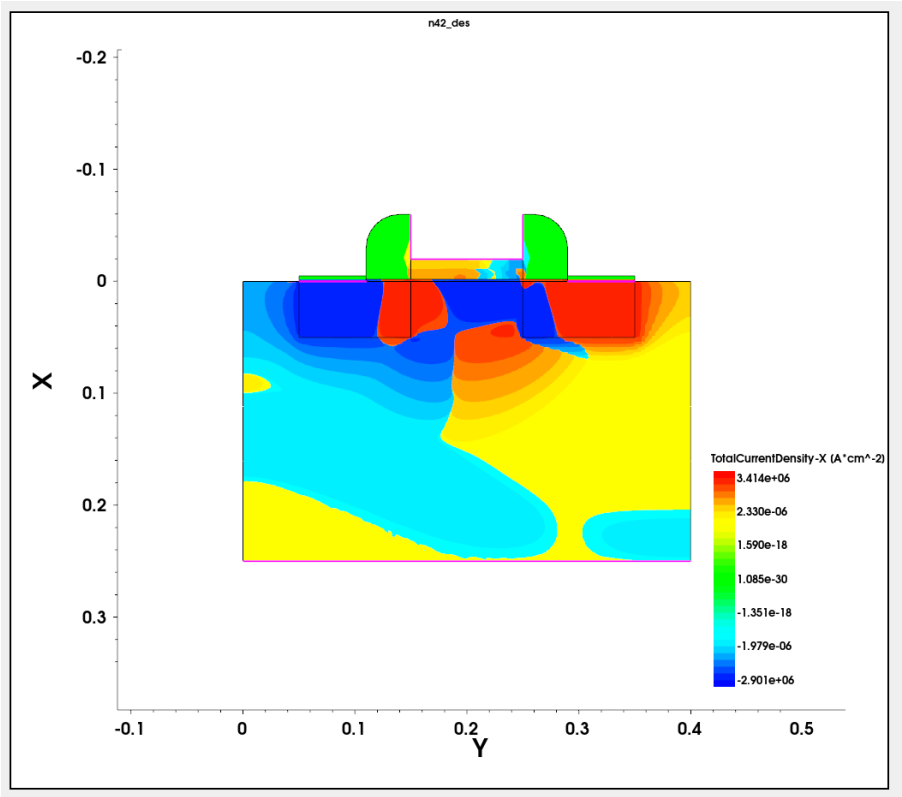


Figure 17: Total Current Density (doping = 1e17, VD= 5V, VG= 1.5V)

Discussion for this on page 16

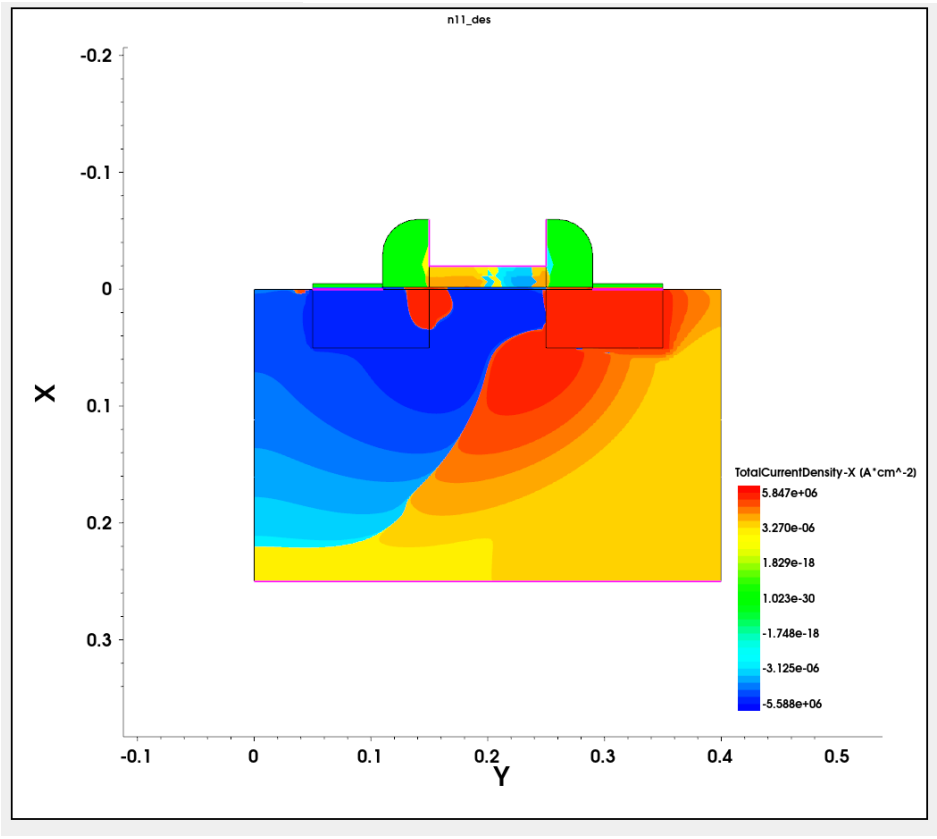


Figure 18: Total Current Density (doping = 1e15, VD= 5V, VG= 1.5V)

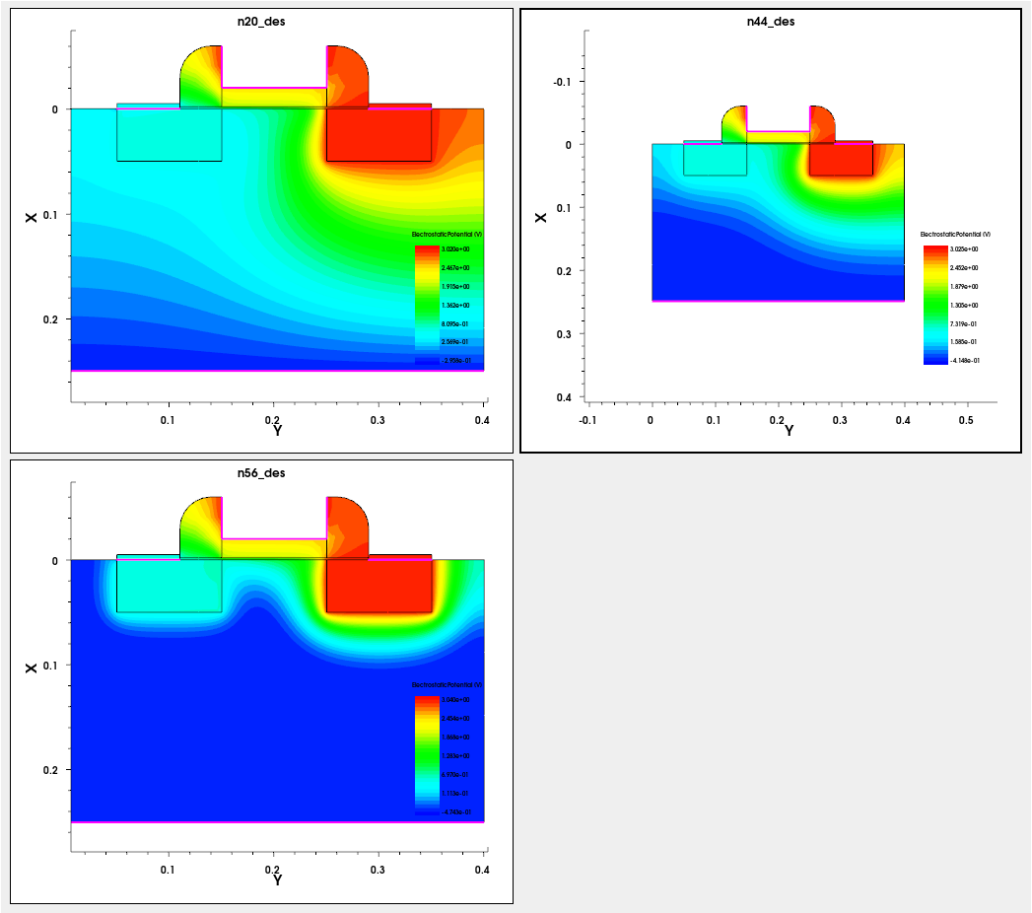


Figure 19: Electrostatic Potential (doping=1e15, 1e17, 1e18, VD=2.5V, VG= 2.5V)

The **Electrostatic Potential** graph shows the variation of the electrostatic potential along the MOSFET channel, influenced by the doping concentration and applied voltages. At higher doping concentrations (1e17 and 1e18), the potential drop across the channel becomes more pronounced, which affects the formation of the conductive channel. The gate voltage (VG) attracts electrons, while the drain voltage (VD) influences the potential near the drain, impacting current flow. This interaction between doping concentration, gate, and drain voltages determines the transistor's behavior and conductivity.

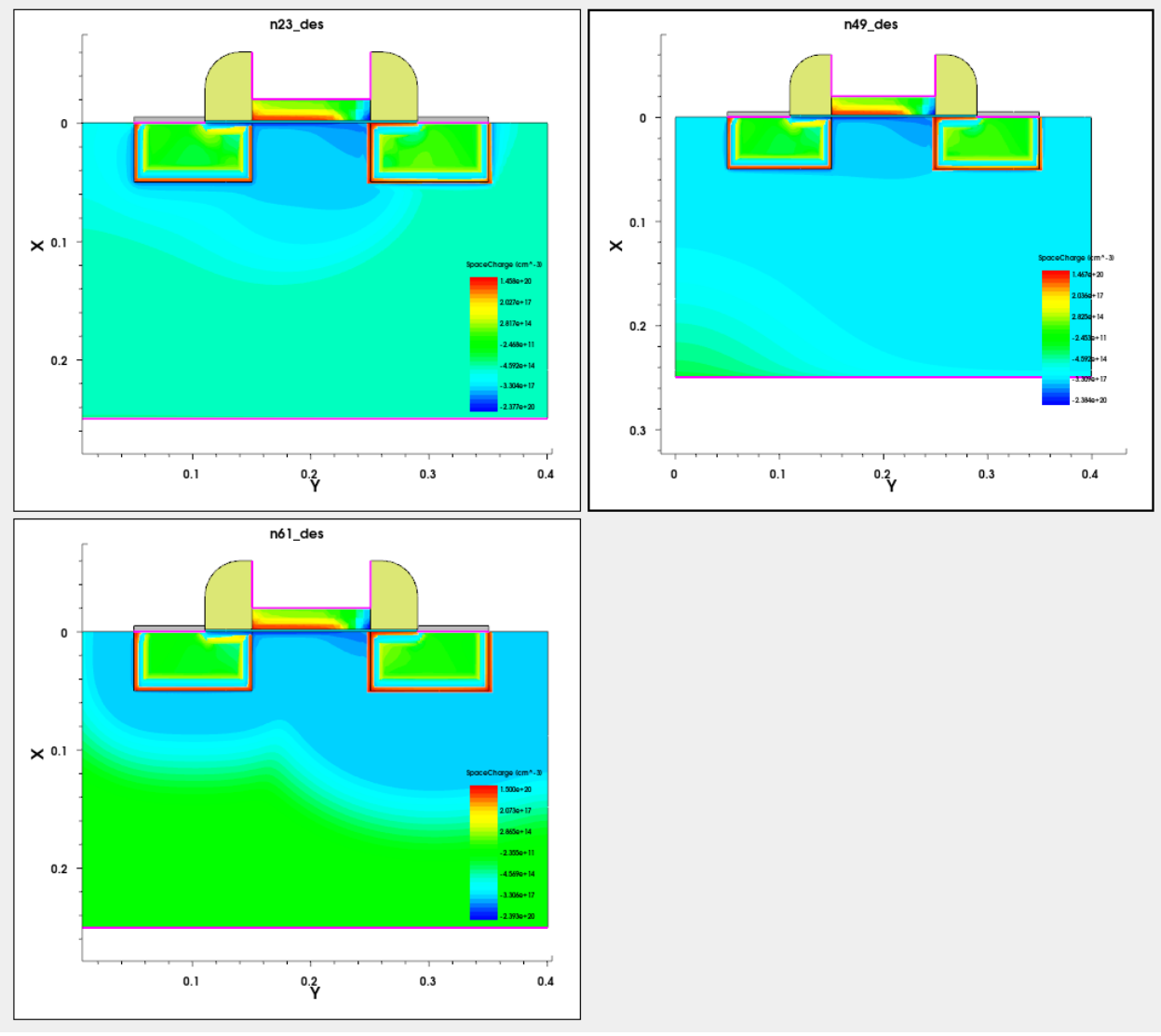


Figure 20: Space charge (doping=1e15, 1e17, 1e18, VD=5V, VG= 2.5V)

The **Space Charge** graph shows the distribution of charge carriers (electrons and holes) within the MOSFET channel, influenced by doping concentrations, applied drain voltage (VD), and gate voltage (VG). At higher doping concentrations (1e17 and 1e18), the space charge region near the source and drain becomes more pronounced, leading to stronger electric fields. The graph illustrates how the charge distribution affects the overall conductivity of the channel.

As doping concentration increases, the space charge region expands, which can impact the transistor's switching behavior and performance. This analysis helps in understanding how doping levels and voltages influence the charge distribution and the transistor's efficiency.

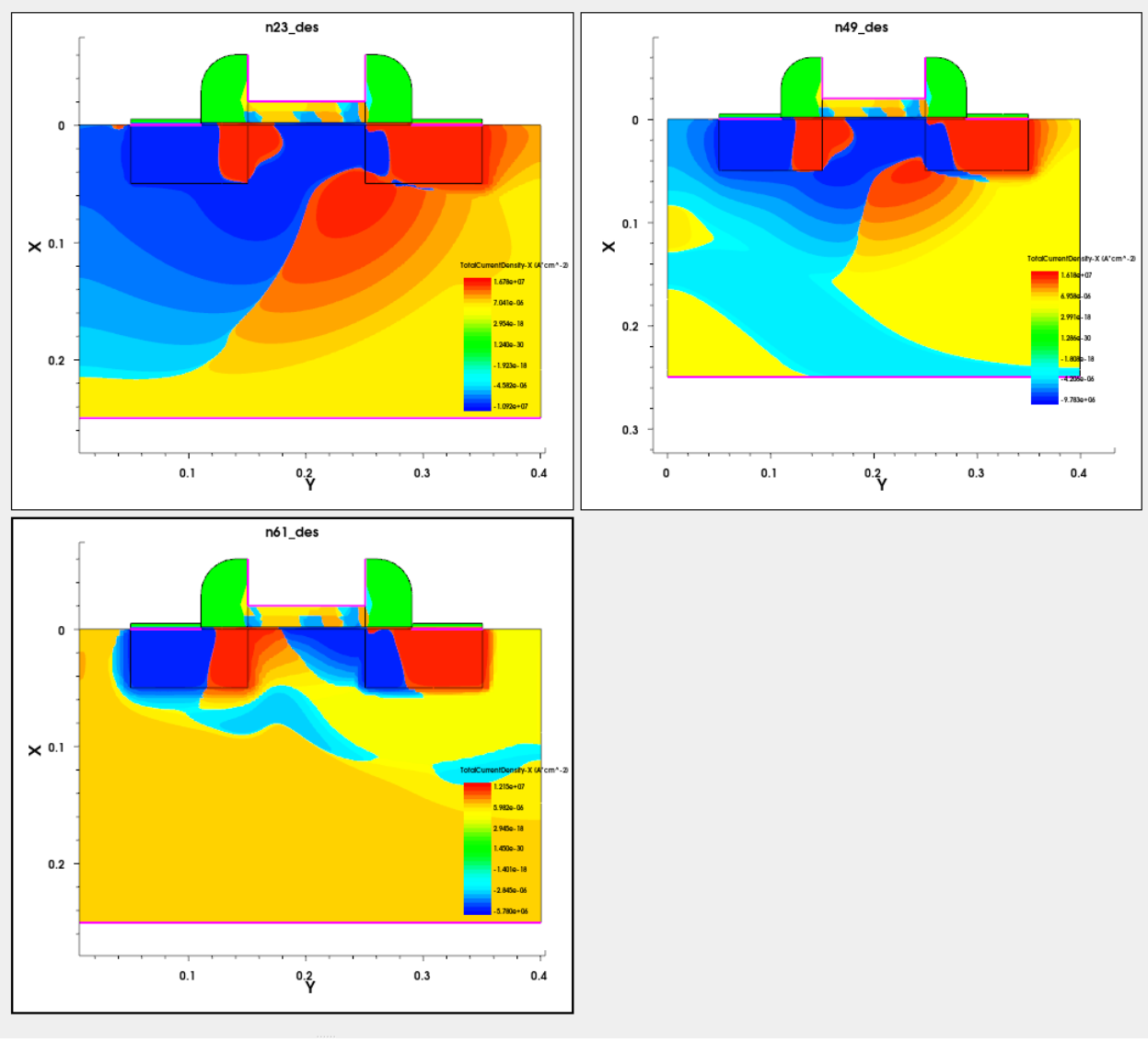


Figure 21: Total Current Density (doping=1e15, 1e17, 1e18, VD=5V, VG= 2.5V)

The **Total Current Density** graph displays the flow of electric current within the MOSFET channel at varying doping concentrations (1e15, 1e17, 1e18) with a constant drain voltage (VD = 5V) and gate voltage (VG = 2.5V). As doping concentration increases, the current density generally increases, indicating a higher number of charge carriers contributing to the current flow.

The graph shows how doping concentration affects the current conduction within the device. Higher doping concentrations result in enhanced carrier mobility and increased current density, which improves the transistor's performance.

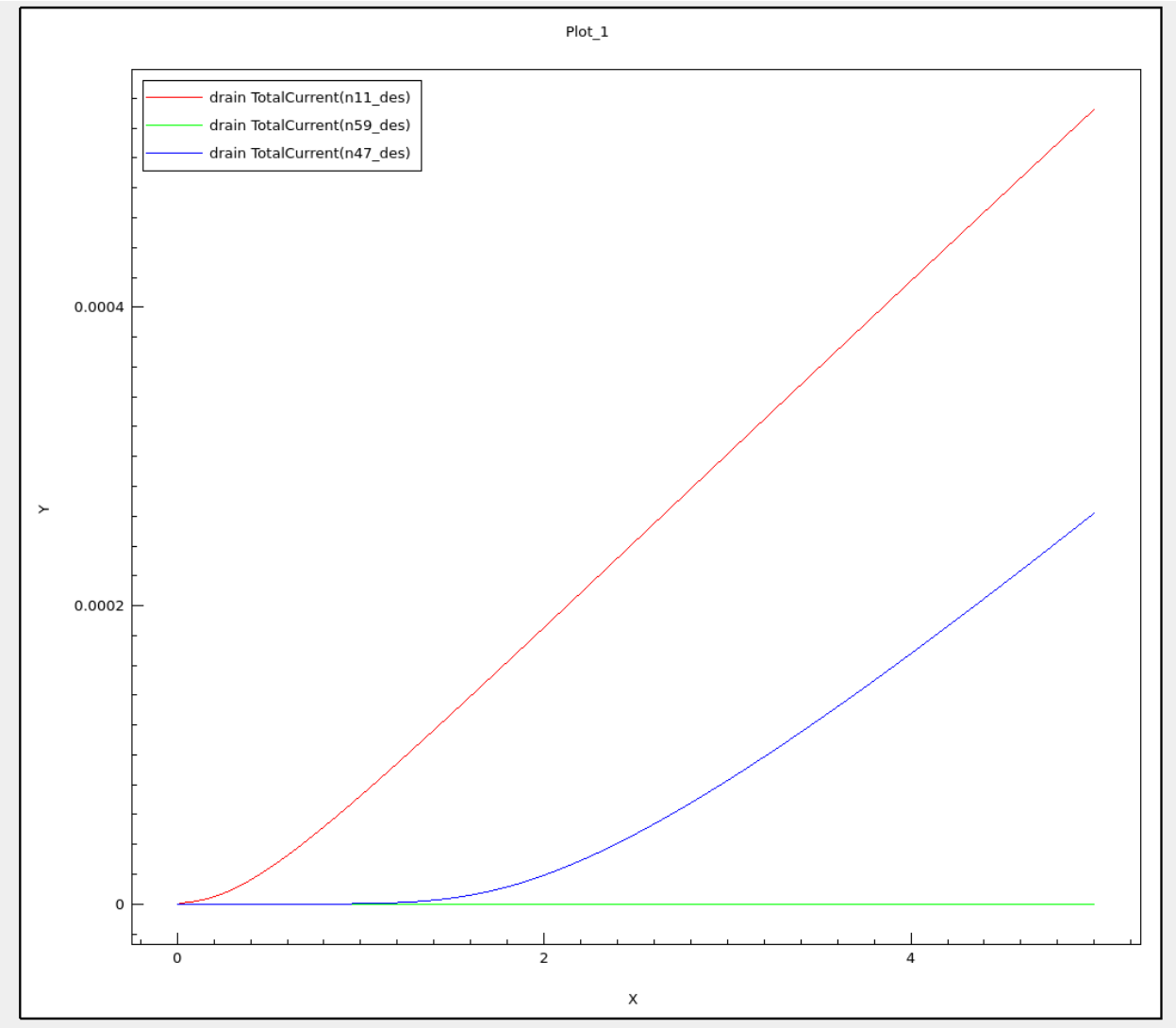


Figure 22: ID vs Vgs (doping=1e15, 1e17, 1e18, VD=5V, VG= 1.5V)

Key Takeaways:

- The **ID vs. Vgs** graph shows the drain current (ID) for three doping concentrations: node 11 (1e15), node 47 (1e17), and node 59 (1e18). As the doping concentration increases:
    - **Node 11 (1e15)**: The current increases gradually, indicating low channel conductivity.
    - **Node 47 (1e17)**: The current rises more sharply, showing better gate modulation and moderate doping.
    - **Node 59 (1e18)**: The current increases significantly, indicating high channel conductivity and strong gate modulation.
- In summary, higher doping concentrations lead to more efficient current flow and greater responsiveness to gate voltage.

Punch Through (Bonus)

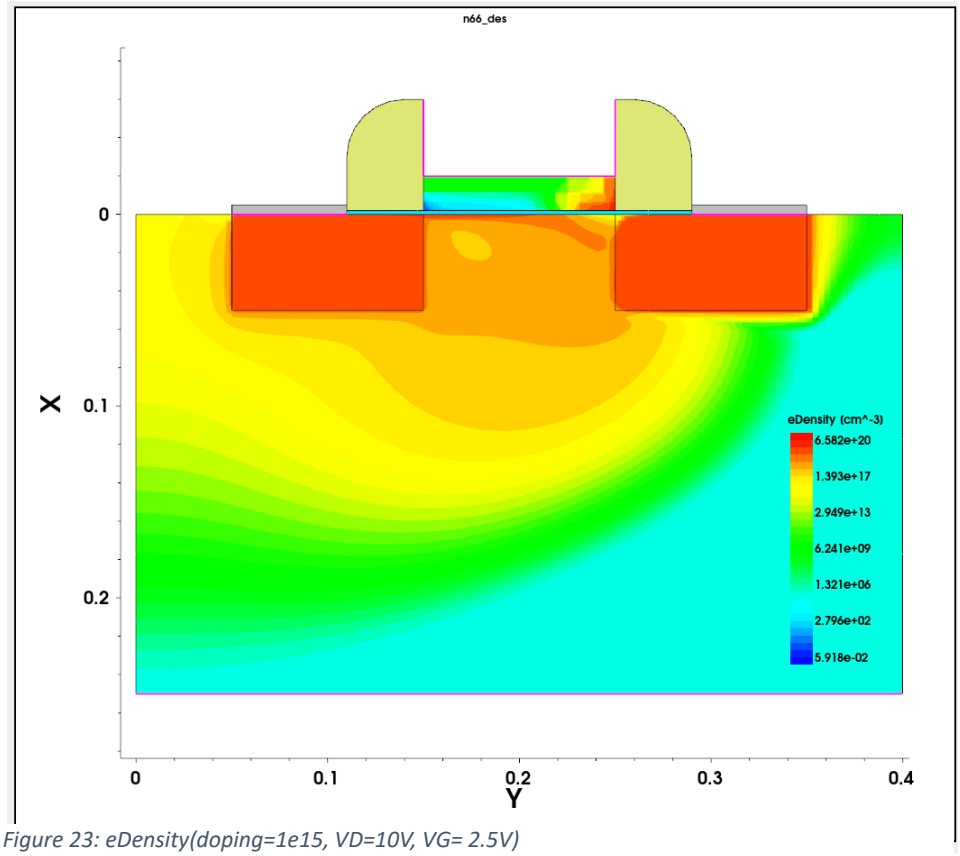


Figure 23: eDensity(doping=1e15, VD=10V, VG= 2.5V)

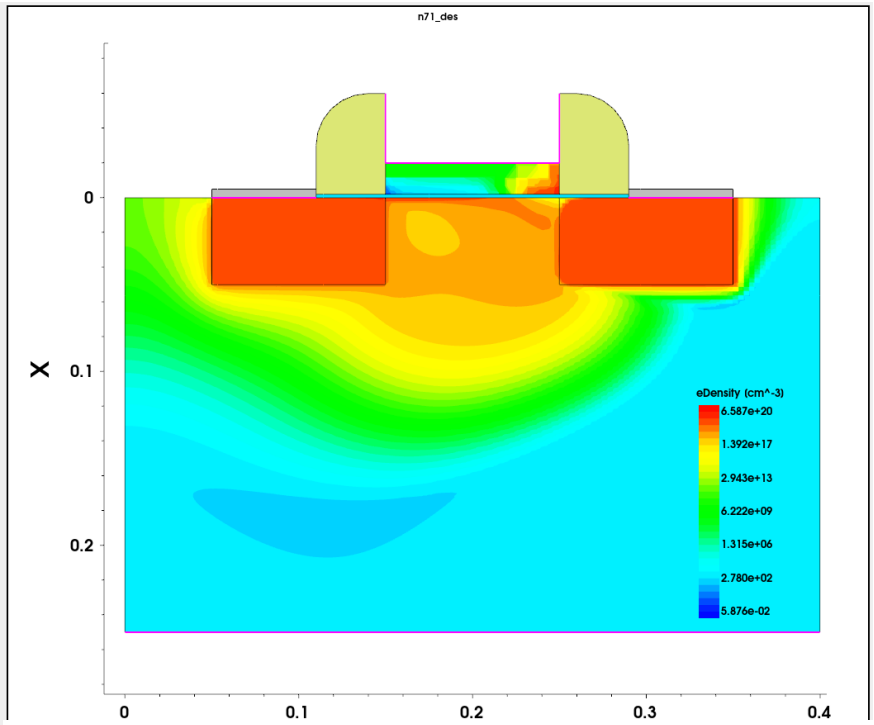


Figure 24: eDensity(doping=1e17, VD=10V, VG= 2.5V)

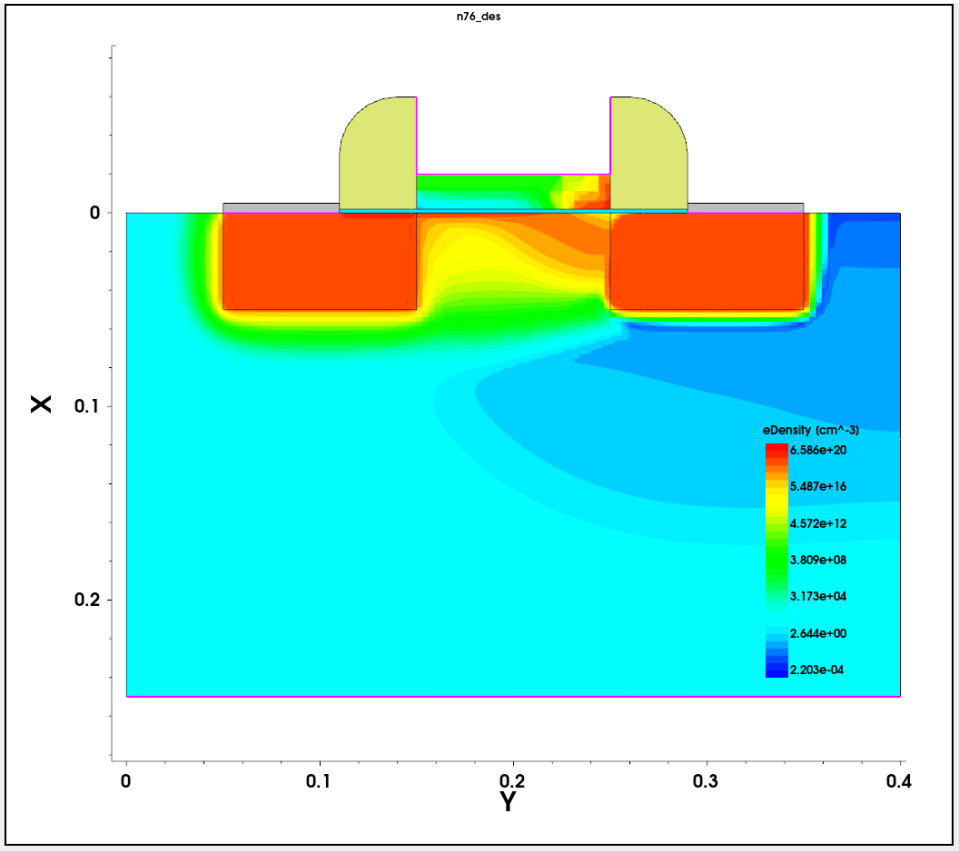


Figure 25: eDensity(doping=1e18, VD=10V, VG= 2.5V)

	SDE		SDEVICE		SVISUAL				
	sde		sdevice		svisual				
		sub_doping		VD	VG		Vtgm	Id	SS	gm
1				2.5	1.5	--	0.550	7.649e-04	3262.651	8.051e-04
2					2.5	--	0.797	1.743e-03	3109.262	1.024e-03
3		1e15	--	5	1.5	--	0.136	1.091e-03	5762.859	7.998e-04
4					2.5	--	0.535	2.093e-03	5435.620	1.065e-03
5				10	1.5	--	--	--	--	--
6					2.5	--	0.035	2.684e-03	9377.841	1.089e-03
7				2.5	1.5	--	0.844	5.256e-04	1152.661	8.010e-04
8					2.5	--	1.034	1.501e-03	1160.173	1.024e-03
9	--	1e17	--	5	1.5	--	0.504	7.955e-04	3246.151	7.986e-04
10					2.5	--	0.817	1.798e-03	3138.717	1.069e-03
11				10	1.5	--	--	--	--	--
12					2.5	--	0.354	2.349e-03	6979.553	1.095e-03
13				2.5	1.5	--	1.315	9.821e-05	114.598	5.304e-04
14					2.5	--	1.513	8.857e-04	119.914	8.978e-04
15		1e18	--	5	1.5	--	1.251	1.569e-04	114.839	6.311e-04
16					2.5	--	1.437	1.012e-03	113.098	9.518e-04
17				10	1.5	--	1.121	2.762e-04	165.461	7.285e-04
18					2.5	--	1.309	1.202e-03	164.251	1.009e-03

Figure 26: Simulation results showcasing NMOS parameters extracted from the I-V curves

I had to rerun the experiment, adding a VD value of 10V to observe punch-through effects. Additionally, two visual nodes appeared to be failing, but they were not necessary for the lab, so I didn't need to address the issue.

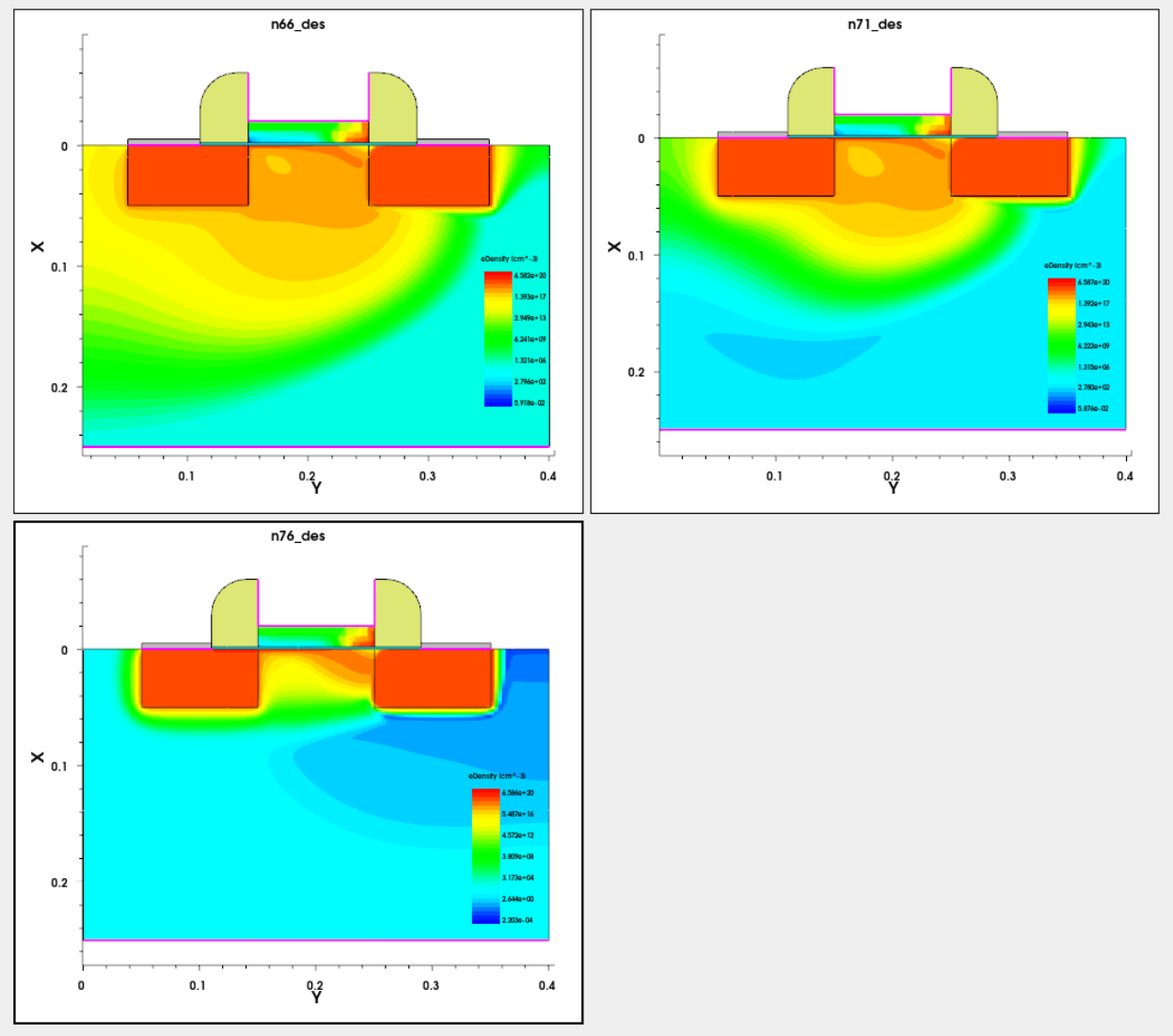


Figure 27: eDensity(doping=1e15, 1e17, 1e18, VD=10V, VG= 2.5V) (Punch-Through)

Punch-through occurs when the depletion regions of the source and drain extend and overlap, creating an unintended conductive path between them, even when the transistor should be "off."

In the simulation with VD = 10V and VG = 2.5V, punch-through happens due to the high drain voltage, causing the depletion regions to grow and overlap, allowing current to flow despite the gate voltage being insufficient to fully create a conductive channel.

For the doping levels 1e15, 1e17, and 1e18, punch-through occurs differently:

- **Doping = 1e15**: The lower doping concentration results in a broader depletion region, making the transistor more susceptible to punch-through. With VD = 10V, the depletion regions overlap more easily, enabling current flow at VG = 2.5V.
- **Doping = 1e17 and 1e18**: Higher doping concentrations lead to narrower depletion regions, making punch-through less likely at the same VD and VG. The higher doping concentration reduces the width of the depletion region, requiring higher VD or lower VG for punch-through to occur.

Conclusion

This lab demonstrated the design and simulation of an NMOS transistor using Sentaurus TCAD tools, focusing on the effects of substrate doping concentrations and operating conditions. Increasing doping concentrations raised the threshold voltage and reduced the drain current for a given gate voltage, which lowered the device's overall drive capability. The simulation also highlighted how higher doping concentrations influenced band diagrams, electron density, and charge carrier behavior. Additionally, a punch-through condition was observed at high drain-to-source voltages, further impacting device performance. Overall, the experiment emphasized the crucial role of doping concentration and voltage control in optimizing the performance of NMOS transistors for advanced electronic applications.

ZIP FILE: Finalchallenge

References

1. https://rodzah.files.wordpress.com/2011/07/how-to-write-lab-report.pdf
2. EE304- TCAD LabFinal_Challenge.pdf