Assignment 2

34349 - FPGA Design for Communication Systems

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March 23, 2022

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1 Specification

This is a specification document for a 4 port gigabit ethernet switch based on Gigabit Media Independent Interface (GMII). The ethernet frame is shown in Fig 1

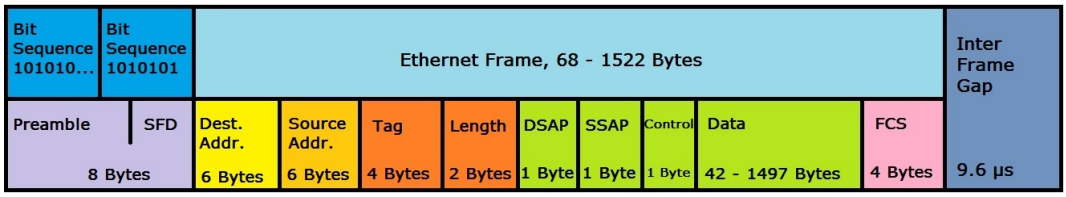

Figure 1: Ethernet Frame

1.a Overview

The switch comprises of three main blocks namely, the FCS and input buffer, MAC learning and Switching and output buffer.
The I/O pins of the switch is mentioned below:

- 32 bit rx_data (input) indicating the data sent to the switch
- 4 bit rx_ctrl (input) indicating the port sending the data to the switch
- clk (input)
- reset (input)
- 32 bit tx_data (output) indicating the data to be sent to the right port
- 4 bit tx_ctrl (output) indicating the port which receives the data

The architecture of the switch is shown in figure 2.

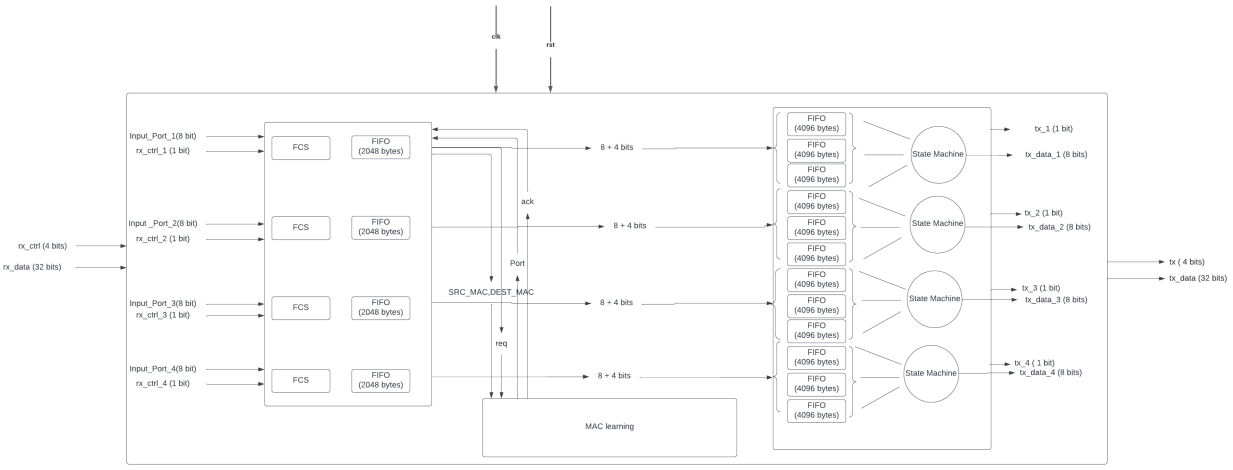

Figure 2: Switch Architecture

1.b FCS and Input Buffer

The received data is split into sets of 8-bits and sent to the corresponding input buffers based on the rx_ctrl bit. The convention for rx_ctrl used in this design is:
0001 - data received from port one
0010 - data received from port two
0100 - data received from port three
1000 - data received from port four

The data is first passed through an FCS block to check for any errors. If error free, the 8-bit data is stored the data in a FIFO buffer. The size of the FIFO buffer is 2048 bytes which is at least twice the size of Ethernet frame (1560 bytes).
Each of the FIFOs also request a handshaking with the MAC learning block. After a successful handshake, the FIFO sends both, the destination and source MAC address to the MAC learning block to retrieve the corresponding destination port. This is further explained in section 1.c.

1.c MAC Learning

The handshaking operation is initiated by a request signal received by the block from one of the four input FIFO buffers. If available, the block responds by sending an acknowledge bit to that FIFO thereby completing the handshaking operation.
The MAC learning block performs two different operations: the table lookup, in order to find the corresponding port address for the destination MAC address given in the packet and the MAC learning itself, which stores the source port and source MAC address into the table. To perform these operations, two inputs will be received in the block. The first one consists of a combination of the source and destination MAC addresses (48 + 48 bits) and the other is the request bit which indicates which port is requesting this operation to be performed.
Afterwards, the destination MAC address will be stored in a 48-bit FIFO, while the source MAC address will be stored in another 48-bit FIFO. The table that stores the MAC addresses along with their respective ports is a RAM memory. As the switch is designed to handle 8k MAC addresses, the size of the RAM is $2^{13} \times 52$ bits.
For the MAC learning operation, the source MAC address will be used. First, it will be hashed by using the CRC16 algorithm, excluding the last 3 bits since the table will only support 13 bit value for the addresses. The hashed value will correspond to the address in the table that both the MAC address is stored in the first 48 bits and the port number will be stored in the last 4 bits (52 bits).
For the table lookup operation, the destination MAC address will be used. It will be hashed as well with the same algorithm, therefore it will know in which address the corresponding port number for this MAC address is stored. The MAC address in the table is compared

with the destination MAC address, and if it matches correctly, then the block will output the corresponding port number. If not, then the block will output the transmission control bit as broadcasting. The transmission control bit convention to transmit data is:
0001 - data sent to port one
0010 - data sent to port two
0100 - data sent to port three
1000 - data sent to port four
1111 - data broadcasted to all ports

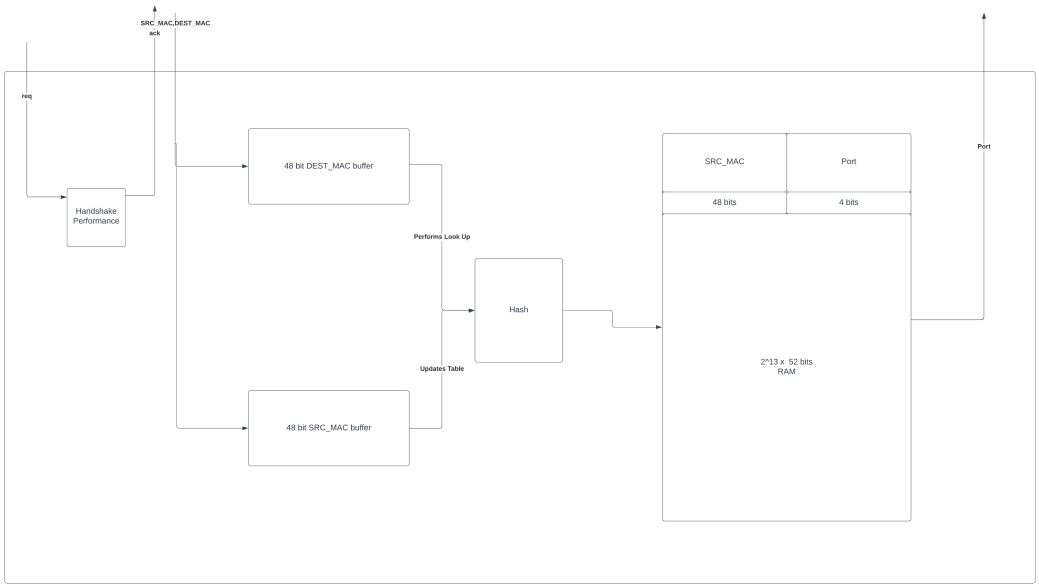

Figure 3: MAC Learning Architecture

1.d Switch and Output Buffering

The switch chosen for this design is a cross-point queuing switch as it is easy to implement as the packet arrives at the corresponding cross-point based on the port received from MAC learning. This mitigates the need for the control mechanism in the switching process. Although the memory required is of the order of N^2, it is not an issue in this design. The generic design of cross-point queuing is shown in Fig 4.

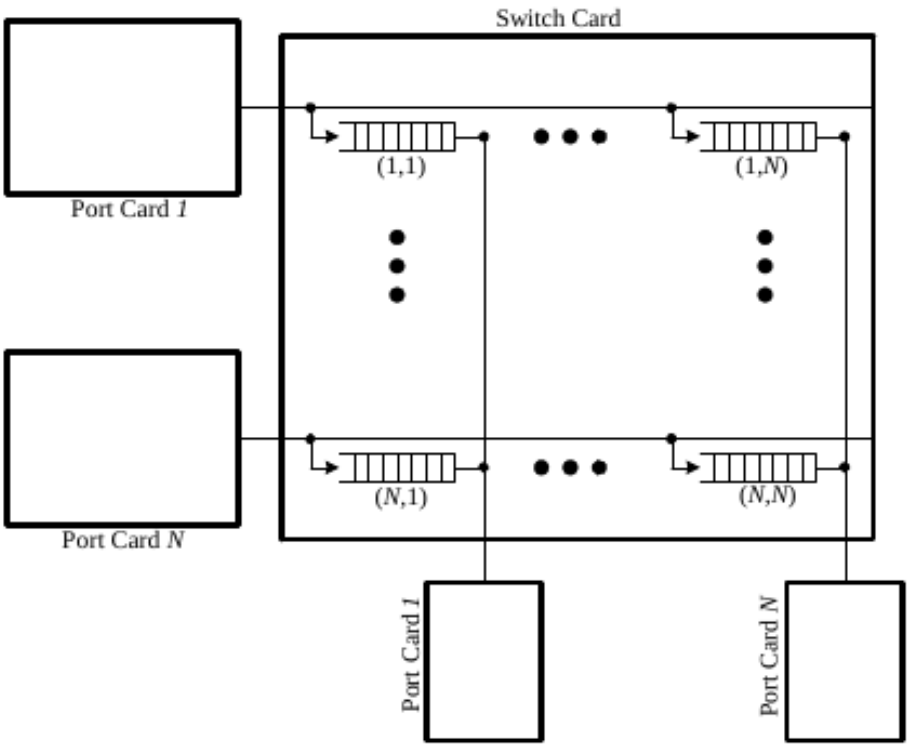

Figure 4: Cross Point Queuing

As shown in figure 4, each port has 3 output buffers indicating the queuing process and a corresponding state machine for scheduling. The size of each buffer is 4096 bytes which is approximately thrice the maximum size of ethernet frame (1560 bytes). This ensures that data can always be read from the buffer without waiting. The scheduling process ensures that data is read from each of the three buffers and is transmitted as 32 bits (4 bytes).