Specialized Subjects

15:00-17:30, Monday, August 24, 2015

Instructions

1. Do not open this booklet before the examination begins.

2. This booklet contains five problems. The number of pages is six excluding this cover sheet and blank pages. If you find missing or badly printed pages, ask the proctor for exchange.

3. Answer three problems. You can select any three out of the five. Your answer to each problem should be written on a separate sheet. You may use the reverse side of the sheet if necessary.

4. Fill the top parts of your three answer sheets as instructed below. Before submitting your answer sheets, make sure that the top parts are correctly filled.

<h2 style="text-align:center">専　門　科　目</h2>

第　　　問		受験番号				

↑ Write the problem No.　　　　　　　　　　↑ Write the applicant No.

5. Submit all the three answer sheets with the applicant number and the problem number, even if your answer is blank.

6. Answer either in Japanese or English.

7. This booklet and the scratch paper must be returned at the end of the examination.

8. This English translation is supplemental and provided for convenience of applicants. The Japanese version is the formal one.

Applicant Number	

Write your applicant No.

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Problem 1

Consider a circuit of a switched-mode power supply, consisting of a constant voltage supply (voltage E), a switch (denoted by SW), a diode (denoted by D), a coil (inductance L), a capacitor (capacitance C), terminals, and a resistor (resistance R) as shown in the figure. Let i be the current of coil, v_0 be the voltage between the terminals (as for the directions, refer to the figure). Assume that $0 < v_0 < E$, and that the forward characteristics of the diode is ideal. Answer the following questions. In (1), (2), and (3), R is not connected to the terminals.

(1) Let us short the switch for very small duration T. Let t be the time, defining $t = 0$ when the switch is shorted. Describe i as a function of t for $0 \leq t \leq T$. Here, assume $i = 0$ when $t = 0$, and ignore the change of v_0 in the meantime.

(2) Let us open the switch when $t = T$. Describe i as a function of t from $t = T$ until when i becomes 0. Here, ignore the change of v_0 as in (1).

(3) Calculate the electric energy stored in the capacitor as a consequence of (1) and (2), i.e., a single operation of "short-open" of the switch, considering the voltage of the capacitor and the current flowed into the capacitor.

(4) Let us connect R to the terminals. Describe the power consumption of the resistor with v_0 and R.

(5) After the connection of R, in order to maintain v_0 to an almost constant voltage, it is necessary to periodically make the "short-open" operations. Calculate the number of operations per unit time to maintain v_0. Here, assume that R is so large that it does not change the results of (1), (2), and (3). You may also assume that $i = 0$ when starting each "short-open" operation.
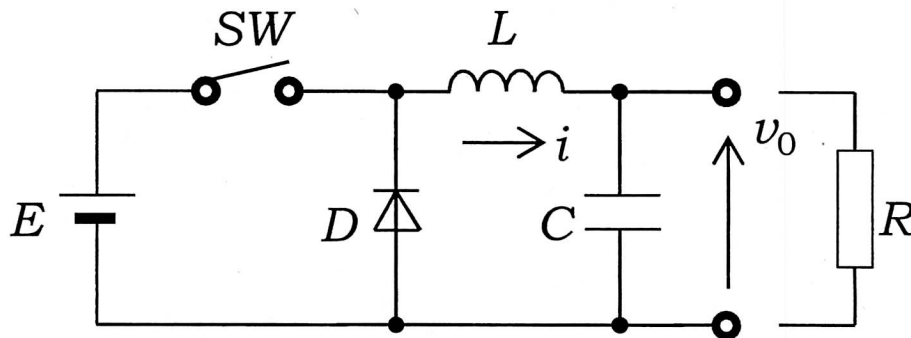
Problem 2

Answer the following questions.

(1) The following assembly code is a calculation part of a program which sequentially reads the elements of an array stored in the memory, obtains a sum of all elements, and stores the result in a designated memory address. In this code, I1 to I6 indicate labels, and r1 to r5 indicate registers. Assume that the values of register r1, r2, and r5 are initialized to the number of elements in the array, the beginning address of the array, and the address for storing the result, respectively. Fill in the each boxed blank α to δ using an adequate register number or an immediate value.

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I1:   LD     r3    0(r2)
I2:   ADD    r4    r4    r3
I3:   ADDi   r2    r2    8
I4:   ADDi   r1    [α]   [β]
I5:   BNZ    [γ]   I1:
I6:   ST     [δ]   0(r5)
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(2) Answer the relevant data dependency for the following instruction pairs (i) and (ii), respectively. Choose the correct answer from the following a, b, and c.

  (i) instruction I1 and instruction I2

  (ii) instruction I1 and instruction I3

  a. Read After Write (Flow dependency)

  b. Write After Read (Anti-dependency)

  c. Write After Write (Output dependency)

(3) Consider a pipelined processor whose stage organization and processing times are given in the following table. Answer the operation frequency of this processor. Each stage is completed within a cycle. You can assume that margins such as for mitigating clock skew are already involved in the values in the table. Note that [ps] represents 10^{-12} seconds.

Fetch	250 [ps]
Decode	100 [ps]
Register read	150 [ps]
Execute	100 [ps]
Memory access	300 [ps]
Register write	150 [ps]

(4) Consider that the code in (1) is executed with this pipelined processor. Here several instructions are expected to generate pipeline bubbles. Answer all of such instructions and the name of the relevant hazard type for each. Assume that the processor is single-issue and in-order. You can also assume the operand forwarding.

(5) Consider that the code in (1) is executed for an array of which number of elements is sufficiently large. Answer the cycles per instruction (CPI) of this processor for this execution. Assume that a fetch stage is stalled for three cycles to resolve the next instruction address when a branch instruction is fetched.

(6) Consider that a branch predictor which memorizes the last branch result associated with its program counter is introduced to this processor. Answer the instructions per second (IPS) of this processor for executing the code of (1) when the size of the array is sufficiently large.

Problem 3

Answer the following questions about the minimum spanning tree of a graph. Assume that all the weights of edges are positive in this problem.

(1) For a given graph, V is a set of vertexes and E is a set of edges. B is a subset of the vertexes and B includes an arbitrary vertex in the initial state. T is a subset of the edges, and includes no edge in the initial state. At each step of the algorithm, find the edge $\{u, v\}: u \in V - B, v \in B$ which has the minimum weight among the edges connecting the vertex of B and the vertex of $V - B$. Then, add the vertex u to B, and add the edge $\{u, v\}$ to T.

Explain that this algorithm can find the minimum spanning tree. You may use figures for your answer.

(2) Find the minimum spanning tree of the graph in the figure shown below. The number attached to each edge represents the weight of the edge.

(3) Describe the program of the algorithm explained in (1) in pseudocode by using the following variables. Use n as the number of vertexes and m as the number of edges.

$L[s, t]$	:	A matrix to describe the weights of edges. Value of the element is defined as ∞ when the edge corresponding to the element does not exist.
$nearest[s]$	:	Vertex $t \in B$ which gives the minimum $L[s, t]$ for $s \in V - B$.
$mindist[s]$	:	$mindist[s] = L[s, nearest[s]]$ for $s \in V - B$ and $mindist[s] = -1$ for $s \in B$.

(4) Estimate the order of computational complexity of the program in (3).

(5) Explain what binary heap is. You may use figures for your answer.

(6) Using binary heap may improve the efficiency of the program in (3). Explain how the binary heap should be applied for the program, and estimate its order of computational complexity. Also, discuss the case which can improve the efficiency of the program with regard to the relationship between the number of vertexes n and the number of edges m.
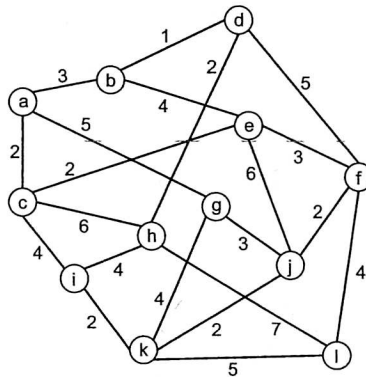
Problem 4

(1) For a four bit code of data bits x_1, x_2, x_3, x_4, consider adding one check bit x_5. Show how to generate such x_5 so that a single error can be detected.

(2) Derive the minimum Hamming distance between $(0, 0, 0, 0, 0)$ and the other code words of the code in (1). Show one of the code words of which Hamming distance to $(0, 0, 0, 0, 0)$ is the minimum Hamming distance.

(3) In a Hamming (7,4) code, three check bits x_5, x_6, x_7 are generated from the data bits x_1, x_2, x_3, x_4 according to the following equations, where "+" means exclusive OR. Show all the code words in tabular form.

$$x_5 = x_1 + x_2 + x_4$$
$$x_6 = x_2 + x_3 + x_4$$
$$x_7 = x_1 + x_2 + x_3$$

(4) Find the minimum Hamming distance between $(0, 0, 0, 0, 0, 0, 0)$ and the other code words using the table derived in (3).

(5) Using the minimum Hamming distance, show how many bit errors the code derived in (1) and the Hamming (7,4) code can correct in the maximum, respectively.

(6) Generally, even under the same bit error rates, the performance of the Hamming code deteriorates more with burst errors than with random errors. Show a countermeasure to burst errors and discuss the advantages and disadvantages of it.

Problem 5

Let us denote the Fourier transform of the signal $f(t)$ as $F(\omega)$, where t and ω represent a time variable and an angle frequency, respectively.

(1) Show the definition of the Fourier transform $F(\omega)$ of the signal $f(t)$. Also, explain the difference between the Fourier transform and the Fourier series expansion.

(2) Explain why $|F(\omega)|^2$ represents the power spectrum, i.e., the power at a certain angle frequency of ω.

(3) Derive the following Parseval's theorem in the Fourier transform and determine k.

$$\int_{-\infty}^{\infty} |f(t)|^2 dt = k \int_{-\infty}^{\infty} |F(\omega)|^2 d\omega, \ k \text{ is a real constant.}$$

You may use $|f(t)|^2 = f(t)\overline{f(t)}$, $(\overline{f(t)}$ is the complex conjugate of $f(t))$. You may also use the Fourier transform of the following convolution integrals

$$\int_{-\infty}^{\infty} f(t-\tau)g(\tau)d\tau = k' \int_{-\infty}^{\infty} F(\omega)G(\omega)e^{j\omega t}d\omega, \ j \text{ is the imaginary unit and } k' \text{ is a real constant.}$$

You may include k' when answering k.

(4) Explain the physical meaning of the Parseval's theorem in the Fourier transform.

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