Specialized Subjects

15:00-17:30, Monday, August 21, 2017

Instructions

1. Do not open this booklet before the examination begins.

2. This booklet contains five problems. The number of pages is seven excluding this cover sheet and blank pages. If you find missing or badly printed pages, ask the proctor for exchange.

3. Answer three problems. You can select any three out of the five. Your answer to each problem should be written on a separate sheet. You may use the reverse side of the sheet if necessary.

4. Fill the top parts of your three answer sheets as instructed below. Before submitting your answer sheets, make sure that the top parts are correctly filled.

<div align="center">

専 門 科 目

</div>

| 第　　　問 | | 受験番号 | | | | |

↑ Write the problem No.　　　　　　　　　　　　　　　↑ Write the examinee No.

5. Submit all the three answer sheets with the examinee number and the problem number, even if your answer is blank.

6. Answer either in Japanese or in English.

7. This booklet and the scratch paper must be returned at the end of the examination.

8. This English translation is supplemental and provided for convenience of applicants. The Japanese version is the formal one.

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Problem 1

(1) Consider a power supply $e(t)$ which is a rectangular pulse with time duration T as shown in Fig. 1. Obtain the Laplace transform of $e(t)$.

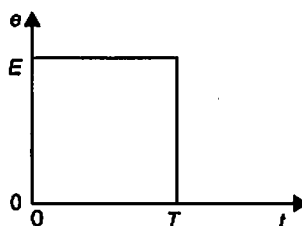$$e(t) = \begin{cases} E & (0 < t \le T) \\ 0 & (\text{otherwise}) \end{cases}$$

Figure 1

(2) Obtain the current $i(t)$ when the power supply $e(t)$ is applied to the circuit consisting of a resistor (resistance R) and a capacitor (capacitance C) shown in Fig. 2 under each of the following conditions (a) and (b). The initial charge of the capacitor is set to 0. The time constant of the circuit is not negligible compared to T.
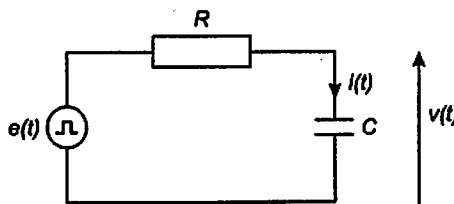
(a) $0 < t \le T$

(b) $T < t \le 2T$

Figure 2

(3) The rectangular pulse of (1) is repeated at a cycle of $2T$ as shown in Fig. 3. This periodic rectangular wave is set to the power supply $e(t)$. $v(nT)$ is the voltage of the capacitor at time nT (n is a positive integer). Obtain $v(T)$, $v(2T)$, $v(3T)$, and $v(4T)$.
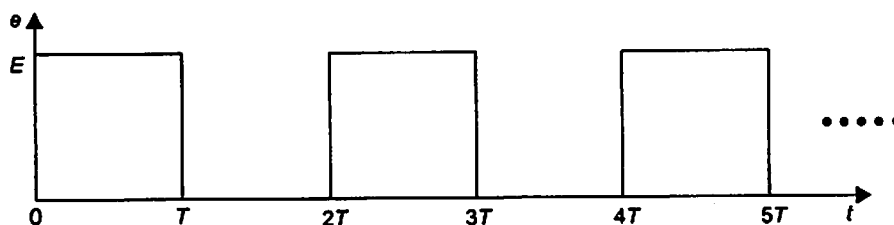

Figure 3

(4) Obtain the current $i(t)$ under each of the following conditions.

(a) Express $i(t)$ for $2nT < t \le (2n+1)T$ by using $v(2nT)$.

(b) Express $i(t)$ for $(2n+1)T < t \le 2(n+1)T$ by using $v((2n+1)T)$.

(5) Show a recurrence equation of $v(2nT)$.

(6) Obtain $\lim_{n \to \infty} v(2nT)$.

(7) Obtain $v(2nT)$ as a function of n.

Problem 2

We design the following modular arithmetic circuit C. C keeps receiving a 2-bit integer $I_1 I_0$ at every cycle in synchronization with the clock. C has a 2-bit output $O_1 O_0$, and keeps outputting the remainder obtained by dividing the sum of the input values up to that time by 4. Both input and output are expressed as unsigned integers, and I_1 and O_1 are assumed to be the MSB. The sum of the input values is assumed to be 0 in the initial state of the circuit. Answer the following questions.

(1) Assume that C is designed as a circuit whose output is determined only by the circuit state at that time. Show its state transition diagram with the least number of states.

(2) Show the state transition table of the state transition diagram designed in (1) as shown in the table below. Here, we assume that the state is held in an n-bit register and is represented as $S_{n-1} \ldots S_0$. Also, $S'_{n-1} \ldots S'_0$ represents the next state. The state should be assigned so that the circuit that generates the output from the state register is the simplest.

$I_1 I_0 S_{n-1} \ldots S_0$	$S'_{n-1} \ldots S'_0$
$0\,0\,0 \ldots 0$	
$\vdots$	

(3) Show the logical expression determining the next state of each bit of the state register in disjunctive normal form (sum-of-products form). Note that the number of terms should be minimized by using a Carnot diagram.

(4) In a manner embodying Fig. 1, show the circuit that realizes the logical expression derived in (3) by assembling AND-gates, OR-gates, NOT-gates, and D-flip-flops. You may use a notation meaning the inversion of the input value as in Fig. 2. Also, you may omit the wires for clock supply. Assume that the flip-flops are ideal.
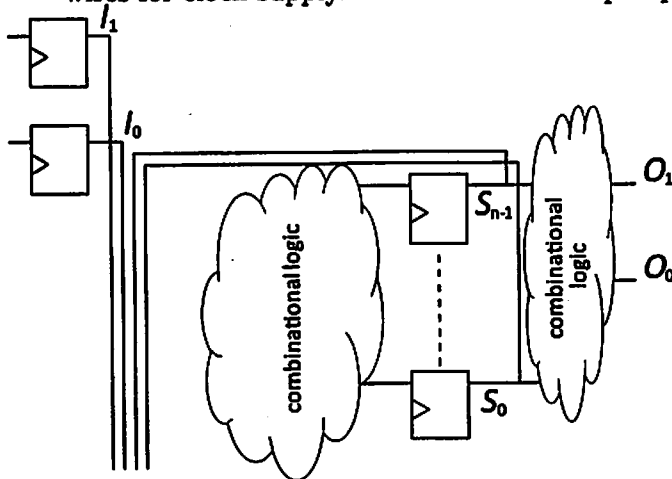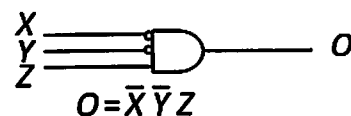

Figure 1

$$O = \overline{X}\,\overline{Y}\,Z$$

Figure 2

Problem 3

Answer the following questions about directed graphs.
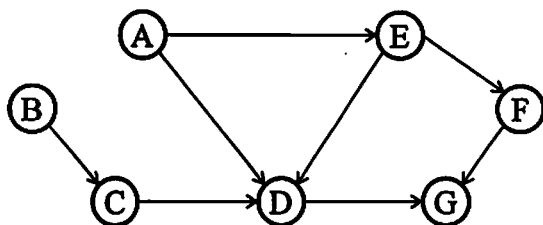

Figure 1:

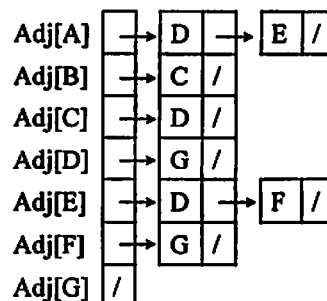

Figure 2:

```
function DFS1(Vertex u)
    visited[u] = TRUE
    print u
    foreach v in Adj[u]
        if(visited[v] != TRUE)
            DFS1(v)
```

Figure 3:

```
function DFS2(Vertex u)
    visited[u] = TRUE
    foreach v in Adj[u]
        if(visited[v] != TRUE)
            DFS2(v)
    print u
```

Figure 4:

(1) Consider the directed graph shown in Fig. 1. The Adj[·] in Fig. 2 represent the edges of this graph as adjacency lists. For this directed graph, you executed the function shown in pseudocode in Fig. 3 as DFS1(A), and the output was ADGEF. Show the output you will see when you execute the function in Fig. 4 as DFS2(A) for the same directed graph.

(2) The edge pointing from vertex u to vertex v is denoted by (u, v). A topological sort of a directed graph is an ordering of all its vertices such that, for any edge (u, v) in the graph, u always appears before v. Give an example of a topological sort for the directed graph shown in Fig. 1.

(3) Give a real-world problem for which a topological sort is useful, and explain the reason briefly.

(4) An algorithm for computing a topological sort can be constructed by using a graph-traversal function similar to the ones shown in Figs. 3 and 4. Figure 5 shows pseudo code for computing a topological sort. Describe the content of the function DFS in pseudo code. Note that in Fig. 5, V is the set of the nodes of the graph, and s is an object that implements a stack and has the following three methods:

- empty(): returns TRUE if the stack is empty, or FALSE otherwise.
- pop(): returns the value at top of the stack. The value is removed from the stack.
- push(X): stores a value X into the stack.

(5) Explain the time complexity of the algorithm shown in Fig. 5.

(6) Give a brief description of another algorithm for computing a topological sort and its time complexity.

```
Bool visited[|V|]
Stack s

function DFS(Vertex u)
┌─────────────────────────────┐
│                             │
│                             │
│                             │
└─────────────────────────────┘


function TopologicalSort()
    foreach v in V
        if (visited[v] != TRUE)
        DFS(v)

    while(s.empty() != TRUE)
        print(s.pop())
```

Figure 5:

Problem 4

We transfer IP packets using TCP/IP from a server to clients in the system shown in the figure. The sizes of transferred IP packets are all M [Bytes]. The bandwidth of each transmission line is B_i [Bytes/sec], and the transmission delay is D_i [sec] ($1 \leq i \leq 3$).

(1) During the IP packet transmission, it is assumed that IP packets may be discarded in the transmission path. In TCP, in order to start an IP packet communication, the information required to start the communication must be synchronized between a server and a client. Describe the procedure at a server and at a client to synchronize the information between a server and a client using state transition diagrams.

(2) Show the minimum interval of IP packet arrivals observed at a client, when the server continuously transmits the IP packets to the same client.

(3) In order to provide error free data transmission between a server and a client, TCP transfers IP packets while confirming the acknowledgment of IP packets' arrival. When the transmission delay of IP packets between a server and a client is large and IP packets are transferred confirming the acknowledgment of IP packets' arrival with every IP packet, high speed data transmission cannot be achieved. In TCP, therefore, a method to improve the speed of data transmission, called window control, is applied. Explain the operating principle and the condition required to achieve the maximum transmission speed.

(4) Consider the case of the data transmission of multiple contents from a server to clients. When the contents are transmitted sequentially, the transmission of the last contents must be suspended until the completion of the transmission of the first contents. Explain a method to solve this problem in TCP.

Next, consider the following system; there are a large number of clients with very large transmission delays to a server, and these clients request the asynchronous transmission of the same contents.

(5) When D_2 [sec] in the figure is very large, describe a method to reduce the transmission delay from a server to clients.

(6) In order to reduce the load of a server against a large volume of transmission requests, methods to distribute the transmission requests from clients by the installation of multiple servers in the Internet are applied. Describe three methods.

Client

Router(R_1) Router(R_2) Server

B_I : Bandwidth[Bytes/sec]
D_I : Delay[sec]
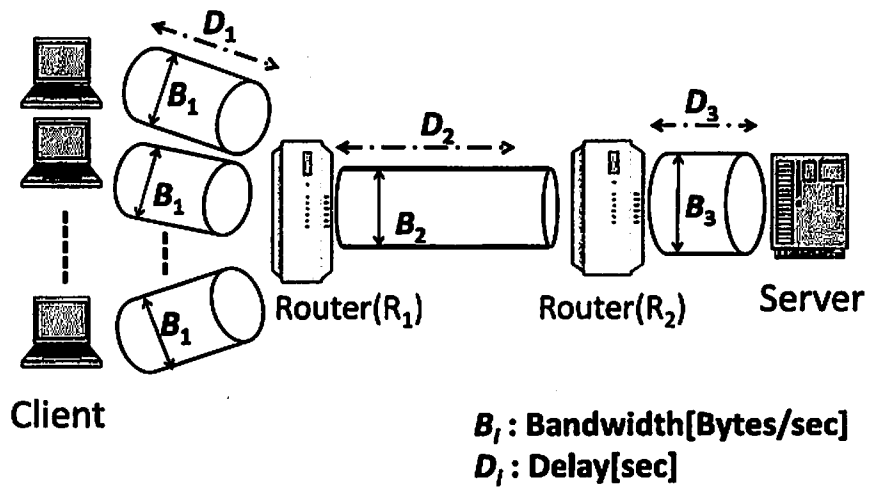
Problem 5

Answer the following questions about discrete signal processing. Here, T is the sampling interval.

(1) Show the definition of the Z-transform $X(z)$ for the discrete signal series x_n ($n = 0, 1, 2, \cdots$), which is defined for $n \geq 0$. Here, z is a complex variable.

(2) Derive the transfer function $H(s)$ in the s-domain (the Laplace transform domain) of the circuit in Fig. 1.

(3) The relationship between the Laplace transform and the Z-transform is described as $z = e^{sT}$. Derive the following approximation.

$$s \simeq \frac{2}{T} \frac{1 - z^{-1}}{1 + z^{-1}}.$$

You can use the following equation if necessary.

$$e^x \simeq 1 + x.$$

(4) Convert $H(s)$ to the transfer function $H(z)$ in the z-domain by using the approximation derived in (3). Here, we assume $T = 1$.

(5) Show a schematic of a discrete signal circuit that corresponds to $H(z)$ in (4).

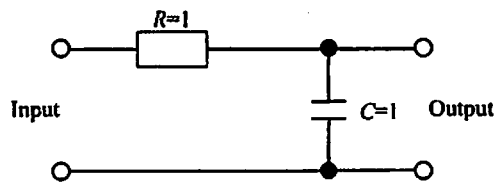(6) By taking the same procedure, show a schematic of a discrete signal circuit for the circuit shown in Fig. 2.
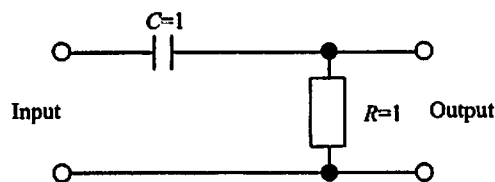

Figure 1

Figure 2

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