

## 1. Description

## 1.1. Project

Project Name	Light_Detector
Board Name	NUCLEO-F411RE
Generated with:	STM32CubeMX 6.1.1
Date	05/17/2021

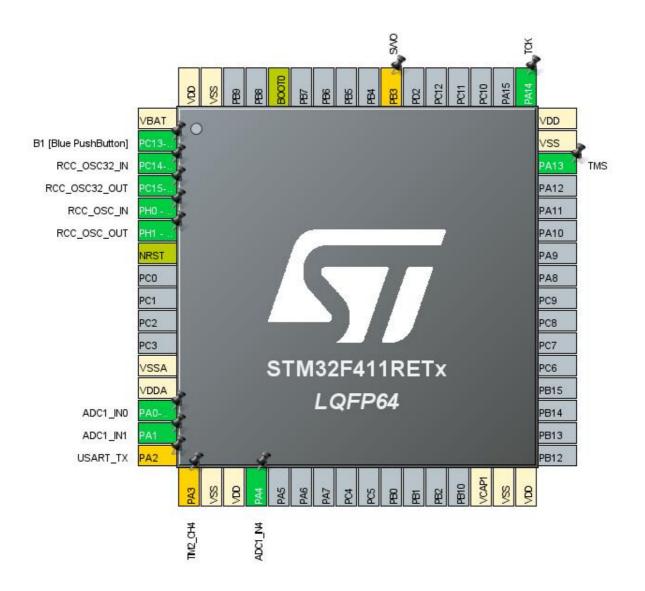
### 1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F411
MCU name	STM32F411RETx
MCU Package	LQFP64
MCU Pin number	64

## 1.3. Core(s) information

Core(s)	Arm Cortex-M4	

## 2. Pinout Configuration

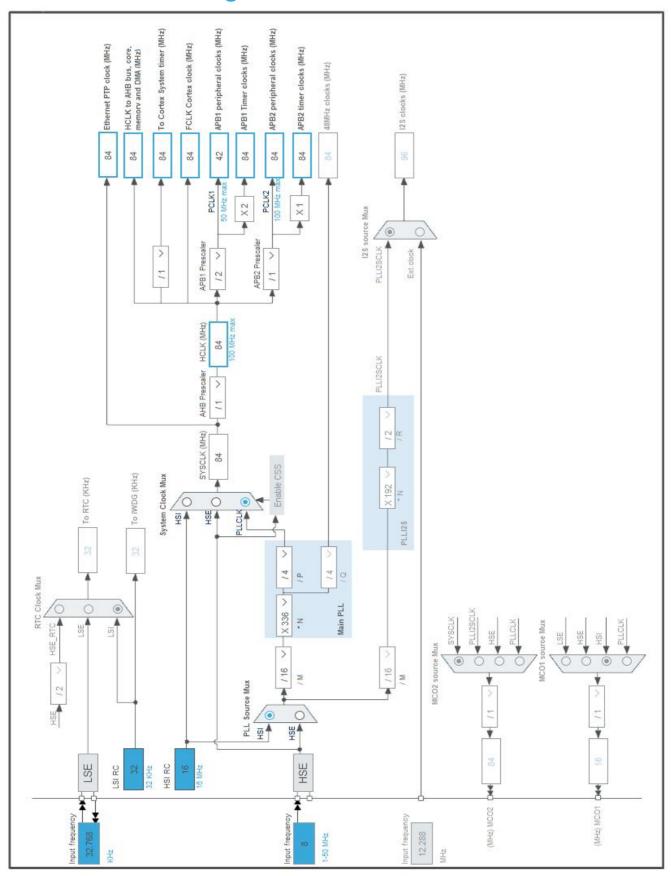


# 3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13-ANTI_TAMP	I/O	GPIO_EXTI13	B1 [Blue PushButton]
3	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
4	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
5	PH0 - OSC_IN	I/O	RCC_OSC_IN	
6	PH1 - OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
12	VSSA	Power		
13	VDDA	Power		
14	PA0-WKUP	I/O	ADC1_IN0	
15	PA1	I/O	ADC1_IN1	
16	PA2 *	I/O	USART2_TX	USART_TX
17	PA3 *	I/O	TIM2_CH4	
18	VSS	Power		
19	VDD	Power		
20	PA4	I/O	ADC1_IN4	
30	VCAP1	Power		
31	VSS	Power		
32	VDD	Power		
46	PA13	I/O	SYS_JTMS-SWDIO	TMS
47	VSS	Power		
48	VDD	Power		
49	PA14	I/O	SYS_JTCK-SWCLK	TCK
55	PB3 *	I/O	SYS_JTDO-SWO	SWO
60	воото	Boot		
63	VSS	Power		
64	VDD	Power		

<sup>\*</sup> The pin is affected with a peripheral function but no peripheral mode is activated

## 4. Clock Tree Configuration



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## 5. Software Project

### 5.1. Project Settings

Name	Value	
Project Name	Light_Detector	
Project Folder	C:\Users\Windows10\Desktop\CU\Year2\Semester_2\EmbedSys\STM32CubelD	
Toolchain / IDE	STM32CubeIDE	
Firmware Package Name and Version	STM32Cube FW_F4 V1.25.2	
Application Structure	Advanced	
Generate Under Root	Yes	
Do not generate the main()	No	
Minimum Heap Size	0x200	
Minimum Stack Size	0x400	

### 5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power	No
consumption)	
Enable Full Assert	No

### 5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	SystemClock_Config	RCC
3	MX_ADC1_Init	ADC1

## 6. Power Consumption Calculator report

#### 6.1. Microcontroller Selection

Series	STM32F4
Line	STM32F411
MCU	STM32F411RETx
Datasheet	DS10314_Rev6

#### 6.2. Parameter Selection

Temperature	25
Vdd	1.7

### 6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

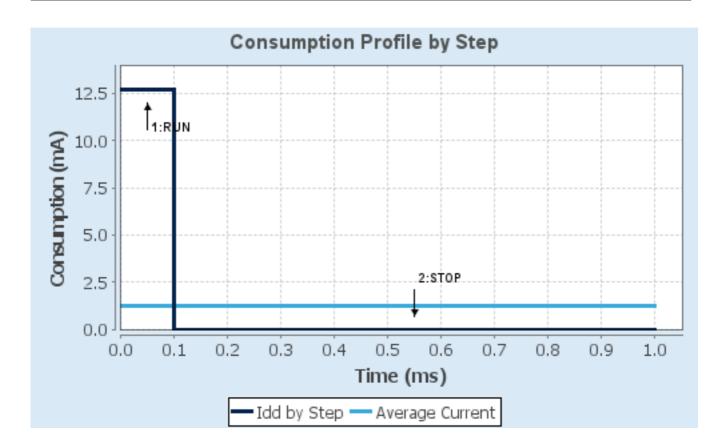
### 6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	1.7	1.7
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	SRAM	n/a
CPU Frequency	100 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator_LPLV Flash-
		PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	12.7 mA	9 μΑ
Duration	0.1 ms	0.9 ms
DMIPS	125.0	0.0
Ta Max	103.99	105
Category	In DS Table	In DS Table

### 6.5. Results

Sequence Time	1 ms	Average Current	1.28 mA
Battery Life	3 months, 19	Average DMIPS	125.0 DMIPS
	days, 6 hours	-	

### 6.6. Chart



## 7. Peripherals and Middlewares Configuration

7.1. ADC1 mode: IN0 mode: IN1 mode: IN4

7.1.1. Parameter Settings:

ADCs\_Common\_Settings:

Mode Independent mode

ADC\_Settings:

Clock Prescaler PCLK2 divided by 4

Resolution 12 bits (15 ADC Clock cycles)

Data Alignment Right alignment
Scan Conversion Mode Disabled
Continuous Conversion Mode Disabled
Discontinuous Conversion Mode Disabled

DMA Continuous Requests Disabled

End Of Conversion Selection EOC flag at the end of single channel conversion

ADC\_Regular\_ConversionMode:

Number Of Conversion 1

External Trigger Conversion Source Regular Conversion launched by software

External Trigger Conversion Edge None Rank 1

Channel Channel 0
Sampling Time 3 Cycles

ADC\_Injected\_ConversionMode:

Number Of Conversions 0

WatchDog:

Enable Analog WatchDog Mode false

7.2. RCC

High Speed Clock (HSE): BYPASS Clock Source

Low Speed Clock (LSE): Crystal/Ceramic Resonator

7.2.1. Parameter Settings:

**System Parameters:** 

VDD voltage (V) 3.3

Instruction Cache Enabled
Prefetch Buffer Enabled
Data Cache Enabled

Flash Latency(WS) 2 WS (3 CPU cycle)

**RCC Parameters:** 

HSI Calibration Value 16
TIM Prescaler Selection Disabled
HSE Startup Timout Value (ms) 100
LSE Startup Timout Value (ms) 5000

**Power Parameters:** 

Power Regulator Voltage Scale Power Regulator Voltage Scale 1

7.3. SYS

**Debug: Serial Wire** 

**Timebase Source: SysTick** 

<sup>\*</sup> User modified value

## 8. System Configuration

## 8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0-WKUP	ADC1_IN0	Analog mode	No pull-up and no pull-down	n/a	
	PA1	ADC1_IN1	Analog mode	No pull-up and no pull-down	n/a	
	PA4	ADC1_IN4	Analog mode	No pull-up and no pull-down	n/a	
RCC	PC14- OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15- OSC32_OU T	RCC_OSC32_O UT	n/a	n/a	n/a	
	PH0 - OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1 - OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS- SWDIO	n/a	n/a	n/a	TMS
	PA14	SYS_JTCK- SWCLK	n/a	n/a	n/a	TCK
Single Mapped Signals	PA2	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	USART_TX
	PA3	TIM2_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB3	SYS_JTDO- SWO	n/a	n/a	n/a	SWO
GPIO	PC13- ANTI_TAMP	GPIO_EXTI13	External Interrupt Mode with Falling edge trigger detection	No pull-up and no pull-down	n/a	B1 [Blue PushButton]

### 8.2. DMA configuration

nothing configured in DMA service

### 8.3. NVIC configuration

## 8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority		
Non maskable interrupt	true	0	0		
Hard fault interrupt	true	0	0		
Memory management fault	true	0	0		
Pre-fetch fault, memory access fault	true	0	0		
Undefined instruction or illegal state	true	0	0		
System service call via SWI instruction	true	0	0		
Debug monitor	true	0	0		
Pendable request for system service	true	0	0		
System tick timer	true	0	0		
PVD interrupt through EXTI line 16	unused				
Flash global interrupt	unused				
RCC global interrupt	unused				
ADC1 global interrupt	unused				
EXTI line[15:10] interrupts	unused				
FPU global interrupt	unused				

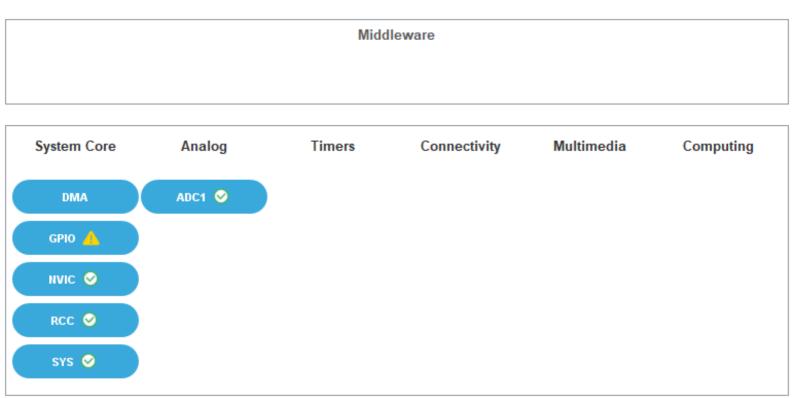
### 8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init	Generate IRQ handler	Call HAL handler
	sequence ordering	nanulei	
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true

#### \* User modified value

## 9. System Views

- 9.1. Category view
- 9.1.1. Current



### 10. Docs & Resources

Type Link

Datasheet http://www.st.com/resource/en/datasheet/DM00115249.pdf

Reference http://www.st.com/resource/en/reference\_manual/DM00119316.pdf

manual

Programming http://www.st.com/resource/en/programming manual/DM00046982.pdf

manual

Errata sheet http://www.st.com/resource/en/errata\_sheet/DM00137034.pdf

Application note http://www.st.com/resource/en/application\_note/CD00167594.pdf

Application note http://www.st.com/resource/en/application\_note/CD00211314.pdf

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Application note http://www.st.com/resource/en/application\_note/CD00264342.pdf

Application note http://www.st.com/resource/en/application\_note/CD00264379.pdf

Application note http://www.st.com/resource/en/application\_note/DM00024853.pdf

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