CS 508 Assignment 7

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Consider the following RISC-V assembly language code sequence:

```
loop:   slli    s2,s1,2       #1
        add     s3,s0,s2      #2
        lw      t1,0(s3)      #3
        mul     t2,t1,t1      #4
        add     t3,t2,t1      #5
        sw      t3,0(s3)      #6
        addi    s1,s1,1       #7
        blt     s1,t0,loop    #8
```

1. A data dependency exists in a sequence of instructions when an instruction reads a register operand whose value is being written by an instruction earlier in the sequence. Identify all data dependencies in the code sequence. Write the dependency in the following format:

   Instruction #___ depends on instruction #___ for the register ___.

   Instruction #1 depends on instruction #7 for the register s1.(If loop already occurred)
   Instruction #2 depends on instruction #1 for the register s2.
   Instruction #3 depends on instruction #2 for the register s3.
   Instruction #4 depends on instruction #3 for the register t1.
   Instruction #5 depends on instruction #4 for the register t2.
   Instruction #5 depends on instruction #3 for the register t1.
   Instruction #6 depends on instruction #2 for the register s3.

2. Data hazards occur in a pipeline when an instruction needs the result of a previous instruction that is still executing in the pipeline. Data hazards are the result of data dependencies but not all data dependencies will result in a hazard. The above code sequence will execute in the RISC-V 5-stage pipeline as described in the lecture, but does not implement data forwarding. In the list of data dependencies you identified in question 1, identify which dependency will result in a data hazard by placing an asterisk (*) in front of the dependency.

   Instruction #1 depends on instruction #7 for the register s1.(If loop already occurred)
   *Instruction #2 depends on instruction #1 for the register s2.
   *Instruction #3 depends on instruction #2 for the register s3.
   *Instruction #4 depends on instruction #3 for the register t1.
   *Instruction #5 depends on instruction #4 for the register t2.
   *Instruction #5 depends on instruction #3 for the register t1.
   Instruction #6 depends on instruction #2 for the register s3.

3. Many data hazards can be eliminated by implementing data forwarding; some cannot. For this question, the RSIC-V 5-stage pipeline implements data forwarding that allows values from the output of the ALU and memory access to be forwarded to the ALU input as illustrated in the lecture. For the data hazards that you identified in question 2 (those that you identified with asterisks), identify which hazards are eliminated with data forwarding by placing a plus sign (+) in front of the asterisk. For example, a hazard eliminated by data forwarding will be marked with both a plus sign and asterisk: + *.

Instruction #1 depends on instruction #7 for the register s1.(If loop already occurred)
+*Instruction #2 depends on instruction #1 for the register s2.
+*Instruction #3 depends on instruction #2 for the register s3.
+*Instruction #4 depends on instruction #3 for the register t1.
+*Instruction #5 depends on instruction #4 for the register t2.
+*Instruction #5 depends on instruction #3 for the register t1.
Instruction #6 depends on instruction #2 for the register s3.

4. a. Consider the execution of the instructions in the pipeline without data forwarding in question 2. How many total cycles will it take for the instructions to complete execution?

   24 Cycles

   b. Consider the execution of the instruction in the pipeline with data forwarding in question 3. How many total cycles will it take for the instructions to complete execution?

   12 Cycles