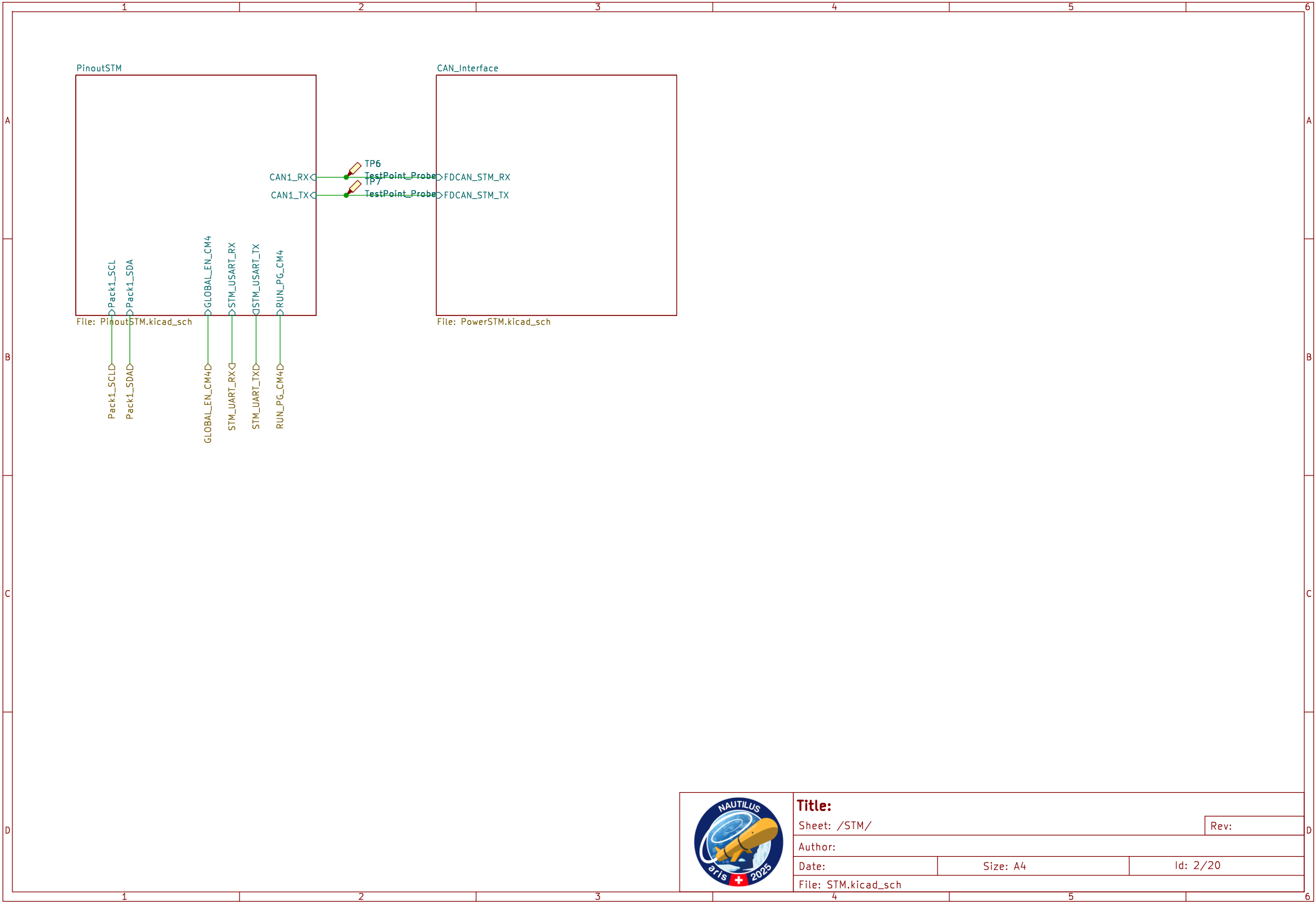
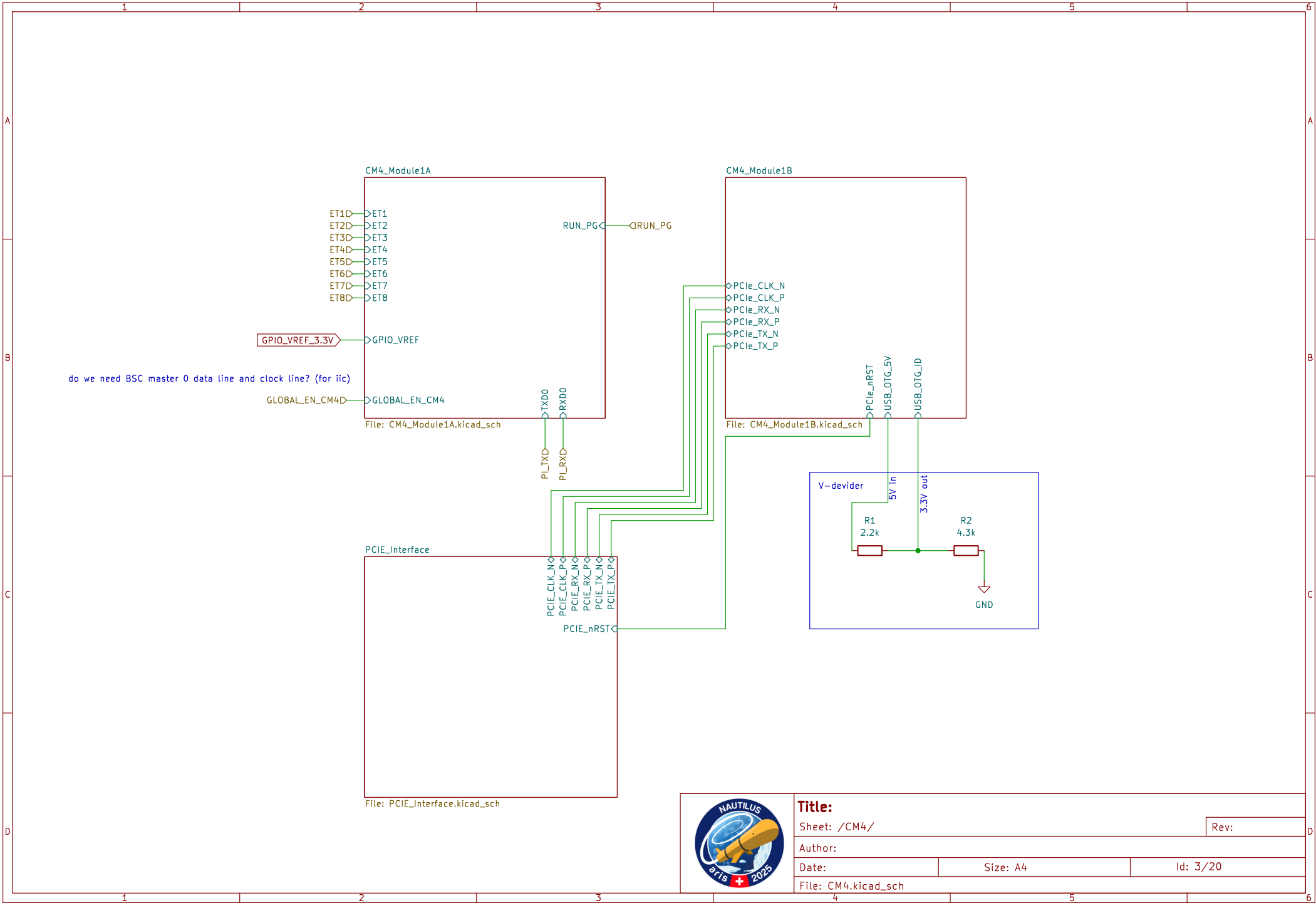


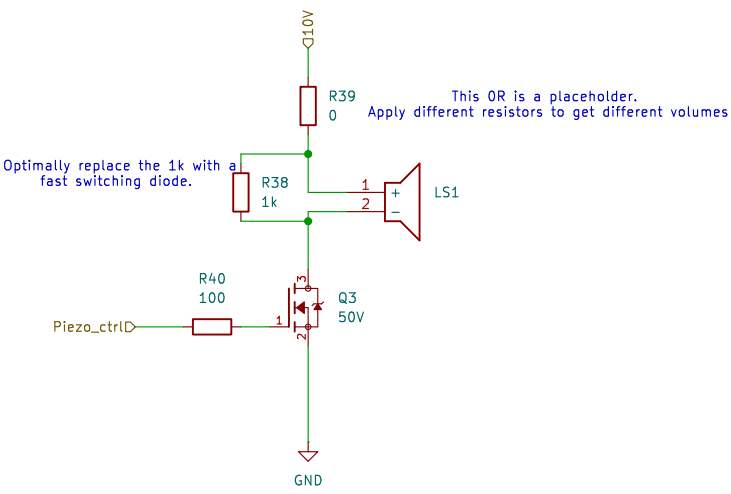
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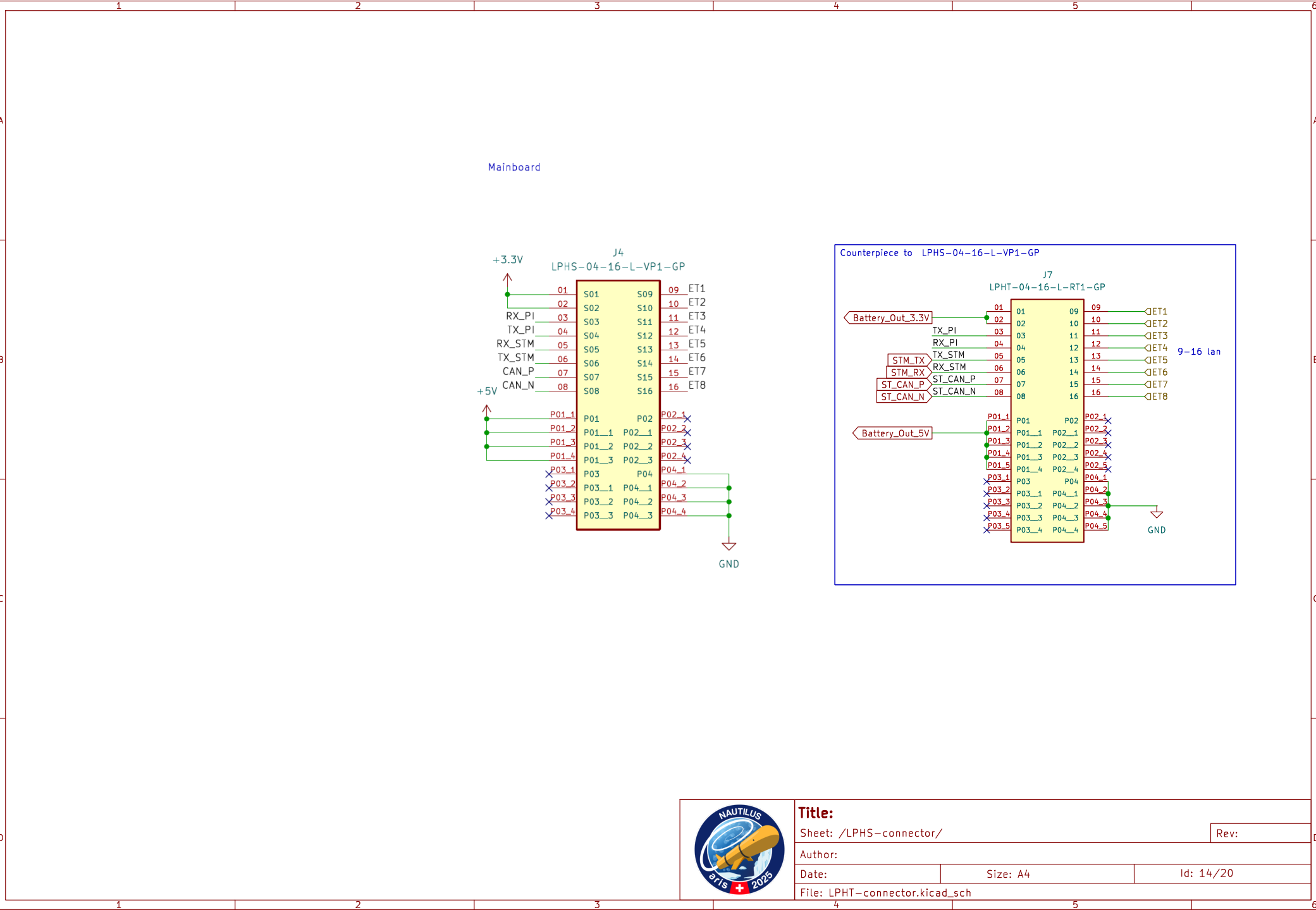
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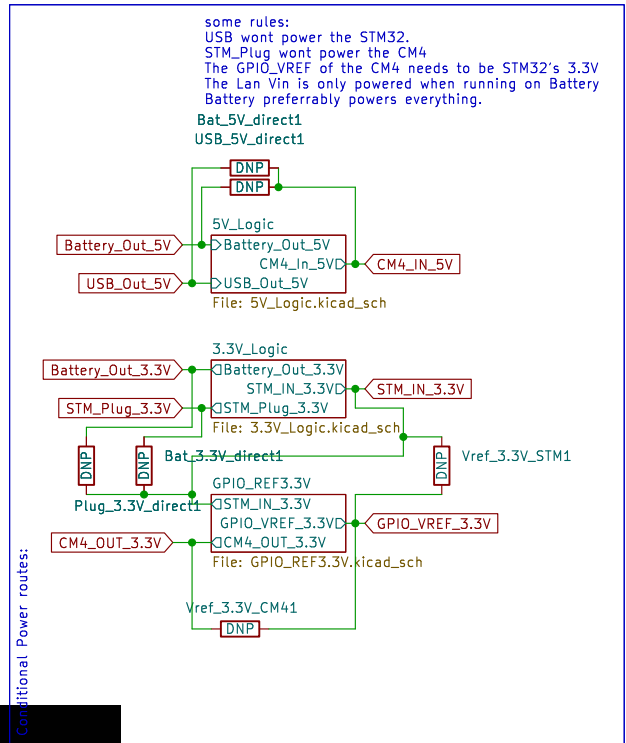
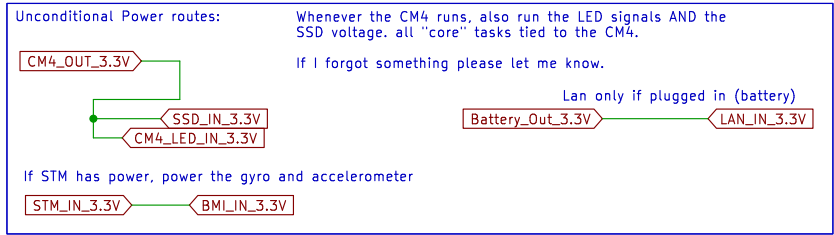
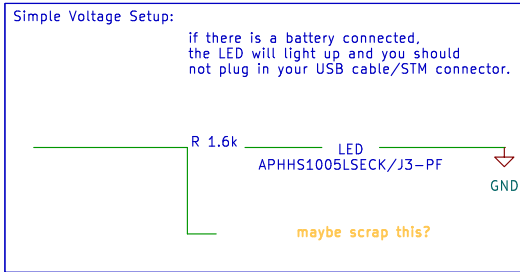
Not in the PCB yet as we dont know if we actually need it.



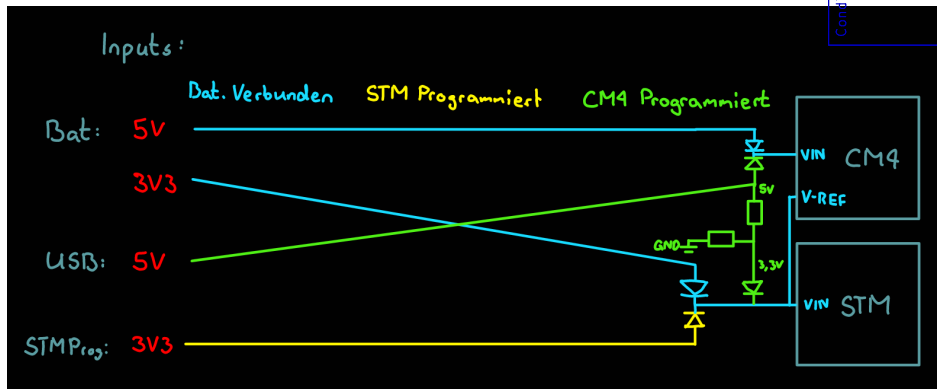
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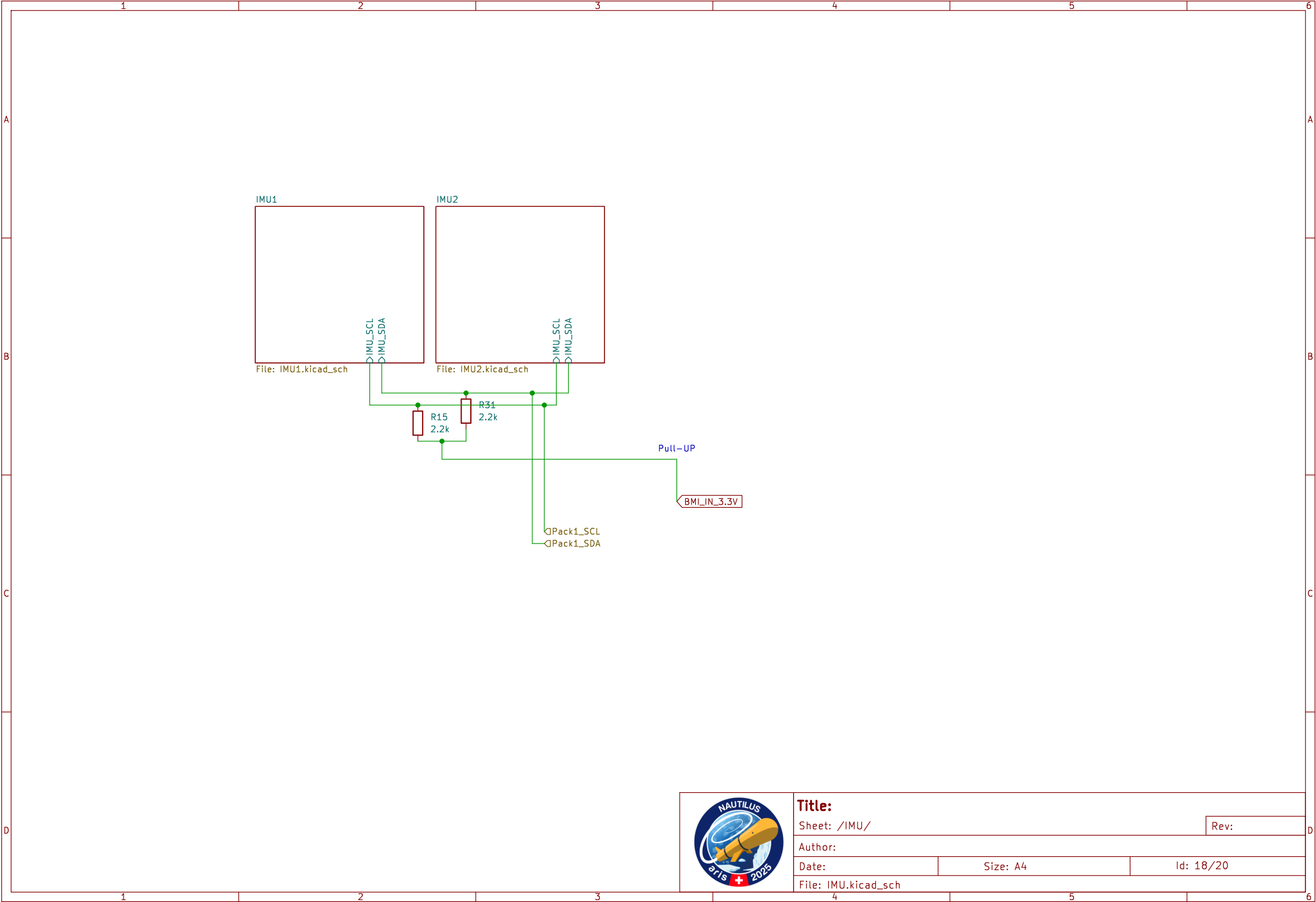
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Wont work... diodes are not perfect...



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File: Power_logic.kicad_sch		



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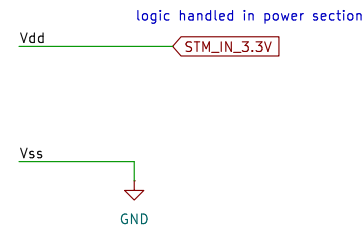
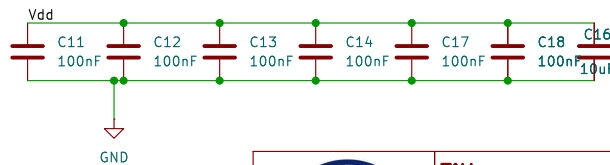
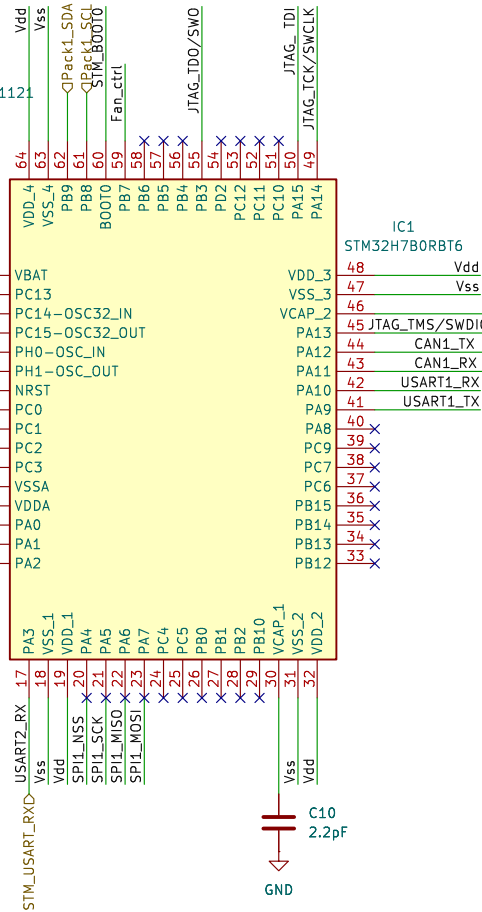
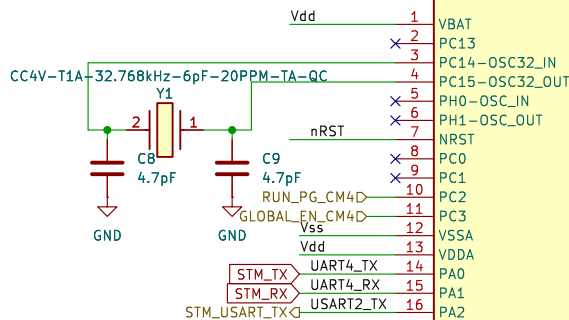
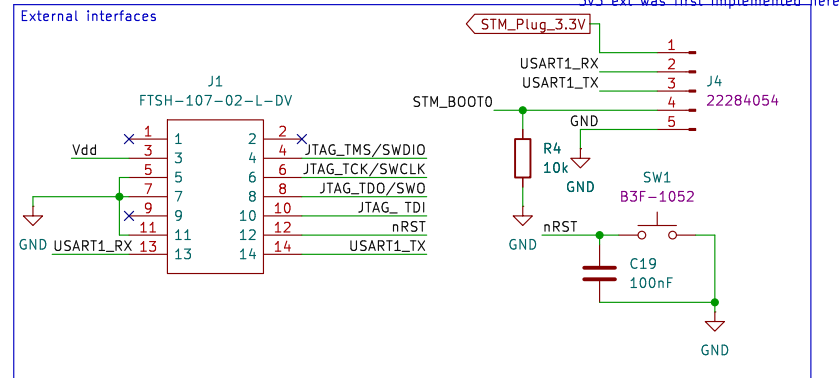
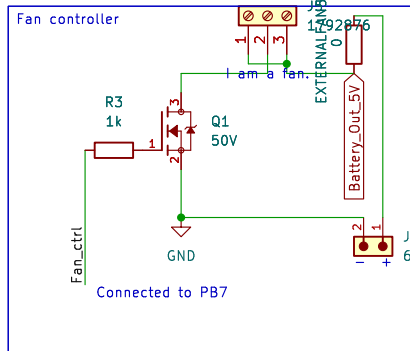
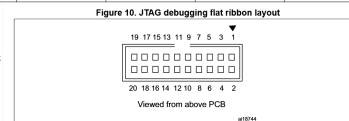
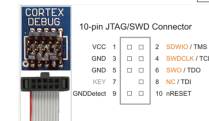


Table 5. JTAG/SWD cable connections on STLINK-V2-ISOL

Pin no.	ST-LINK/V2 connector (CN3)	ST-LINK/V2 function	Target connection (JTAG)	Target connection (SWD)
1	VAPP	Target VCC	MCU VDD <sup>(1)</sup>	MCU VDD <sup>(1)</sup>
3	TRST	JTAG TRST	NJTRST	GND <sup>(2)</sup>
4	Not connected	Not connected	Not connected	Not connected
5	TDI	JTAG TDO	JTDI	GND <sup>(2)</sup>
6	Not connected	Not connected	Not connected	Not connected
7	TMS_SWDIO	JTAG TMS, SW IO	JTMS	SWDIO
8	Not connected	Not connected	Not connected	Not connected
9	TCK_SWCLK	JTAG TCK, SW CLK	JTCK	SWCLK
10	Not used <sup>(5)</sup>	Not used <sup>(5)</sup>	Not connected <sup>(5)</sup>	Not connected <sup>(5)</sup>
11	Not connected	Not connected	Not connected	Not connected
12	GND	GND	GND <sup>(3)</sup>	GND <sup>(3)</sup>
13	TDO_SWO	JTAG TDI, SWO	JTDO	TRACESWO <sup>(4)</sup>
14	Not used <sup>(5)</sup>	Not used <sup>(5)</sup>	Not connected <sup>(5)</sup>	Not connected <sup>(5)</sup>
15	NRST	NRST	NRST	NRST
16	Not connected	Not connected	Not connected	Not connected
17	Not connected	Not connected	Not connected	Not connected
18	GND	GND	GND <sup>(3)</sup>	GND <sup>(3)</sup>
19	Not connected	Not connected	Not connected	Not connected
20	GND	GND	GND <sup>(3)</sup>	GND <sup>(3)</sup>

Table 4. JTAG/SWD cable connections on STLINK-V2

Pin no.	ST-LINK/V2 connector (CN3)	ST-LINK/V2 function	Target connection (JTAG)	Target connection (SWD)
1	VAPP	Target VCC	MCU VDD <sup>(1)</sup>	MCU VDD <sup>(1)</sup>
3	TRST	JTAG TRST	NJTRST	GND <sup>(2)</sup>
4	GND	GND	GND <sup>(2)</sup>	GND <sup>(2)</sup>
5	TDI	JTAG TDO	JTDI	GND <sup>(2)</sup>
6	GND	GND	JTMS	GND <sup>(2)</sup>
7	TMS_SWDIO	JTAG TMS, SW IO	JTMS	SWDIO
8	GND	GND	JTMS	GND <sup>(2)</sup>
9	TCK_SWCLK	JTAG TCK, SW CLK	JTCK	SWCLK
10	GND	GND	GND <sup>(3)</sup>	GND <sup>(3)</sup>
11	Not connected	Not connected	Not connected	Not connected
12	GND	GND	GND <sup>(3)</sup>	GND <sup>(3)</sup>
13	TDO_SWO	JTAG TDI, SWO	JTDO	TRACESWO <sup>(4)</sup>
14	GND	GND	GND <sup>(3)</sup>	GND <sup>(3)</sup>
15	NRST	NRST	NRST	NRST
16	GND	GND	GND <sup>(3)</sup>	GND <sup>(3)</sup>
17	Not connected	Not connected	Not connected	Not connected
18	GND	GND	GND <sup>(3)</sup>	GND <sup>(3)</sup>
19	VDD	VDD (3.3 V)	Not connected	Not connected
20	GND	GND	GND <sup>(3)</sup>	GND <sup>(3)</sup>



Title:

Sheet: /STM/PinoutSTM/

Rev:

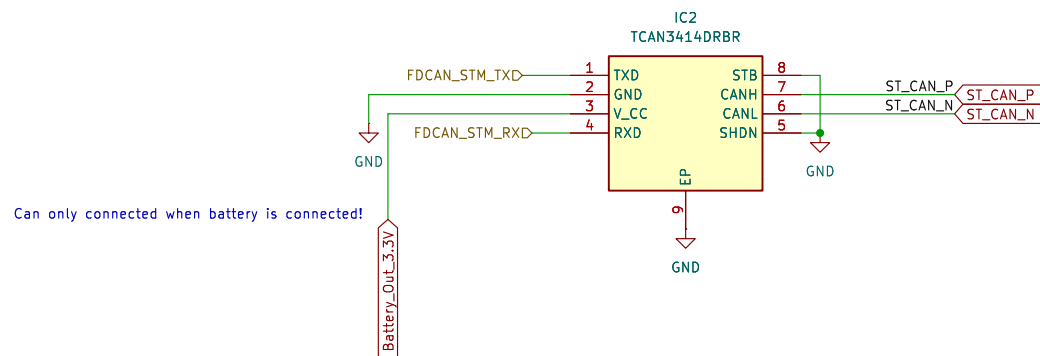
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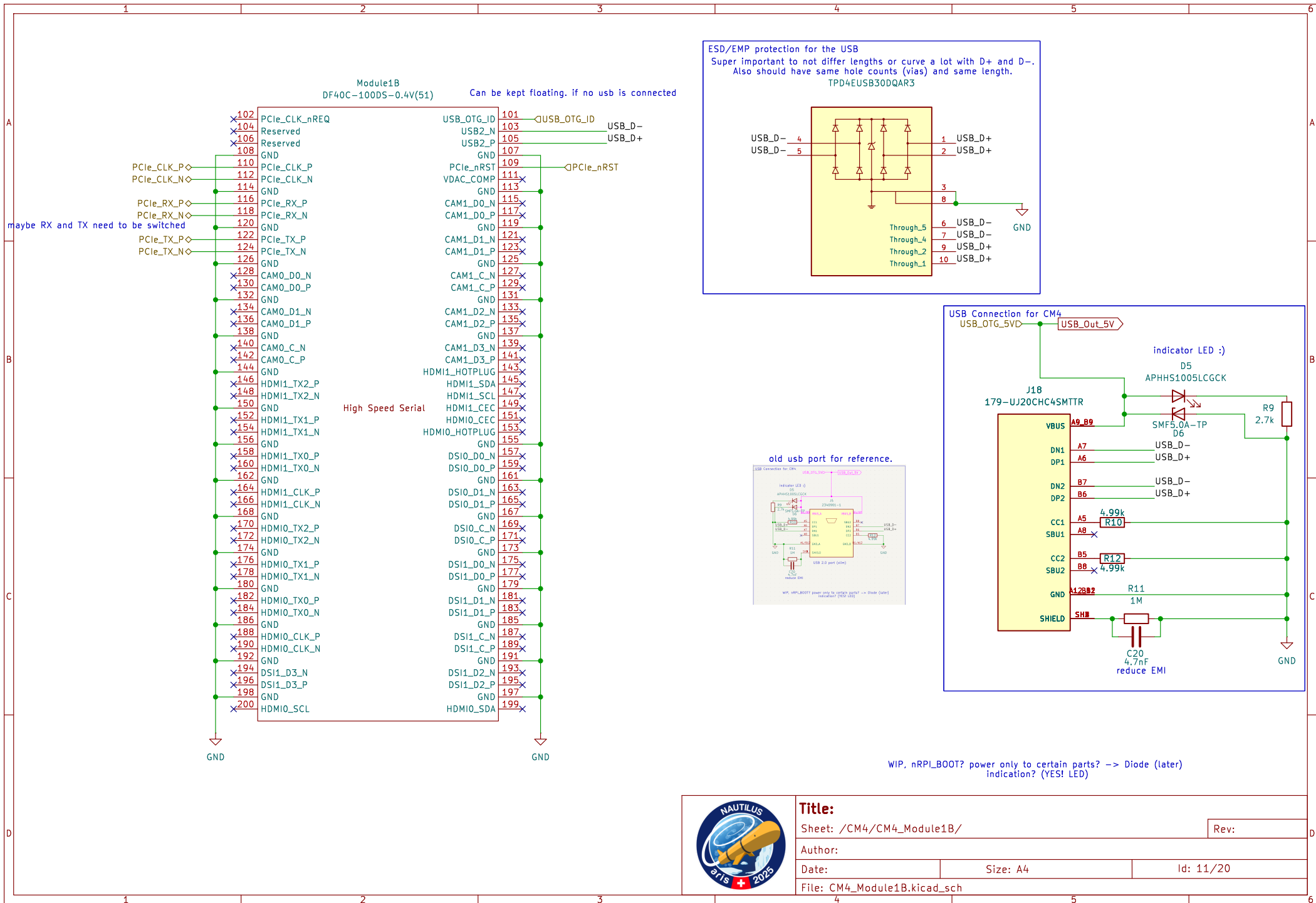
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Author:		
Date:	Size: A4	Id: 7/20
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for questions about wiring etc please consult the datasheet...  
<https://www.ti.com/lit/ds/symlink/tps2120.pdf?ts=1761678178328>

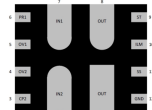
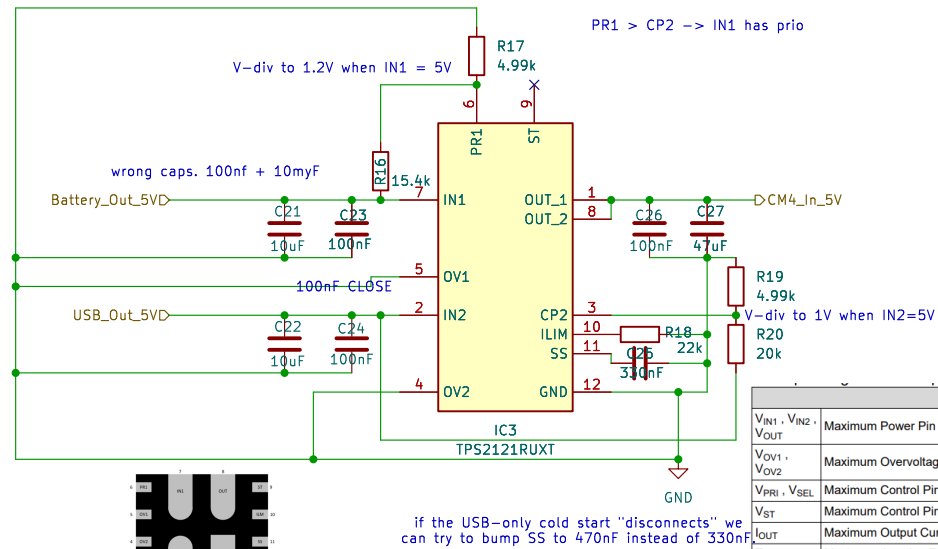


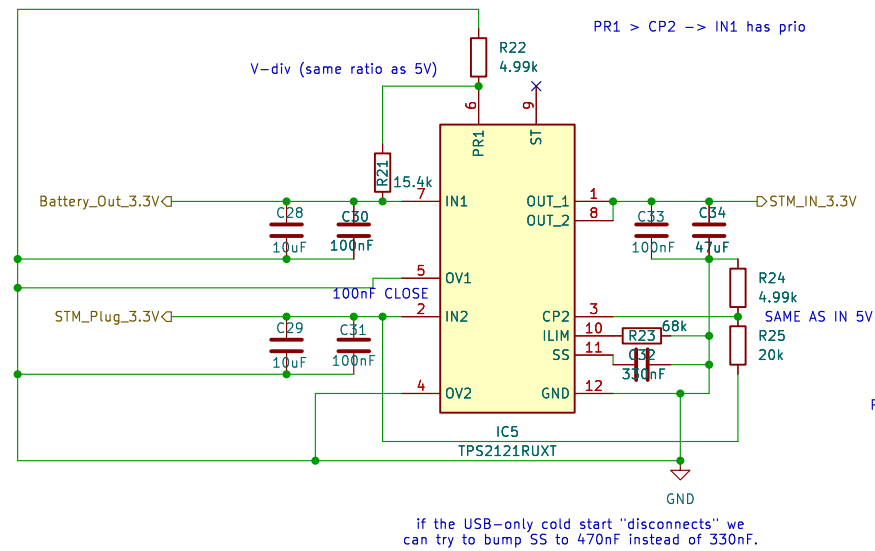
Figure 6-2. TPS2121 (RUX) Package 12-Pin VQFN-HR Bottom View

PIN		TPS2121		IO	DESCRIPTION
NAME	TPS2120	TPS2121	WCSIP		
IN1	B1, B2, C1	7	1	I	Power Input for Source 1
IN2	B3, B4, C4	2	1	I	Power Input for Source 2
OUT	C2, C3, D1, D2, D3, D4	1, 8	1	O	Power Output
ST	E1	9	0	O	Status output indicating which channel is selected. Connect to GND if not required.
ILIM	E2	10	0	O	Output Current Limiting for both channels.
ISL	E3	11	0	O	Adjusts Input Settling Delay Time and Output Soft Start Time
GND	E4	12	—	—	Device Ground
PRI	A1	6	1	I	Enables Priority Operation. Connect to IN1 to set switchover voltage. Connect to GND if not required.
OV1	A2	5	1	I	Active Low Enable Supervisor for IN1 Overvoltage Protection. Connect to GND if not required.
OV2	A3	4	1	I	Active Low Enable Supervisor for IN2 Overvoltage Protection. Connect to GND if not required.
SEL	A4	—	1	I	Active Low Enable for IN1. Allows GPIO to override priority operation and manually select IN2. TPS2120 only.
CP2	—	3	1	I	Enables Comparator Operation and is compared to PRI to set switchover voltage. Connect to GND if not required. TPS2121 only.

		Pins	MIN	MAX	UNIT
V <sub>IN1</sub> , V <sub>IN2</sub> , V <sub>OUT</sub>	Maximum Power Pin Voltage	IN1, IN2, OUT	-0.3	24	V
V <sub>OV1</sub> , V <sub>OV2</sub>	Maximum Overvoltage Pin Voltage	OV1, OV2	-0.3	6	V
V <sub>PRI</sub> , V <sub>SEL</sub>	Maximum Control Pin Voltage	PRI, SEL	-0.3	6	V
V <sub>ST</sub>	Maximum Control Pin Voltage	ST	-0.3	6	V
I <sub>OUT</sub>	Maximum Output Current	OUT	Internally Limited		
T <sub>J, MAX</sub>	Maximum Junction Temperature		Internally Limited		
T <sub>STG</sub>	Storage temperature		-65	150	°C



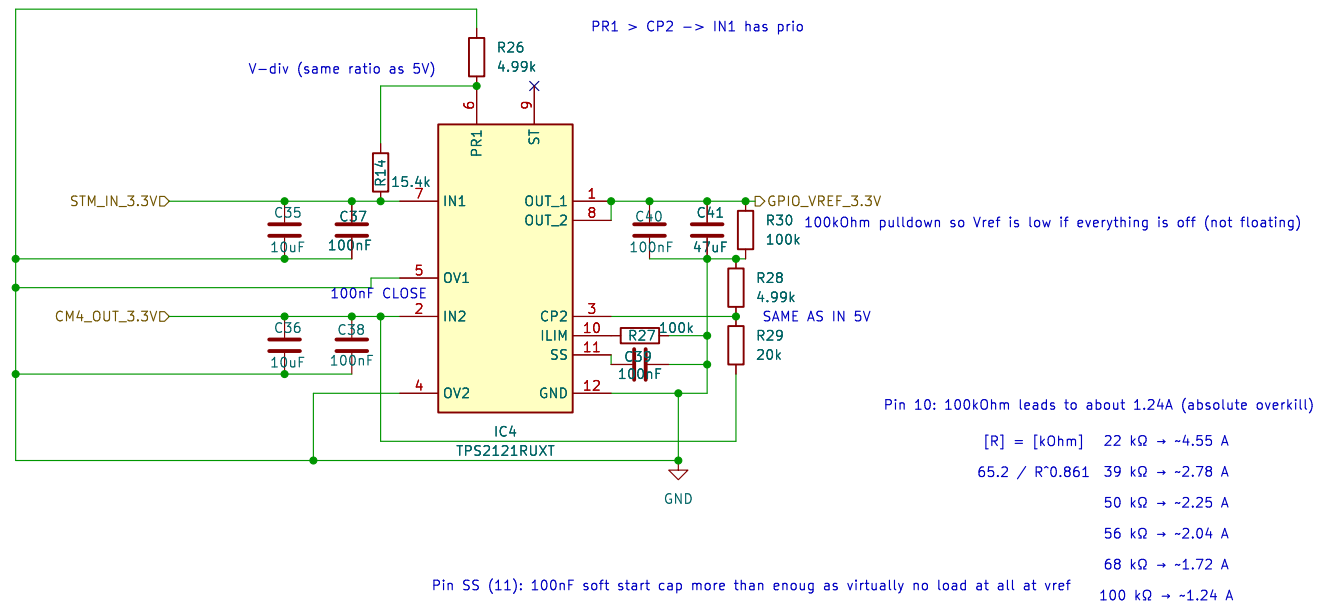
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Author:		
Date:	Size: A4	Id: 15/20
File: 5V_Logic.kicad_sch		



[R] = [kOhm]	22 kΩ	→ -4.55 A
65.2 / R*0.861	39 kΩ	→ -2.78 A
	50 kΩ	→ -2.25 A
	56 kΩ	→ -2.04 A
	68 kΩ	→ -1.72 A
	100 kΩ	→ -1.24 A



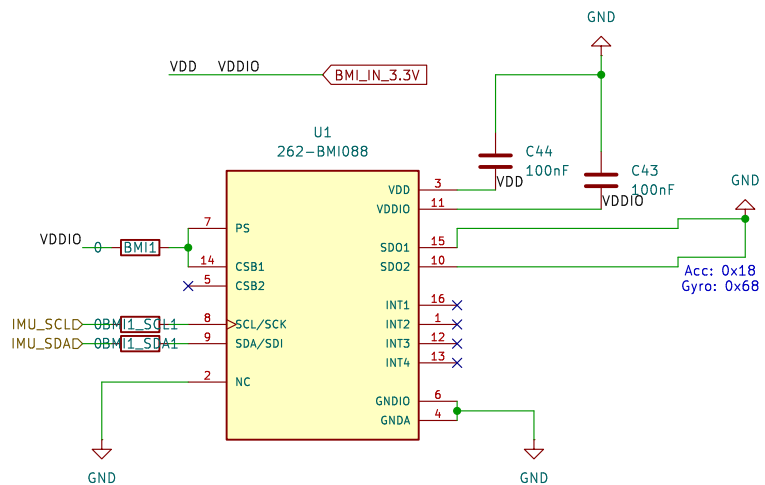
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Date:	Size: A4	Id: 17/20
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PS -> 3.3V IIC  
CSB1 -> 3.3V NOT SPI

PB8 on STM  
PB9 on STM



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Rev:

Author:

Date:

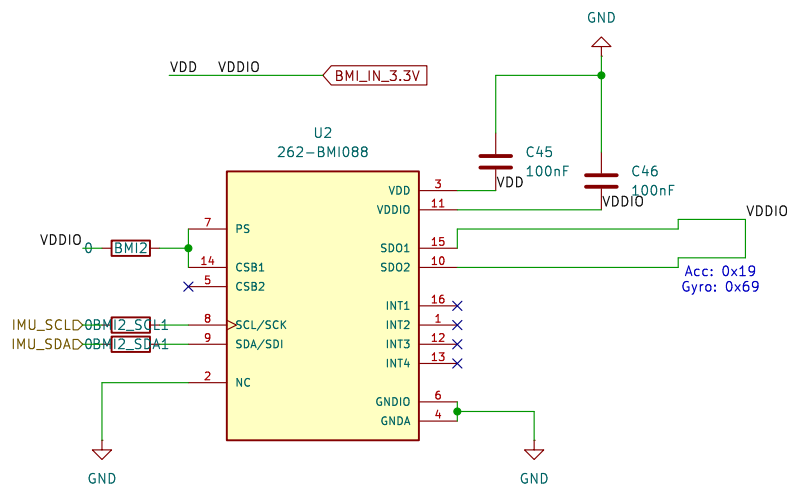
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Id: 19/20

File: IMU1.kicad\_sch

PS -> 3.3V IIC  
CSB1 -> 3.3V NOT SPI

PB8 on STM  
PB9 on STM



Accelerometer  
SD01 pin pulled to GND (0x18)  
SD01 pin pulled to VDDIO: (0x19)

Gyroscope:  
SD02 pin pulled to GND: (0x68)  
SD02 pin pulled to VDDIO: (0x69)



# Title:

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Rev:

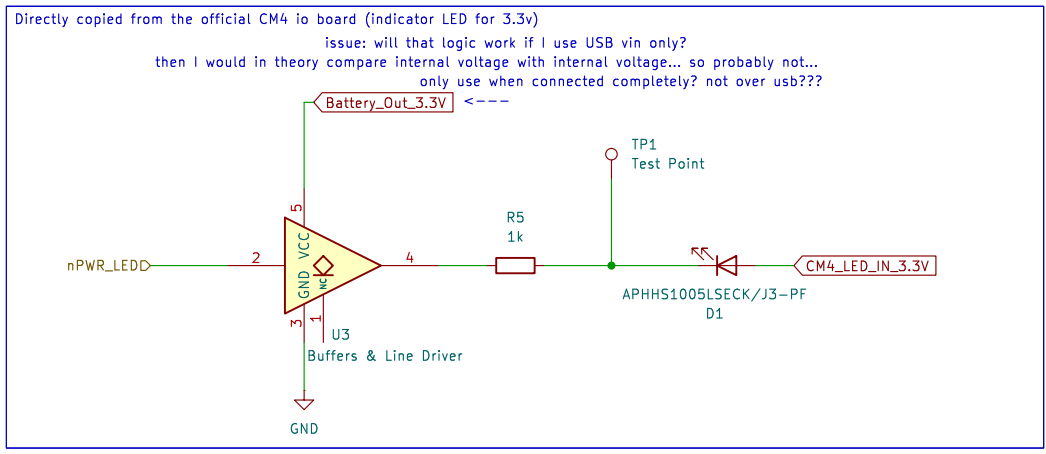
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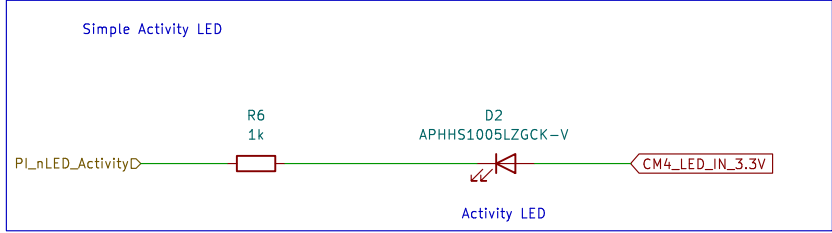
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Rev:

Author:

Date:

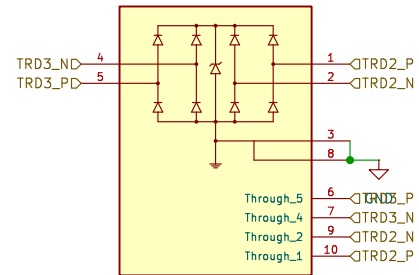
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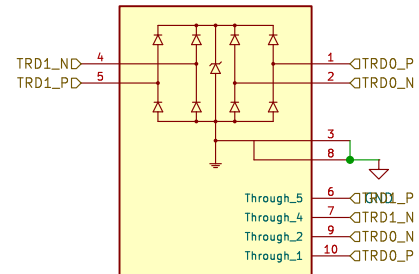
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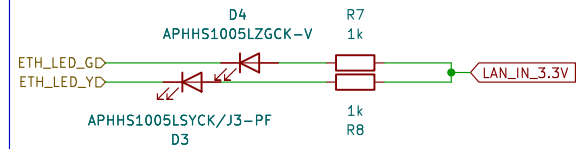
TPD4EUSB30DQAR1



TPD4EUSB30DQAR2



Optimal: Green: 325 Ohm (3.3-2.65)/0.002  
Optimal: Yellow: 725 Ohm (3.3-1.85)/0.002



## Title:

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Rev:

Author:

Date:

Size: A4

Id: 10/20

File: CM4\_Ethernet.kicad\_sch