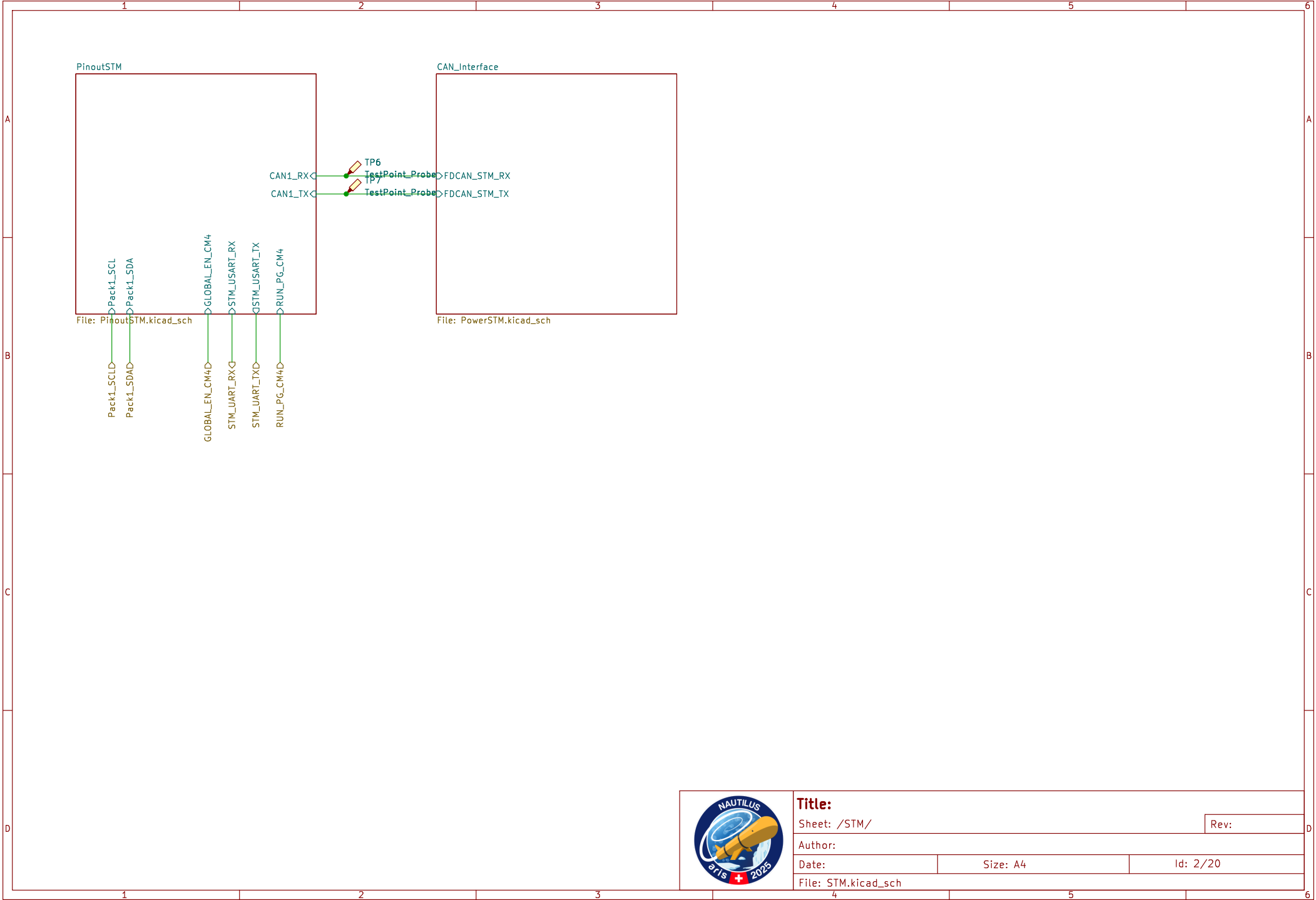
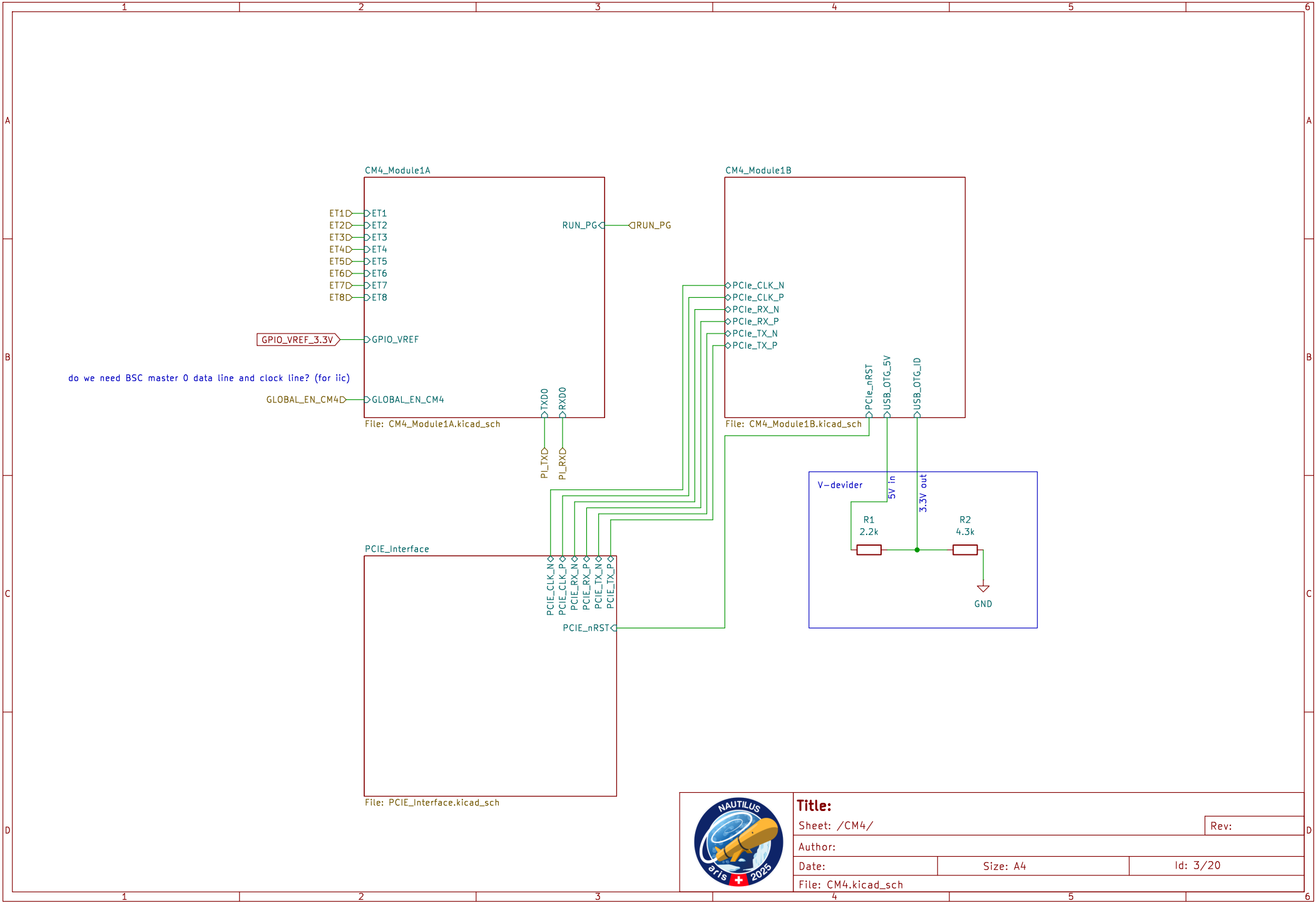
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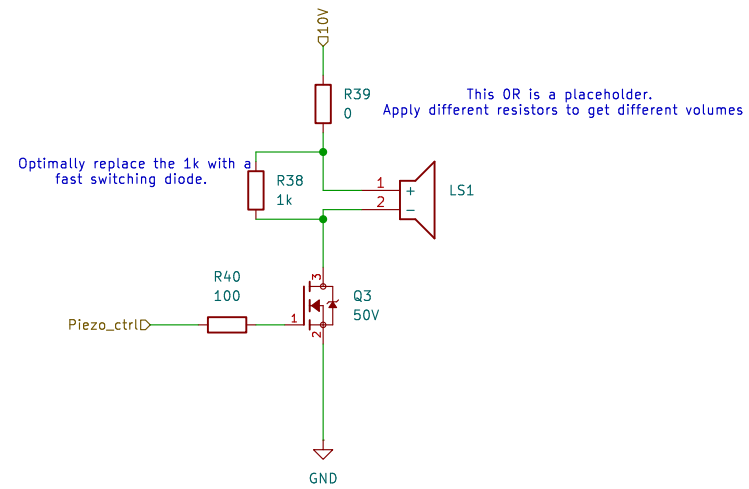


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Not in the PCB yet as we dont know if we actually need it.



Title:

Sheet: /Piezzo/

Rev:

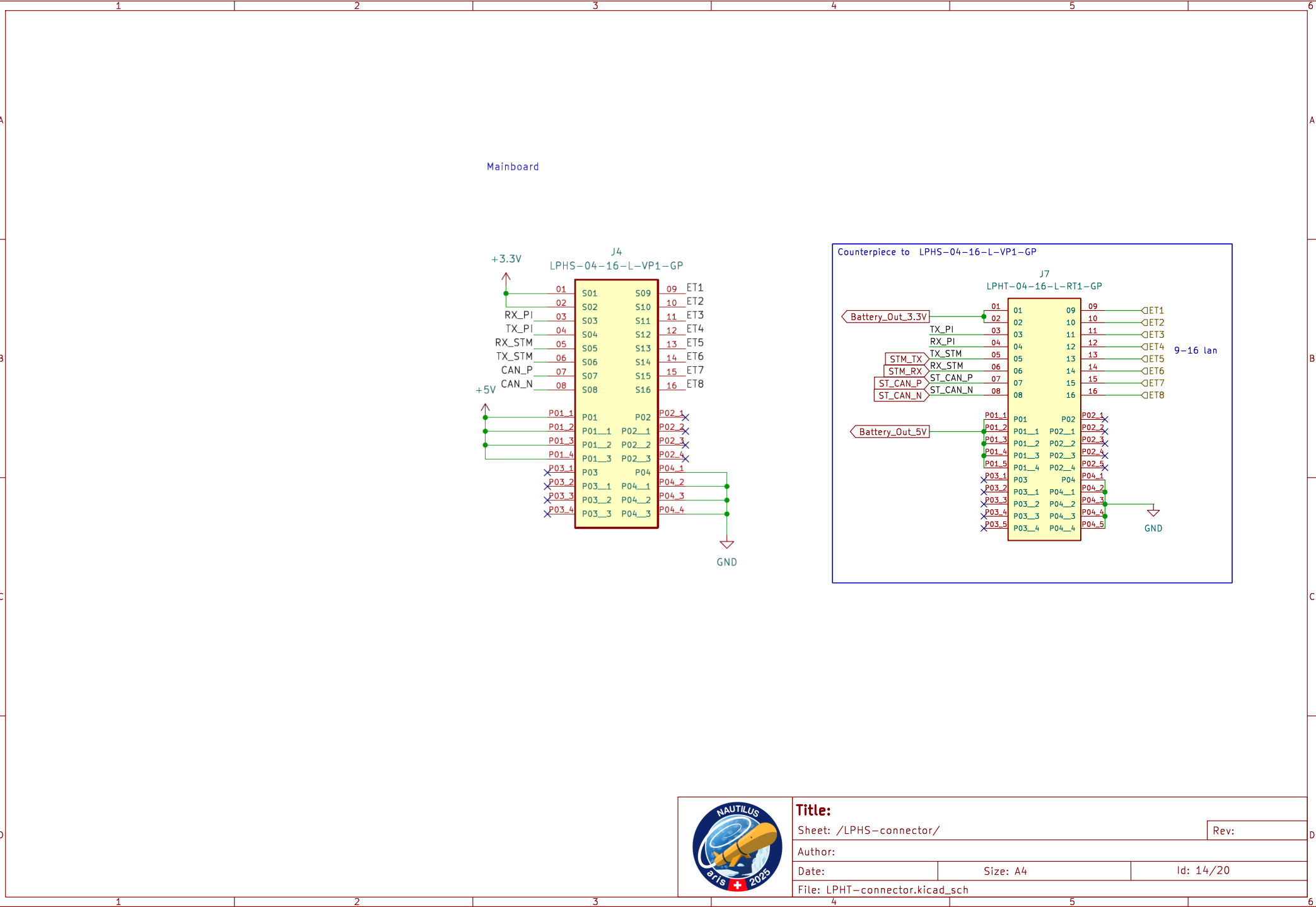
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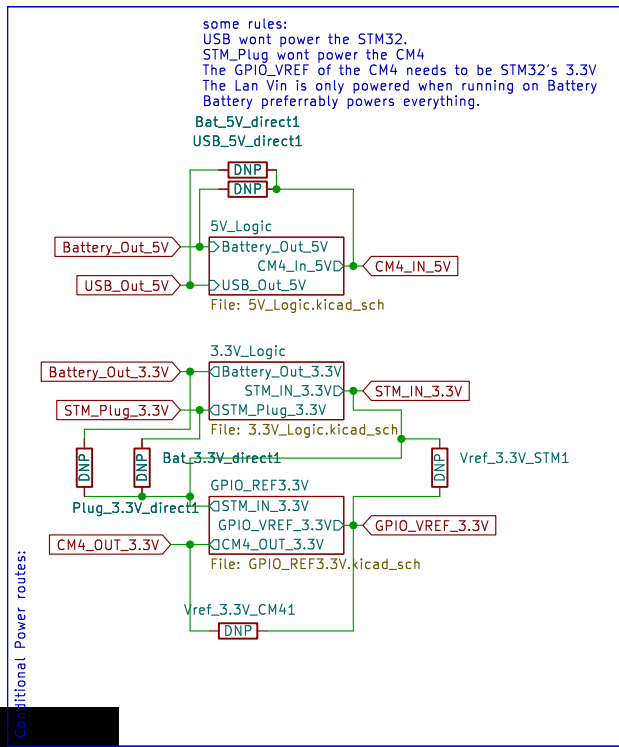
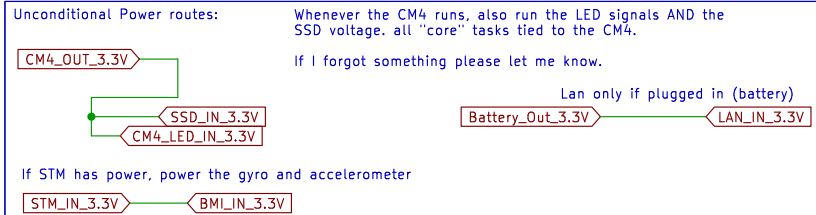
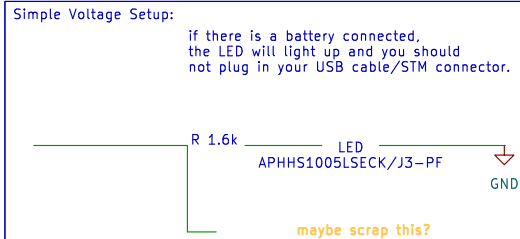
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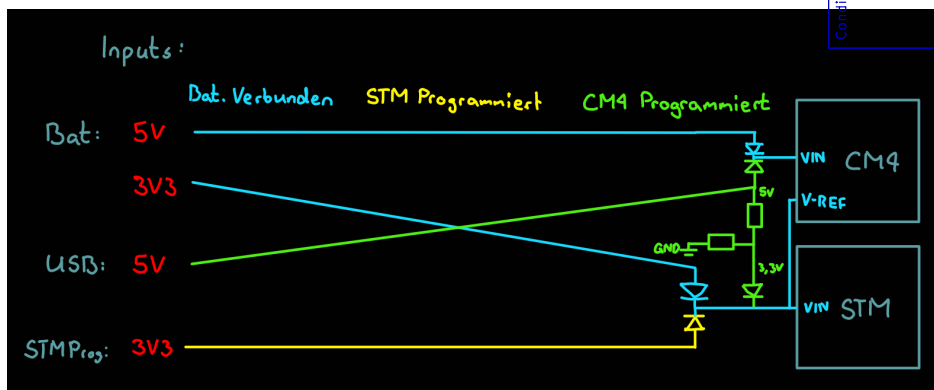
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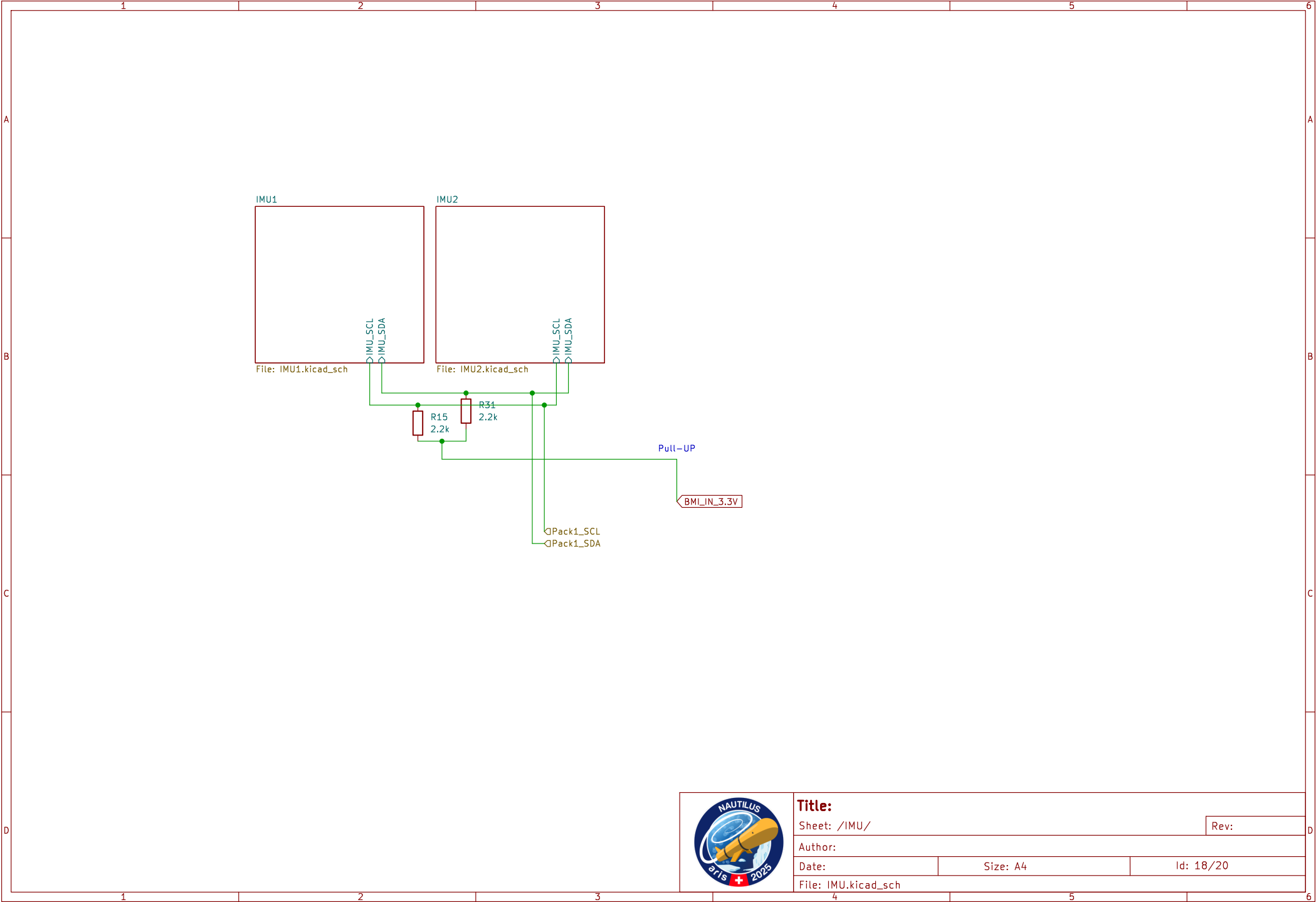




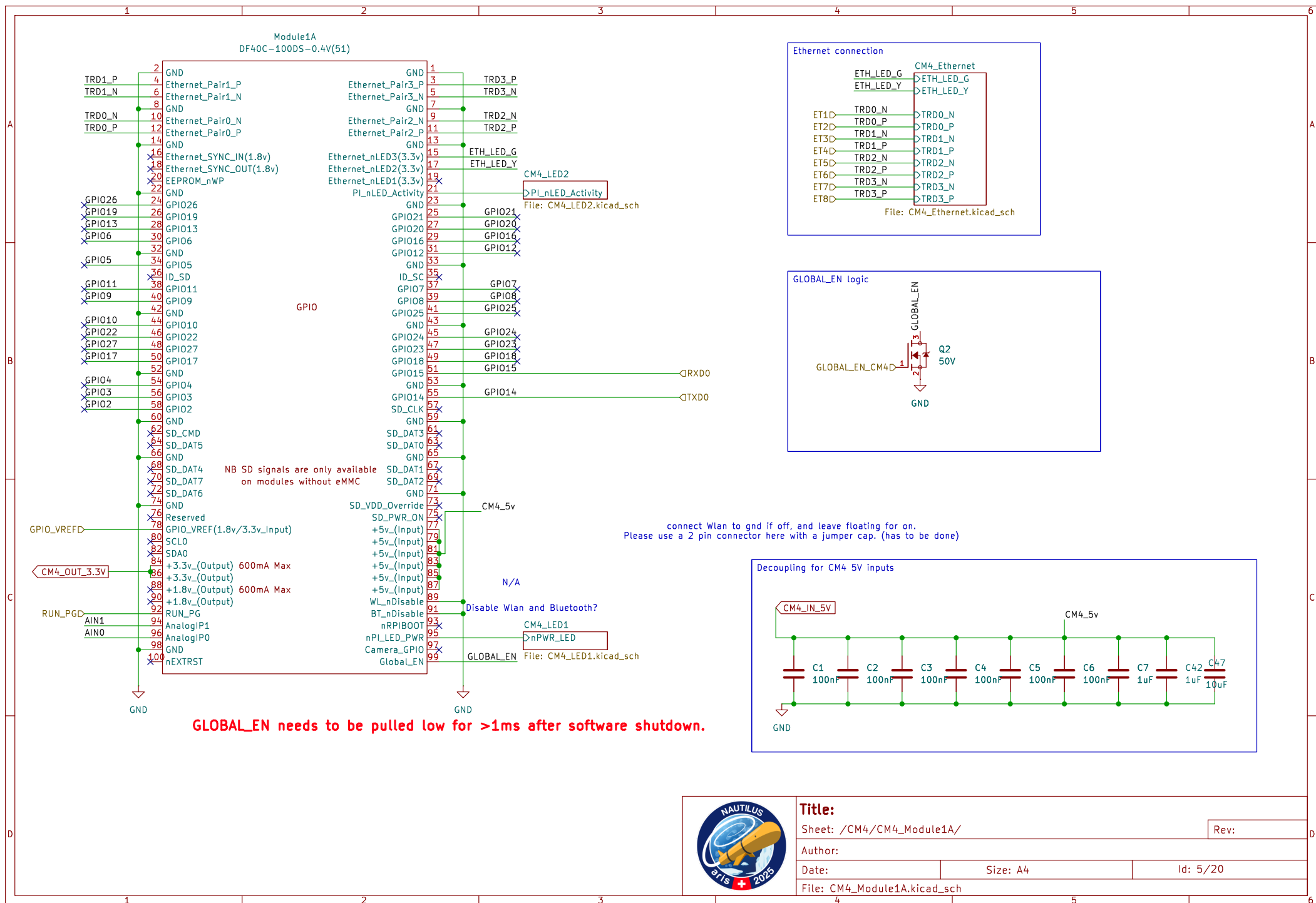
Wont work... diodes are not perfect...



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Date:	Size: A4	Id: 14/20
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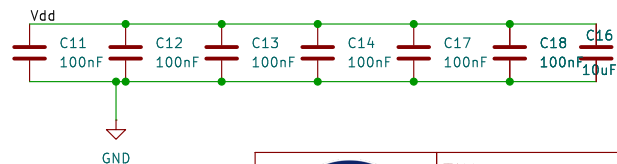
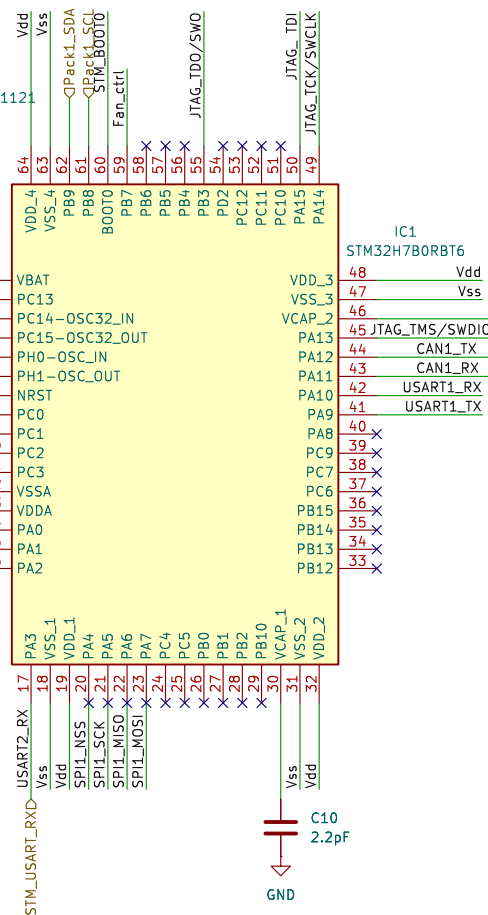
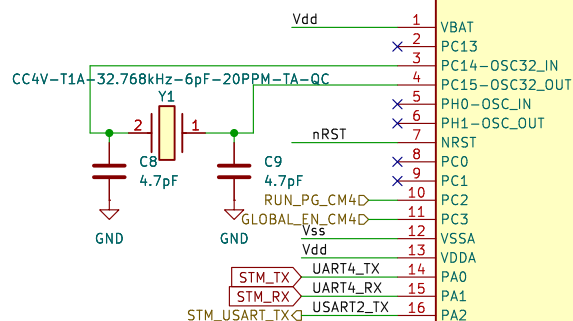
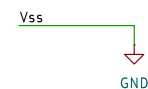
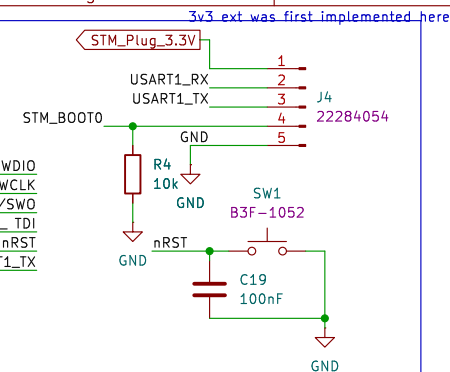
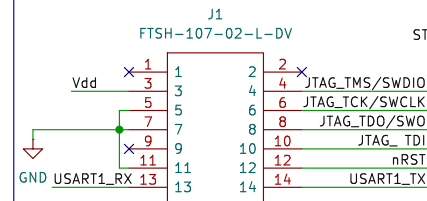
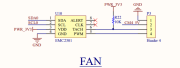


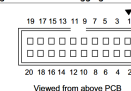
Table 5. JTAG/SWD cable connections on STLINK-V2-ISOL

Pin no.	STLINK/V2 connector (CN3)	STLINK/V2 function	Target connection (JTAG)	Target connection (SWD)
1	VAPP	Target VCC	MCU VDD ⁽¹⁾	MCU VDD ⁽¹⁾
3	TRST	JTAG TRST	NJTRST	GND ⁽²⁾
4	Not connected	Not connected	Not connected	Not connected
5	TDI	JTAG TDO	JTDO	GND ⁽²⁾
6	Not connected	Not connected	Not connected	Not connected
7	TMS_SWDIO	JTAG TMS, SW IO	JTMS	SWDIO
8	Not connected	Not connected	Not connected	Not connected
9	TCK_SWCLK	JTAG TCK, SW CLK	JTCK	SWCLK
10	Not used ⁽¹⁾	Not used ⁽²⁾	Not connected ⁽³⁾	Not connected ⁽³⁾
11	Not connected	Not connected	Not connected	Not connected
12	GND	GND	GND ⁽³⁾	GND ⁽³⁾
13	TDO_SWO	JTAG TDI, SWO	JTDO	TRACESWO ⁽⁴⁾
14	Not used ⁽¹⁾	Not used ⁽²⁾	Not connected ⁽³⁾	Not connected ⁽³⁾
15	NRST	NRST	NRST	NRST
16	Not connected	Not connected	Not connected	Not connected
17	Not connected	Not connected	Not connected	Not connected
18	GND	GND	GND ⁽³⁾	GND ⁽³⁾
19	Not connected	Not connected	Not connected	Not connected
20	GND	GND	GND ⁽³⁾	GND ⁽³⁾

Table 4. JTAG/SWD cable connections on STLINK-V2

Pin no.	ST-LINKV2 connector (CN3)	ST-LINKV2 function	Target connection (JTAG)	Target connection (SWD)
1	VAPP	Target VCC	MCU VDD ⁽¹⁾	MCU VDD ⁽¹⁾
2	TRST	JTAG TRST	NJTRST	GND ⁽²⁾
3	GND	GND	GND ⁽³⁾	GND ⁽²⁾
5	TDI	JTAG TMS	JTMS	GND ⁽²⁾
7	TMS_SWDIO	JTAG TMS, SW IO	GND ⁽³⁾	SWDIO
8	GND	GND	GND ⁽³⁾	GND ⁽²⁾
9	TCK_SWCLK	JTAG TCK, SW CLK	JTCK	SWCLK
10	GND	GND	GND ⁽³⁾	GND ⁽²⁾
11	Not connected	Not connected	Not connected	Not connected
12	GND	GND	GND ⁽³⁾	GND ⁽²⁾
13	TD0_SWO	JTAG TDI, SWO	JTDO	TRACESWO ⁽⁴⁾
14	GND	GND	GND ⁽³⁾	GND ⁽²⁾
15	NRST	NRST	NRST	NRST
16	GND	GND	GND ⁽³⁾	GND ⁽²⁾
17	Not connected	Not connected	Not connected	Not connected
18	GND	GND	GND ⁽³⁾	GND ⁽²⁾
19	VDD	VDD (3.3 V)	Not connected	Not connected
20	GND	GND	GND ⁽³⁾	GND ⁽²⁾

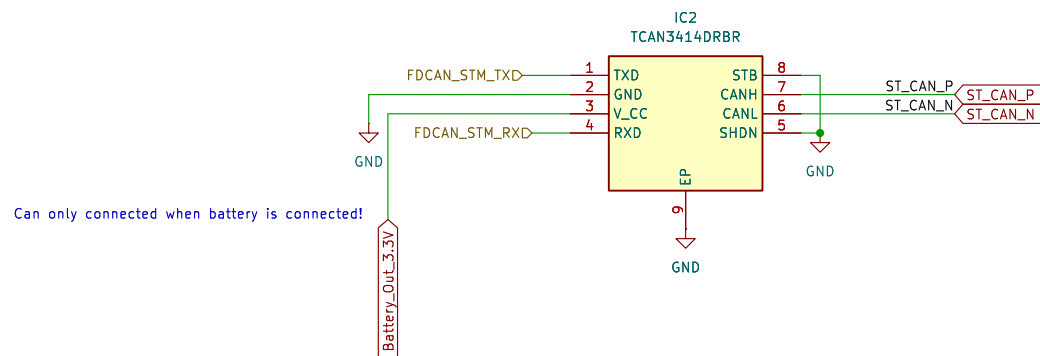
Figure 10. JTAG debugging flat ribbon layout



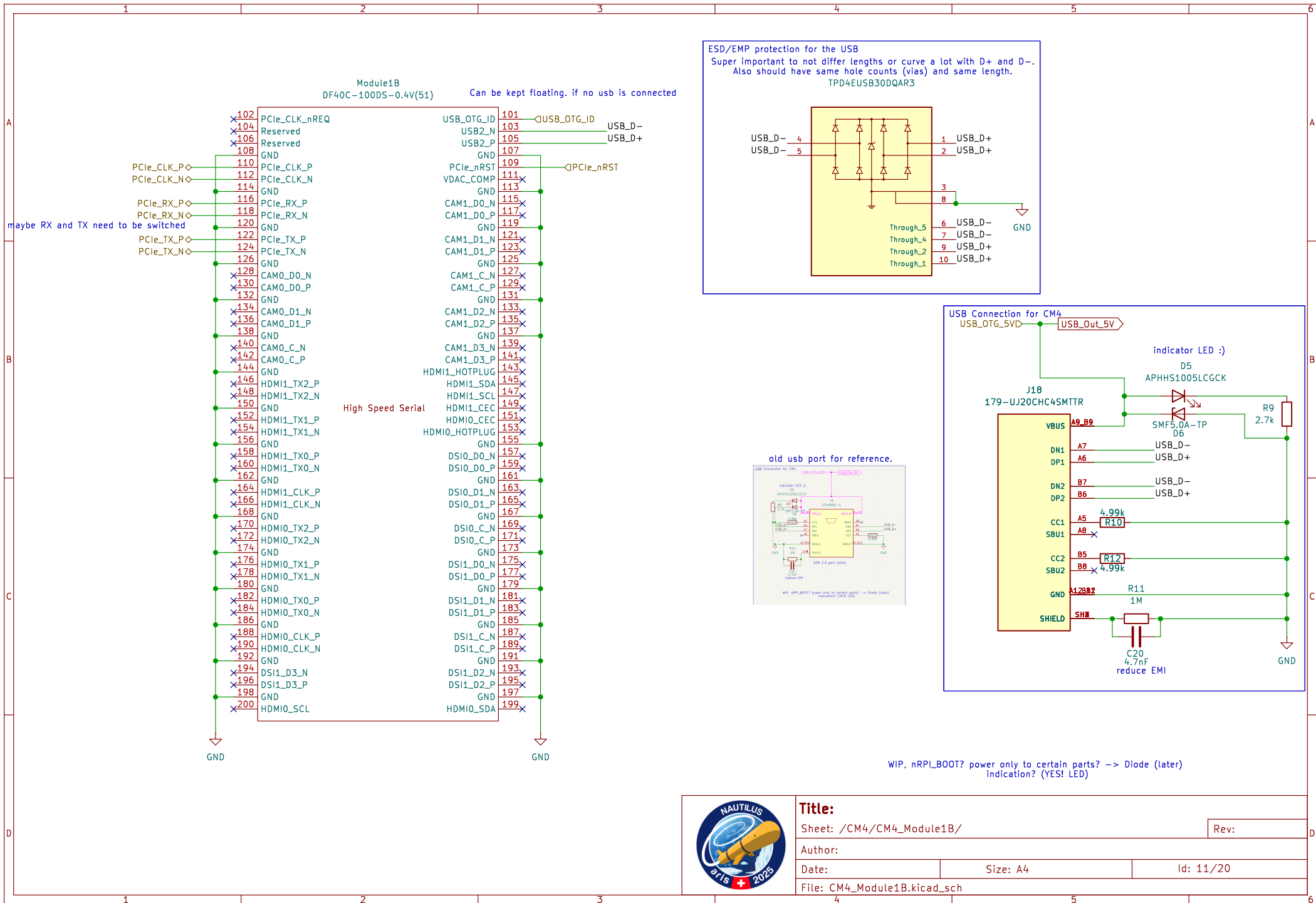
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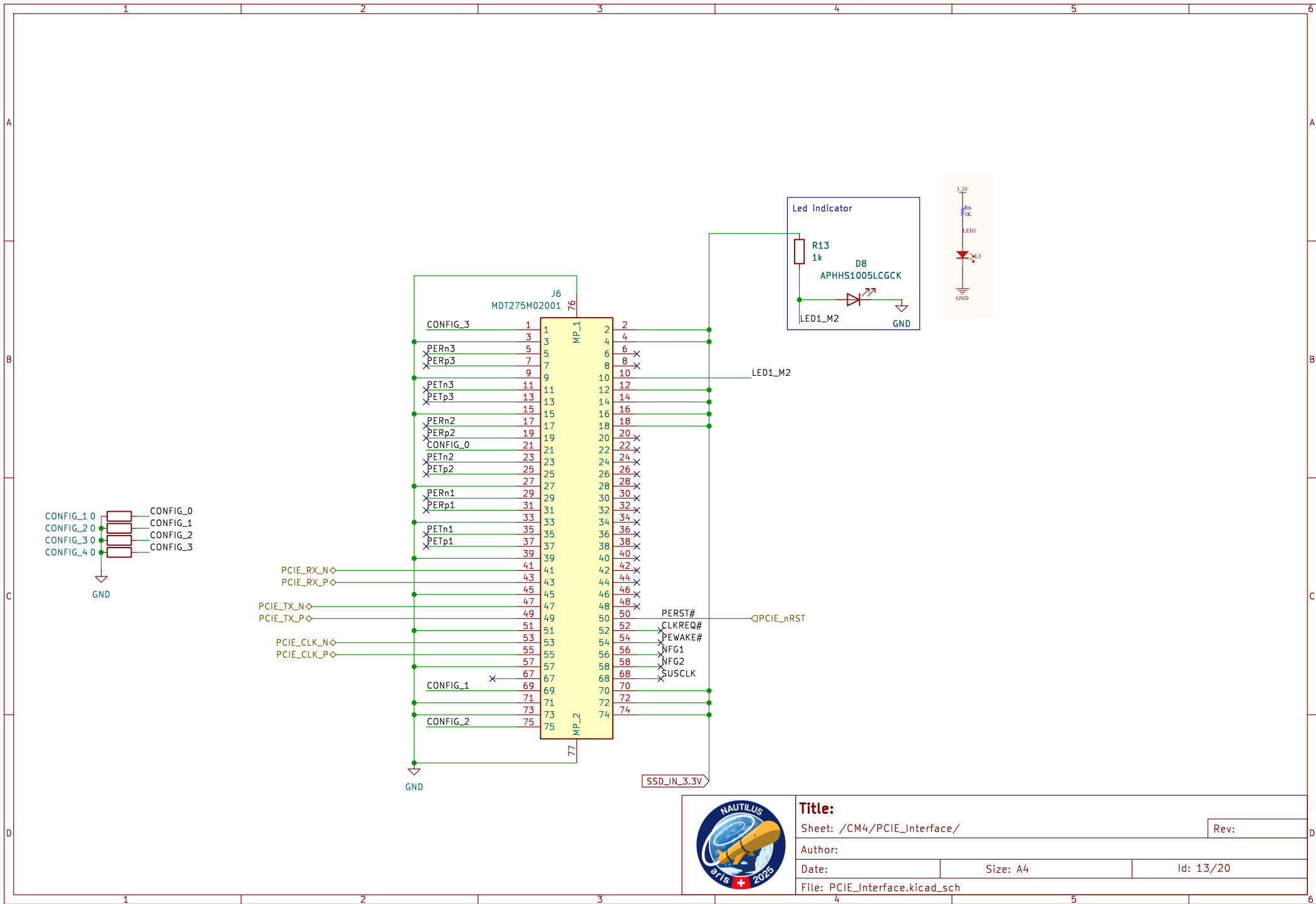
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Title:		
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Author:		
Date:	Size: A4	Id: 13/20
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for questions about wiring etc please consult the datasheet...
<https://www.ti.com/lit/ds/symlink/tps2120.pdf?ts=1761678178328>

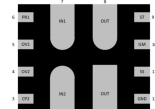
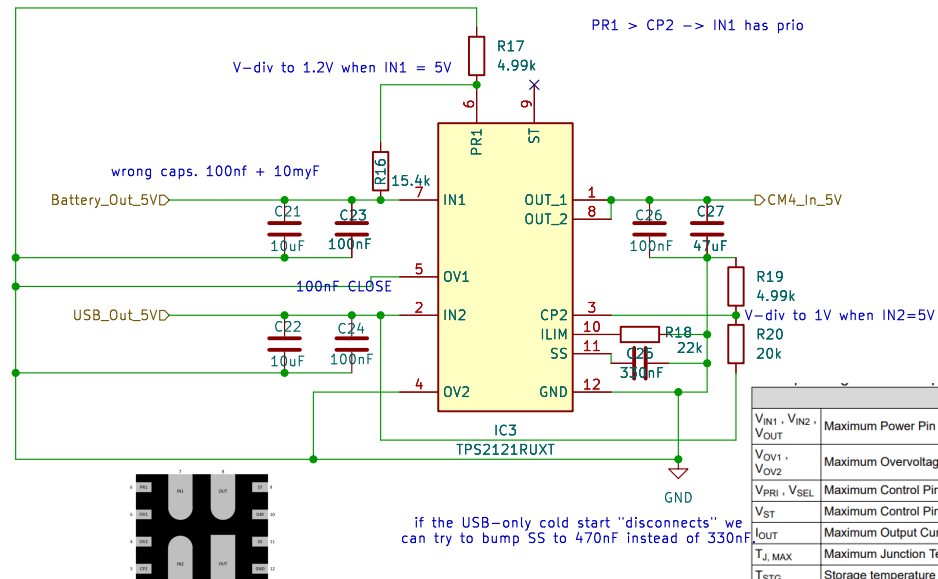


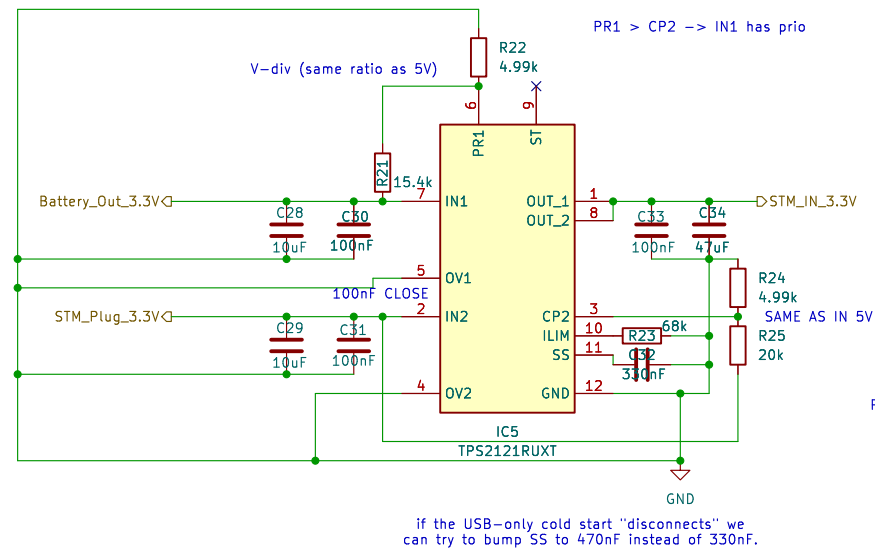
Figure 6-2. TPS2121 (RUX) Package 12-Pin VQFN-HR Bottom View

NAME	PIN		IO	DESCRIPTION
	TPS2120	TPS2121		
IN1	B1, B2, C1	7	I	Power Input for Source 1
IN2	B3, B4, C4	2	I	Power Input for Source 2
OUT	C2, C3, D1, D2, D3, D4	1, 8	O	Power Output
ST	E1	9	O	Status output indicating which channel is selected. Connect to GND if not required.
ILIM	E2	10	O	Output Current Limiting for both channels.
ISL	E3	11	O	Adjusts Input Settling Delay Time and Output Soft Start Time
GND	E4	12	—	Device Ground
PRI	A1	6	I	Enables Priority Operation. Connect to IN1 to set switchover voltage. Connect to GND if not required.
OV1	A2	5	I	Active Low Enable Supervisor for IN1 Overvoltage Protection. Connect to GND if not required.
OV2	A3	4	I	Active Low Enable Supervisor for IN2 Overvoltage Protection. Connect to GND if not required.
SEL	A4	—	I	Active Low Enable for IN1. Allows GPIO to override priority operation and manually select IN2. TPS2120 only.
CP2	—	3	I	Enables Comparator Operation and is compared to PRI to set switchover voltage. Connect to GND if not required. TPS2121 only.

		Pins	MIN	MAX	UNIT
V _{IN1} , V _{IN2} , V _{OUT}	Maximum Power Pin Voltage	IN1, IN2, OUT	-0.3	24	V
V _{OV1} , V _{OV2}	Maximum Overvoltage Pin Voltage	OV1, OV2	-0.3	6	V
V _{PRI} , V _{SEL}	Maximum Control Pin Voltage	PRI, SEL	-0.3	6	V
V _{ST}	Maximum Control Pin Voltage	ST	-0.3	6	V
I _{OUT}	Maximum Output Current	OUT	Internally Limited		
T _{J, MAX}	Maximum Junction Temperature		Internally Limited		
T _{STG}	Storage temperature		-65	150	°C



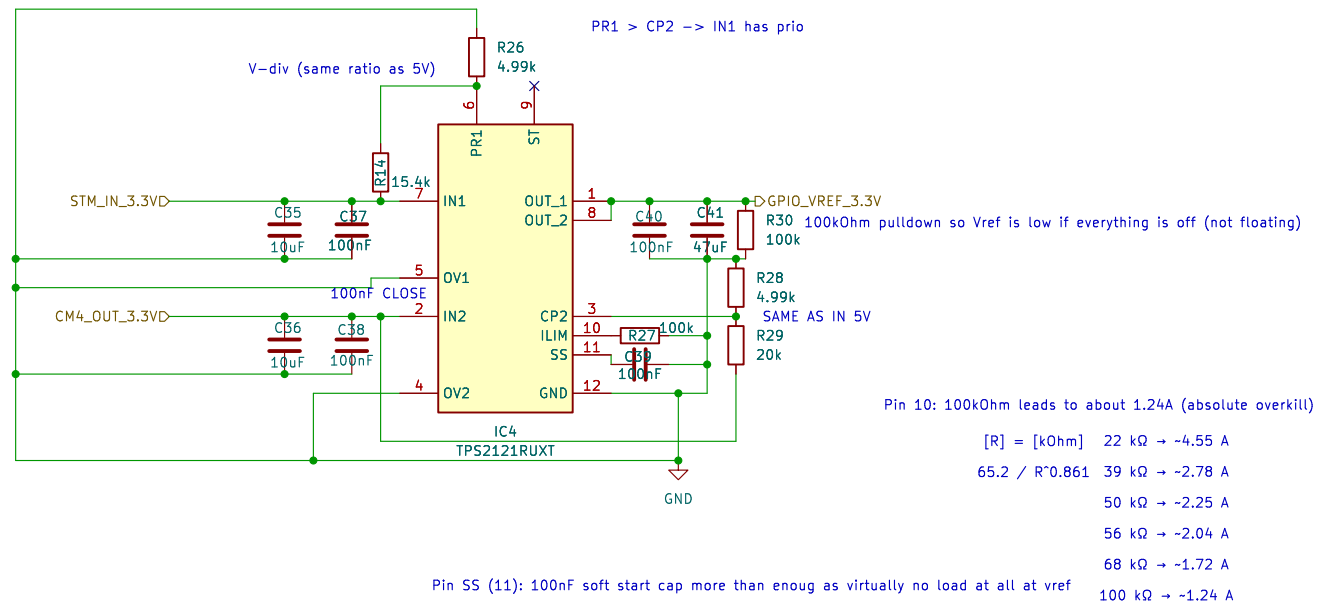
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Date:	Size: A4	Id: 15/20
File: 5V_Logic.kicad_sch		



[R] = [kOhm]	22 kΩ	→ -4.55 A
65.2 / R*0.861	39 kΩ	→ -2.78 A
	50 kΩ	→ -2.25 A
	56 kΩ	→ -2.04 A
	68 kΩ	→ -1.72 A
	100 kΩ	→ -1.24 A



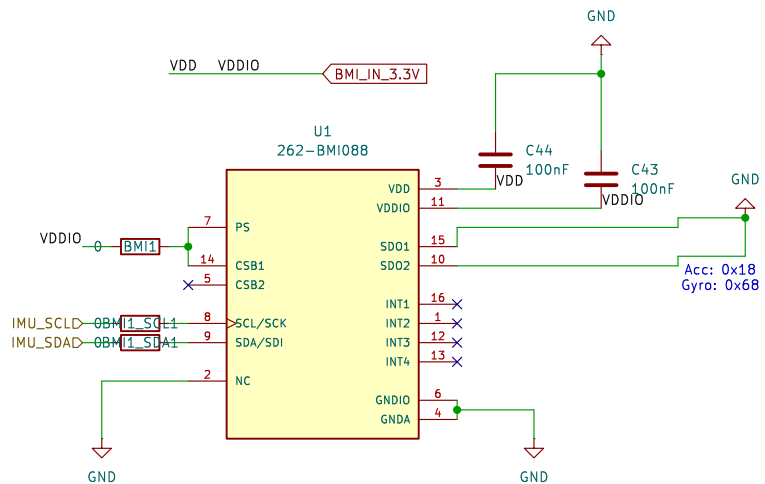
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Title:		
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Author:		
Date:	Size: A4	Id: 17/20
File: GPIO_REF3.3V.kicad_sch		

PS -> 3.3V IIC
CSB1 -> 3.3V NOT SPI

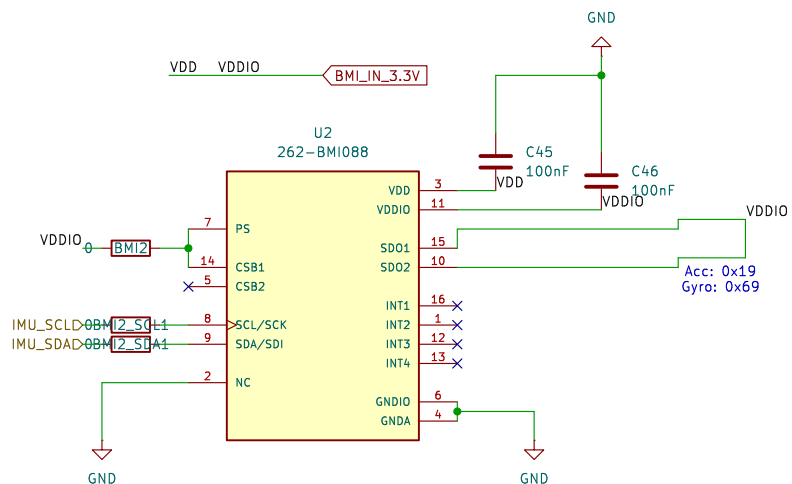
PB8 on STM
PB9 on STM



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PS -> 3.3V IIC
CSB1 -> 3.3V NOT SPI

PB8 on STM
PB9 on STM

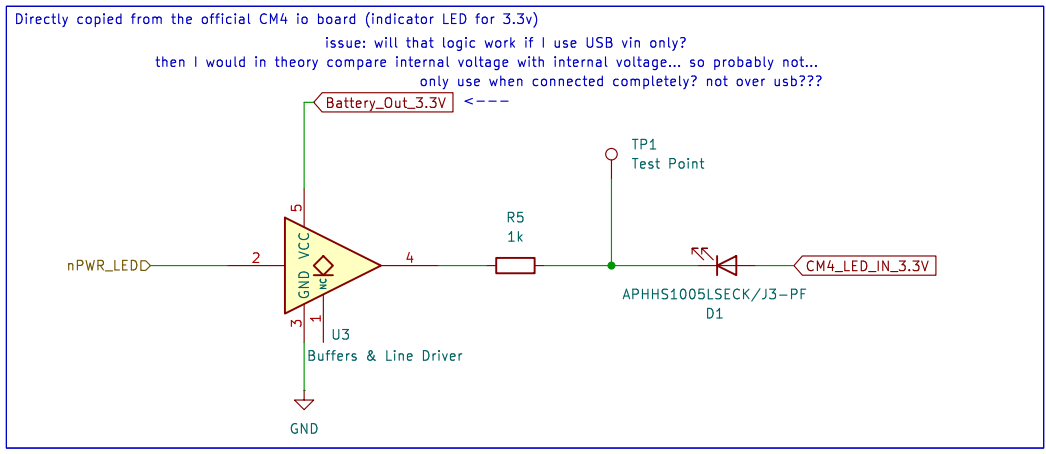


Accelerometer
SD01 pin pulled to GND (0x18)
SD01 pin pulled to VDDIO: (0x19)

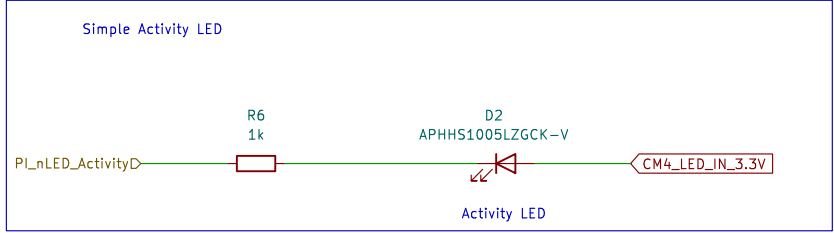
Gyroscope:
SD02 pin pulled to GND: (0x68)
SD02 pin pulled to VDDIO: (0x69)



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Rev:

Author:

Date:

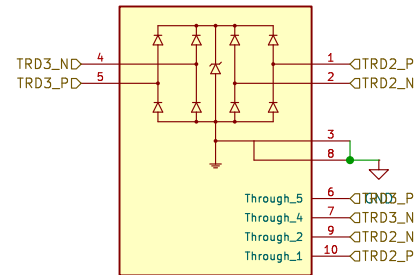
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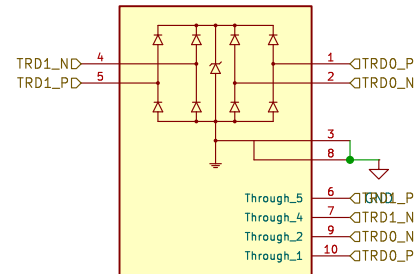
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POE Protection

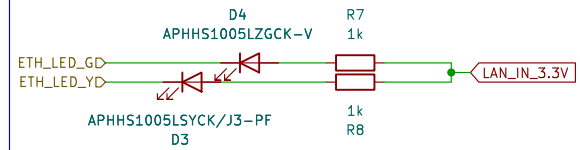
TPD4EUSB30DQAR1



TPD4EUSB30DQAR2



Optimal: Green: 325 Ohm (3.3-2.65)/0.002
Optimal: Yellow: 725 Ohm (3.3-1.85)/0.002



Title:

Sheet: /CM4/CM4_Module1A/CM4_Ethernet/

Rev:

Author:

Date:

Size: A4

Id: 10/20

File: CM4_Ethernet.kicad_sch