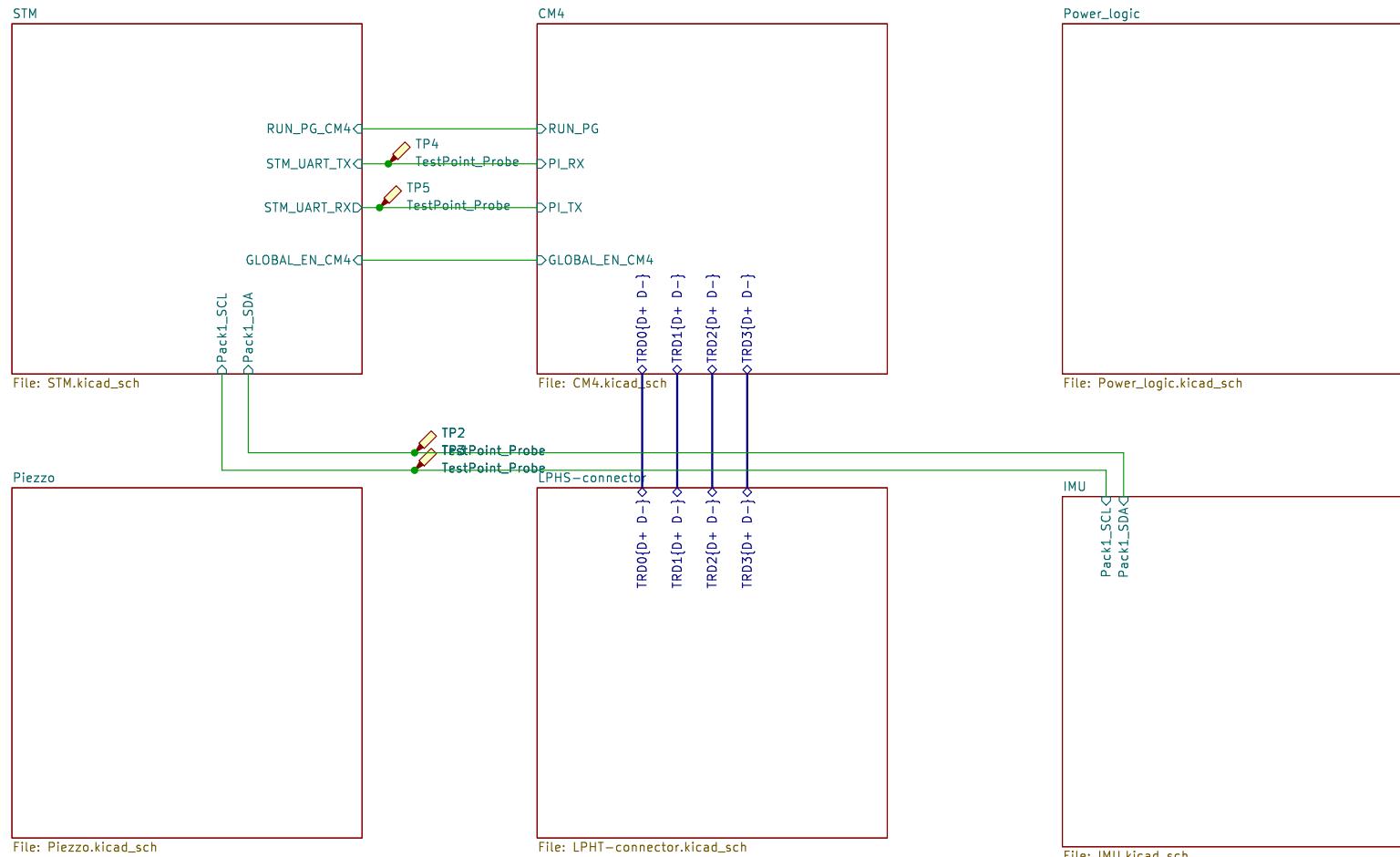


1 2 3 4 5 6



We should consider that we NEVER want the CM4 to power the unpowered STM over the TX pin. Found a neat part for that:

<https://www.mouser.ch/ProductDetail/Texas-Instruments/SN74LVC1G126DBVR?qs=pajglaoyDUI3T2WgNNfd3w%3D%3D>

connections:

Pin 5: VCC → CM4_3V3

Pin 2: A → CM4 TX (PLTX)

Pin 4: Y → STM_UART_RX

Pin 1: OE → STM_IN_3.3V

Pin 3: GND

0.1uF decoupling cap VCC-GND



Title:

Sheet: /

Rev: /

Author: /

Date: /

Size: A4

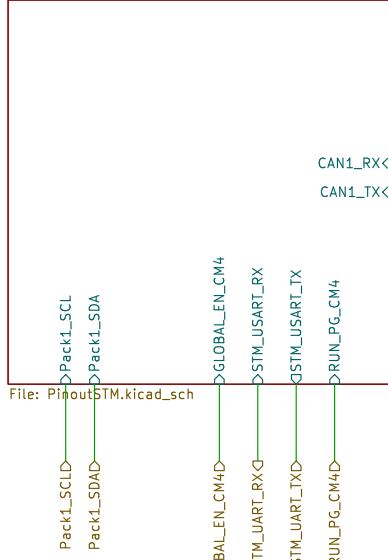
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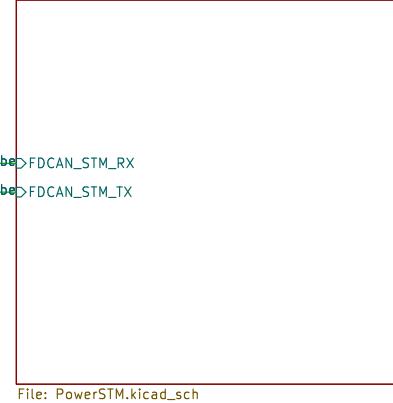
1 2 3 4 5 6

220 Ohm series at Y (to STM). (current limiting)

PinoutSTM



CAN_Interface



A

A

B

B

C

C

D

D

**Title:**

Sheet: /STM/

Rev:

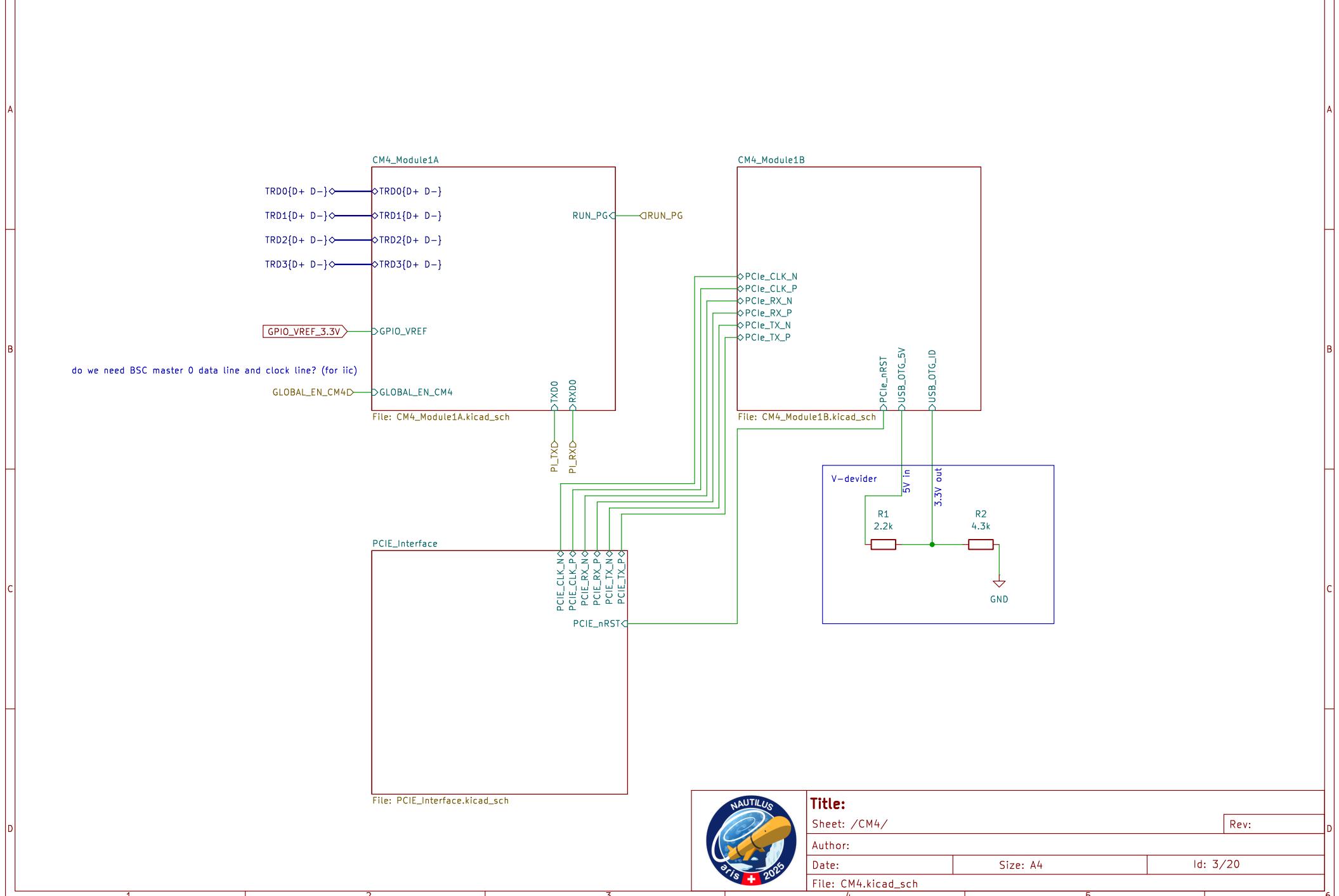
Author:

Date:

Size: A4

Id: 2/20

File: STM.kicad_sch



A

A

B

B

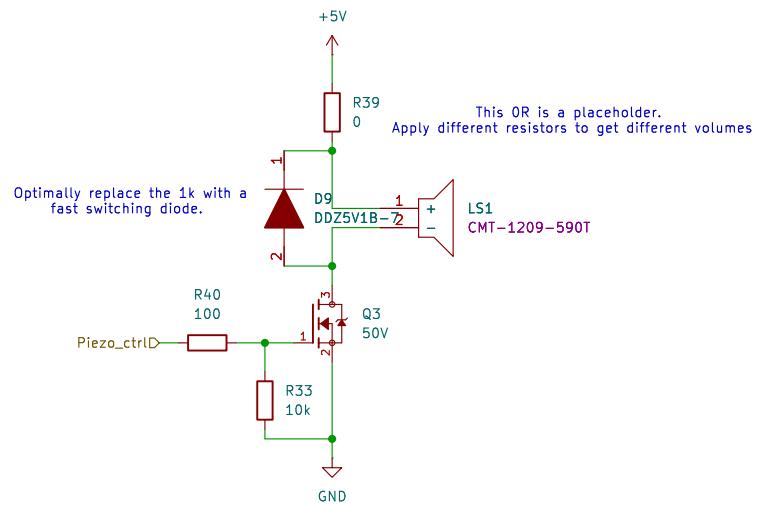
C

C

D

D

Not in the PCB yet as we dont know if we actually need it.


Title:

Sheet: /Piezzo/

Rev:

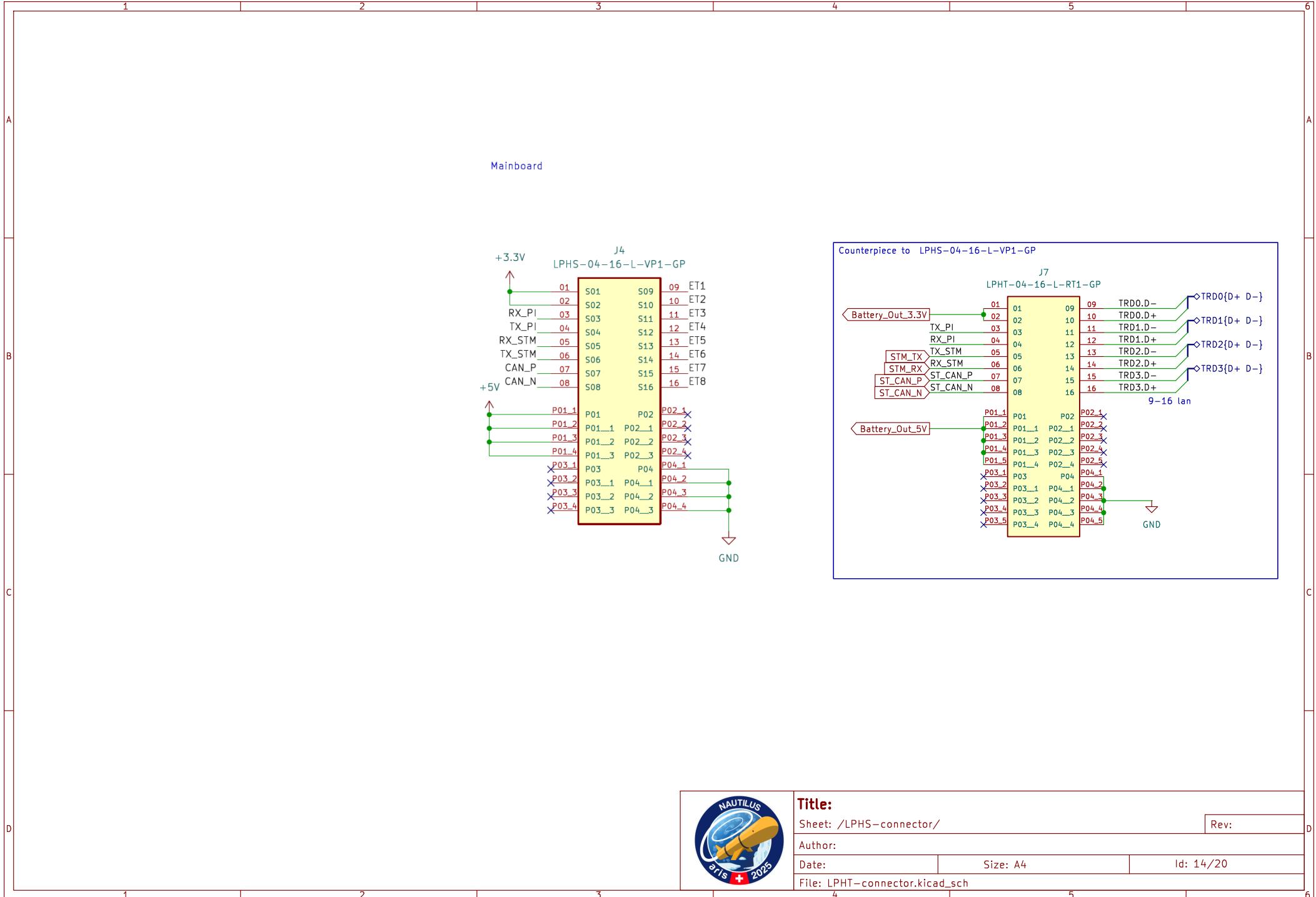
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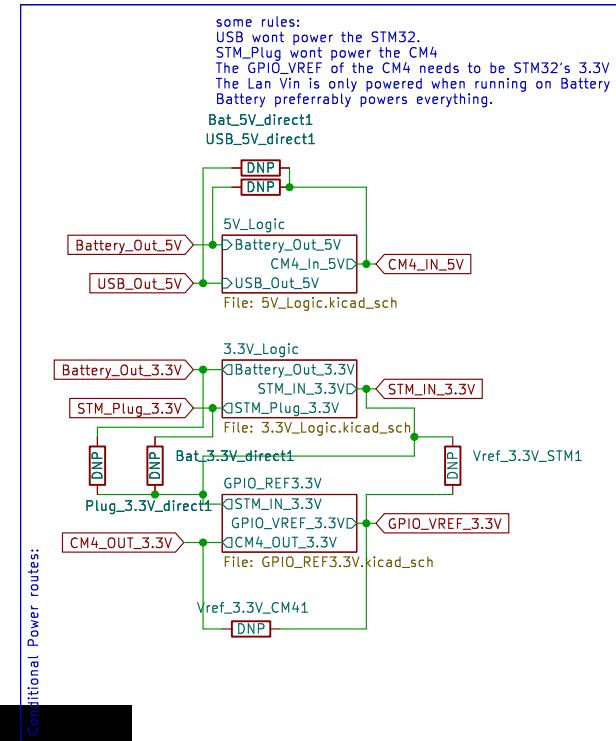
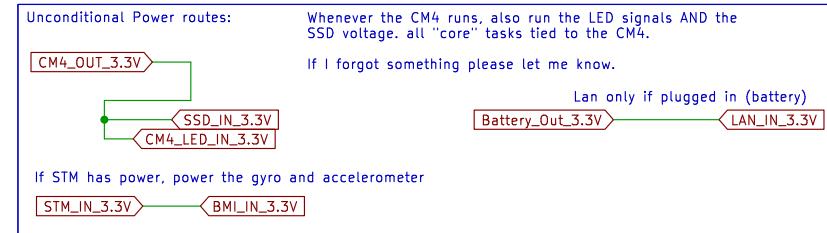
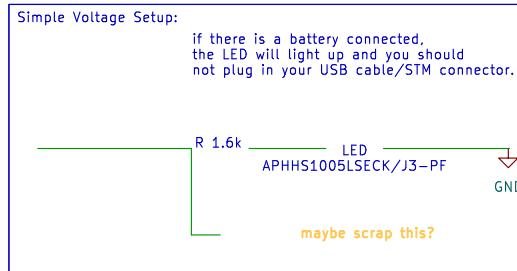
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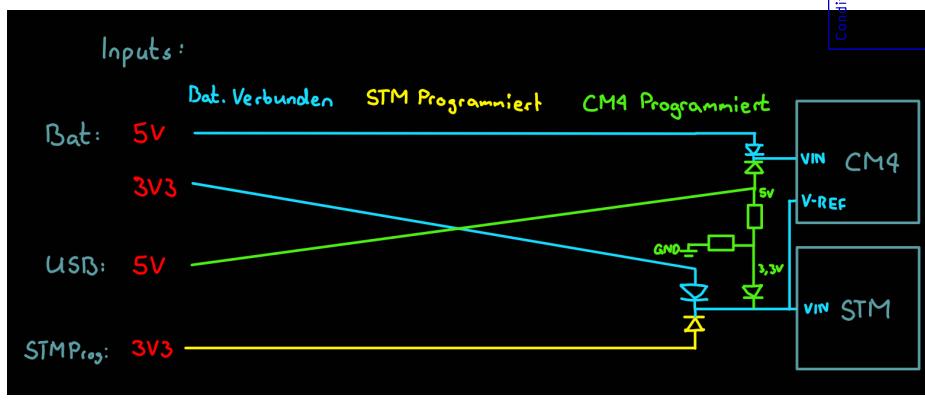
Id: 4/20

File: Piezzo.kicad_sch





Wont work... diodes are not perfect...



Title:

Sheet: /Power_logic/

Author:

Date:

Size: A4

Rev:

Id: 14/20

File: Power_logic.kicad_sch

A

A

B

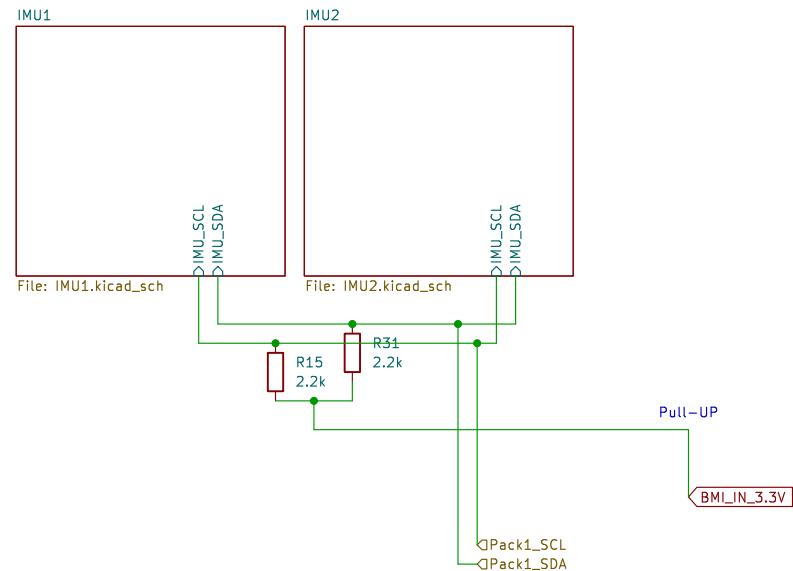
B

C

C

D

D

**Title:**

Sheet: /IMU/

Rev:

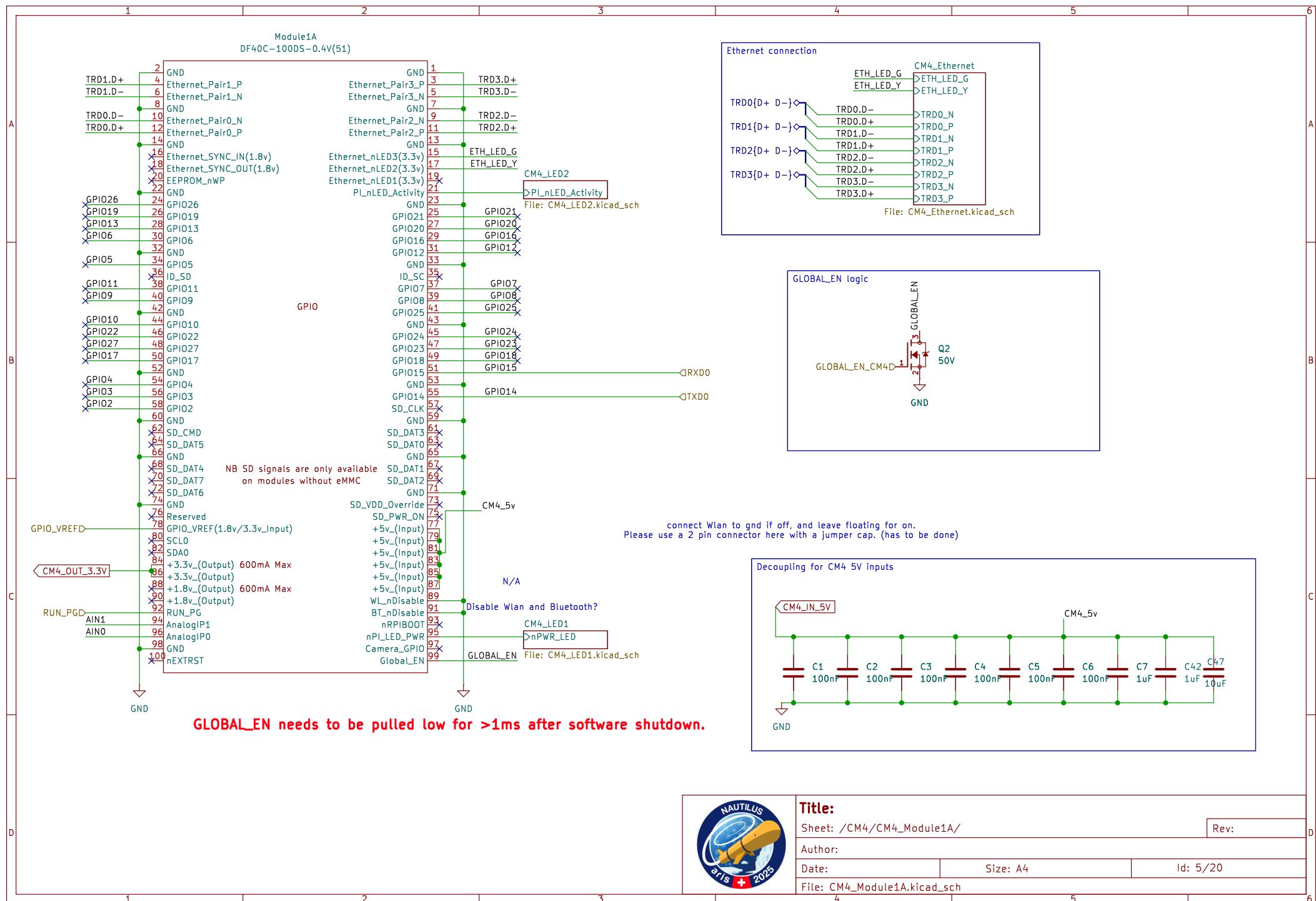
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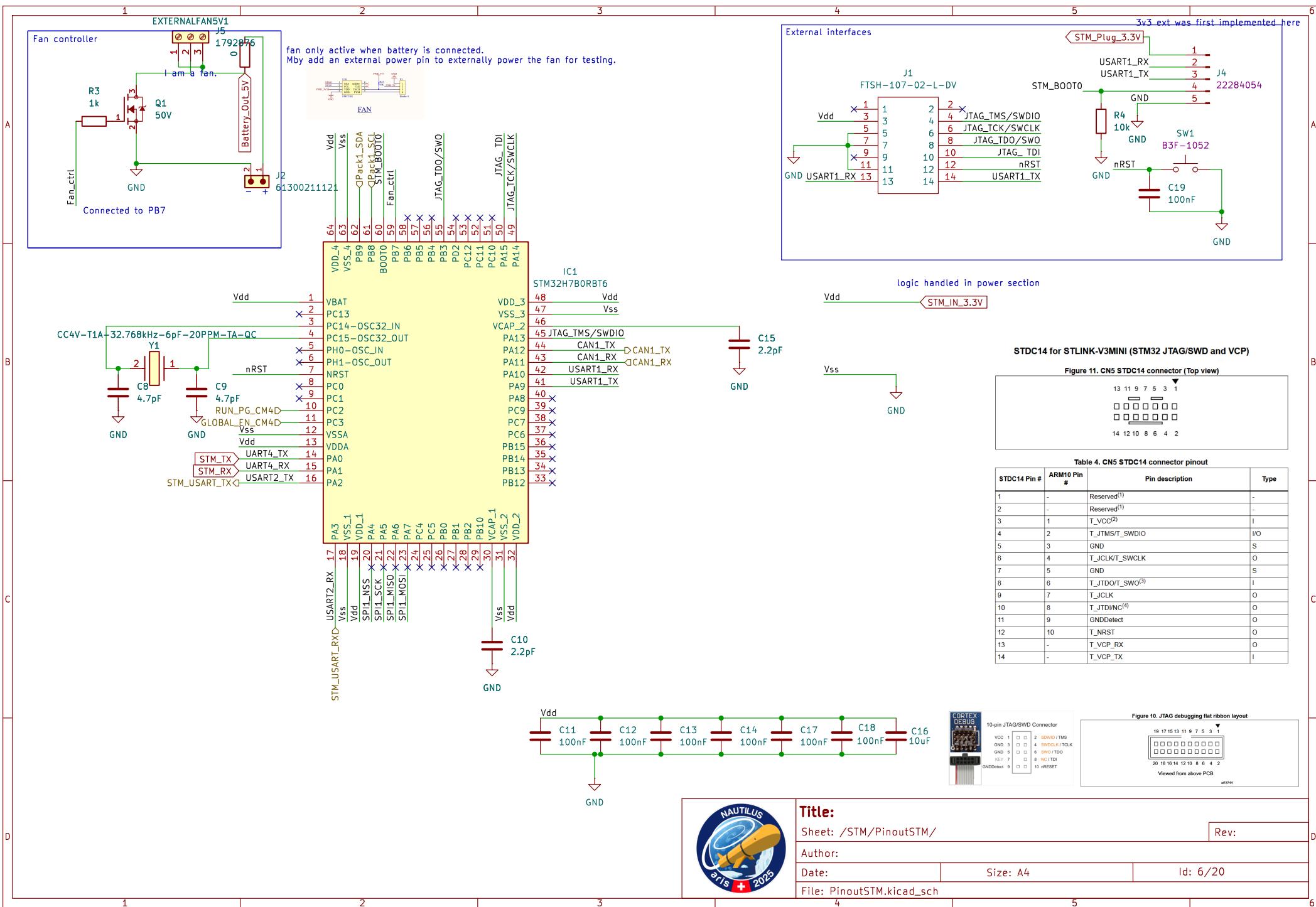
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Size: A4

Id: 18/20

File: IMU.kicad_sch





A

A

B

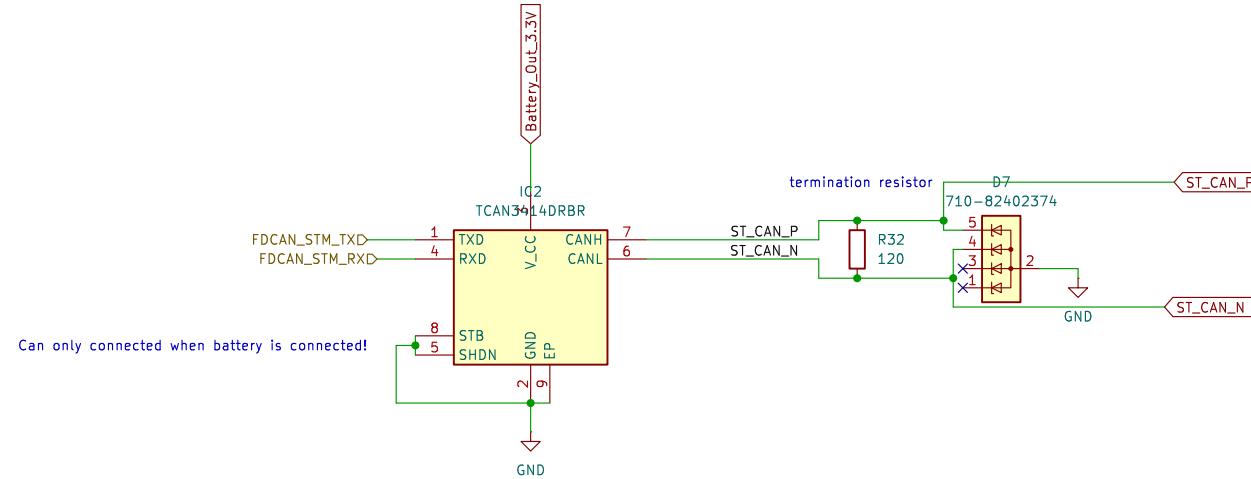
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C

C

D

D

**Title:**

Sheet: /STM/CAN_Interface/

Rev:

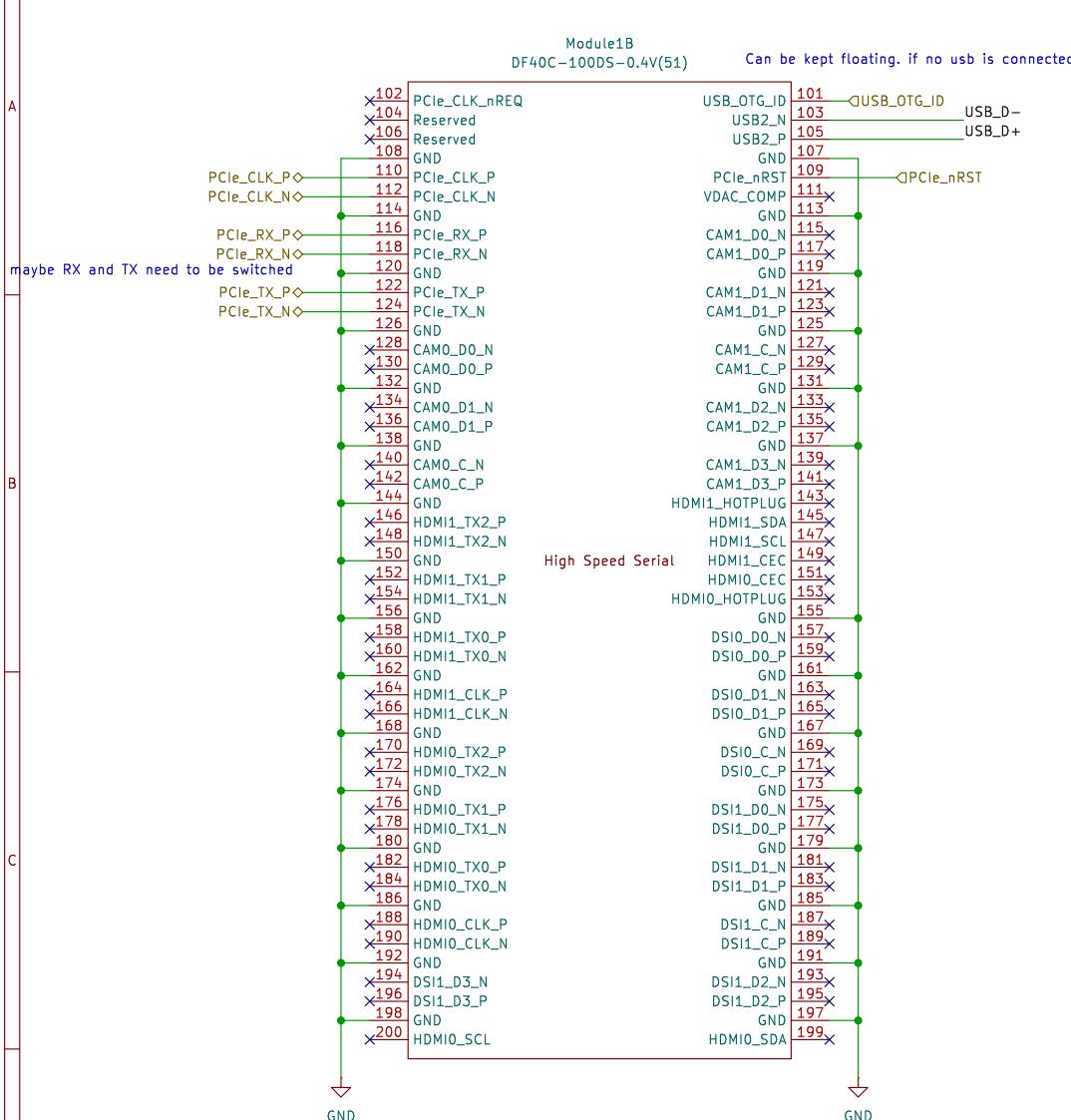
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Date:

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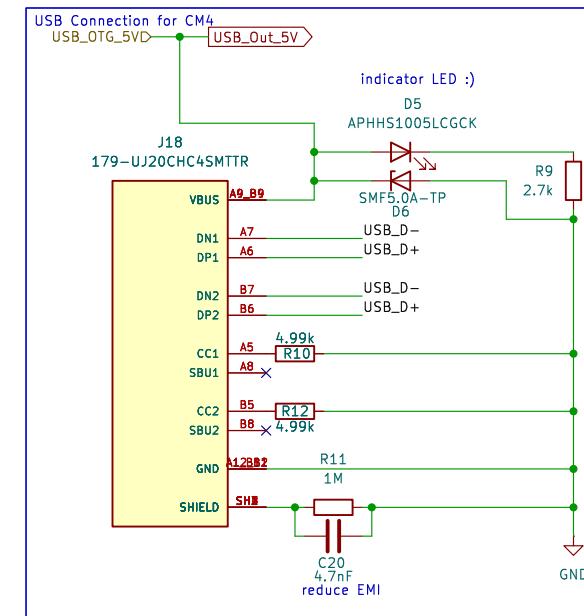
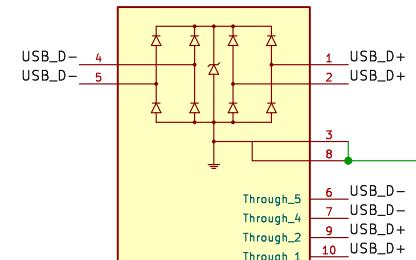
Id: 7/20

File: PowerSTM.kicad_sch



ESD/EMP protection for the USB
Super important to not differ lengths or curve a lot with D+ and D-.
Also should have same hole counts (vias) and same length.

TPD4EUSB30DQAR3



WIP, nRPI_BOOT? power only to certain parts? -> Diode (later)
indication? (YES! LED)

**Title:**

Sheet: /CM4/CM4_Module1B/

Rev:

Author:

Date:

Size: A4

Id: 11/20

File: CM4_Module1B.kicad_sch

1 2 3 4 5 6

A

A

B

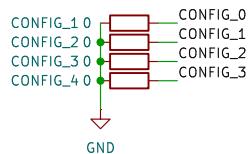
B

C

C

D

D



PCIE_RX_N ◇

PCIE_RX_P ◇

PCIE_TX_N ◇

PCIE_TX_P ◇

PCIE_CLK_N ◇

PCIE_CLK_P ◇

MDT275M02001
J6

CONFIG_3

PERn3

PERp3

PETn3

PETp3

PERn2

PERp2

CONFIG_0

PETn2

PETp2

PERn1

PERp1

PETn1

PETp1

CONFIG_1

CONFIG_2

PERn3

PERp3

PETn3

PETp3

PERn2

PERp2

CONFIG_0

PETn2

PETp2

PERn1

PERp1

PETn1

PETp1

PERn3

PERp3

PETn3

PETp3

PERn2

PERp2

CONFIG_0

PETn2

PETp2

PERn1

PERp1

PETn1

PETp1

PERn3

PERp3

PETn3

PETp3

PERn2

PERp2

CONFIG_1

CONFIG_2

PERn3

PERp3

PETn3

PETp3

PERn2

PERp2

CONFIG_0

PETn2

PETp2

PERn1

PERp1

PETn1

PETp1

PERn3

PERp3

PETn3

PETp3

PERn2

PERp2

CONFIG_1

CONFIG_2

PERn3

PERp3

PETn3

PETp3

PERn2

PERp2

CONFIG_0

PETn2

PETp2

PERn1

PERp1

PETn1

PETp1

PERn3

PERp3

PETn3

PETp3

PERn2

PERp2

CONFIG_1

CONFIG_2

PERn3

PERp3

PETn3

PETp3

PERn2

PERp2

CONFIG_0

PETn2

PETp2

PERn1

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CONFIG_1

CONFIG_2

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PERn1

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CONFIG_1

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PETn3

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CONFIG_1

CONFIG_2

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CONFIG_0

PETn2

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PERn1

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CONFIG_1

CONFIG_2

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CONFIG_0

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PETp2

PERn1

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PERn3

PERp3

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CONFIG_1

CONFIG_2

PERn3

PERp3

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PETp3

PERn2

PERp2

CONFIG_0

PETn2

PETp2

PERn1

PERp1

PETn1

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PERn2

PERp2

CONFIG_1

CONFIG_2

PERn3

PERp3

PETn3

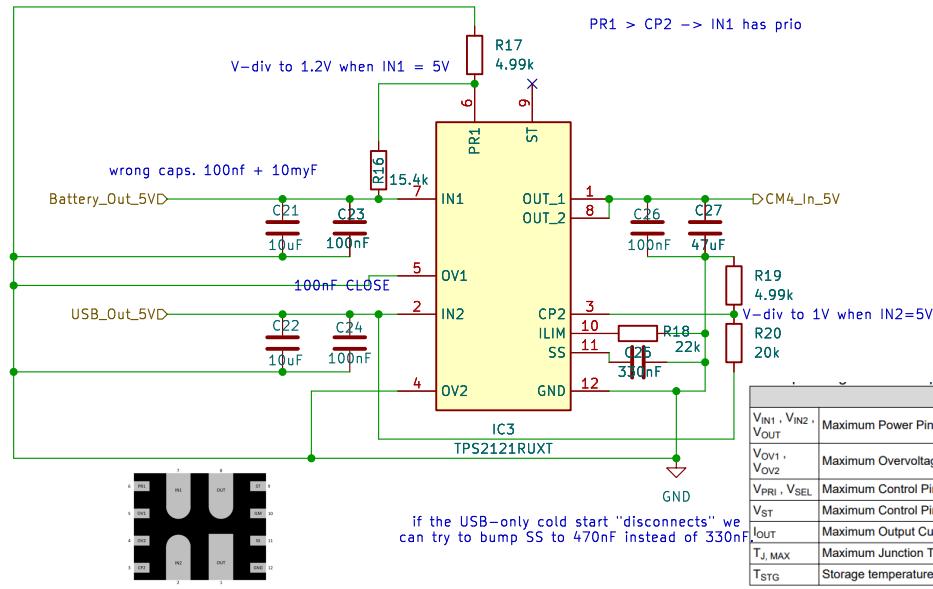
PETp3

PERn2

PERp2

CONFIG_0

for questions about wiring etc please consult the datasheet...
<https://www.ti.com/lit/ds/symlink/tps2120.pdf?ts=1761678178328>



		Pins	MIN	MAX	UNIT
V_{IN1} , V_{IN2} , V_{OUT}	Maximum Power Pin Voltage	IN1, IN2, OUT	-0.3	24	V
V_{OV1} , V_{OV2}	Maximum Overvoltage Pin Voltage	OV1, OV2	-0.3	6	V
V_{PRI} , V_{SEL}	Maximum Control Pin Voltage	PRI, SEL	-0.3	6	V
V_{ST}	Maximum Control Pin Voltage	ST	-0.3	6	V
I_{OUT}	Maximum Output Current	OUT	Internally Limited		
T_J, MAX	Maximum Junction Temperature		Internally Limited		
T_{STG}	Storage temperature		-65	150	°C

Pin Functions					
NAME	PIN	TPS2120 WCB1	TPS2121 VQFN-24	IO	DESCRIPTION
IN1	B1	1	1	I	Power Input for Source 1
IN2	B1, BA, C4	2	2	I	Power Input for Source 2
OUT	C2, C3, D1	1, B	—	I	Power Output
ST	E1	9	—	O	Status output indicating which channel is selected. Connect to GND if not required.
ILIM	E2	10	—	O	Output Current Limiting for both channels.
GND	E4	12	11	—	Device Ground
PRI	A1	6	—	I	Enables Priority Operation. Connect to VDD to set switcher voltage. Connect to GND if not required.
DV1	A2	5	—	I	Active Low Enable for INT1 Overvoltage Protection. Connect to GND if not required.
DV2	A3	4	—	I	Active Low Enable for INT2 Overvoltage Protection. Connect to GND if not required.
SEL	A4	—	—	I	Active low enable for INT1. Allows GPG to override priority operation and manually select INT2. INT2 can only trigger.
CP2	—	3	1	Enables Compare Operation and is compared to PRI to set switcher voltage.	



Title

Sheet: /Power Logic /5V Logic /

Rev.

Autobus

Date: _____ Size: _____

Page 15 / 20

A

A

B

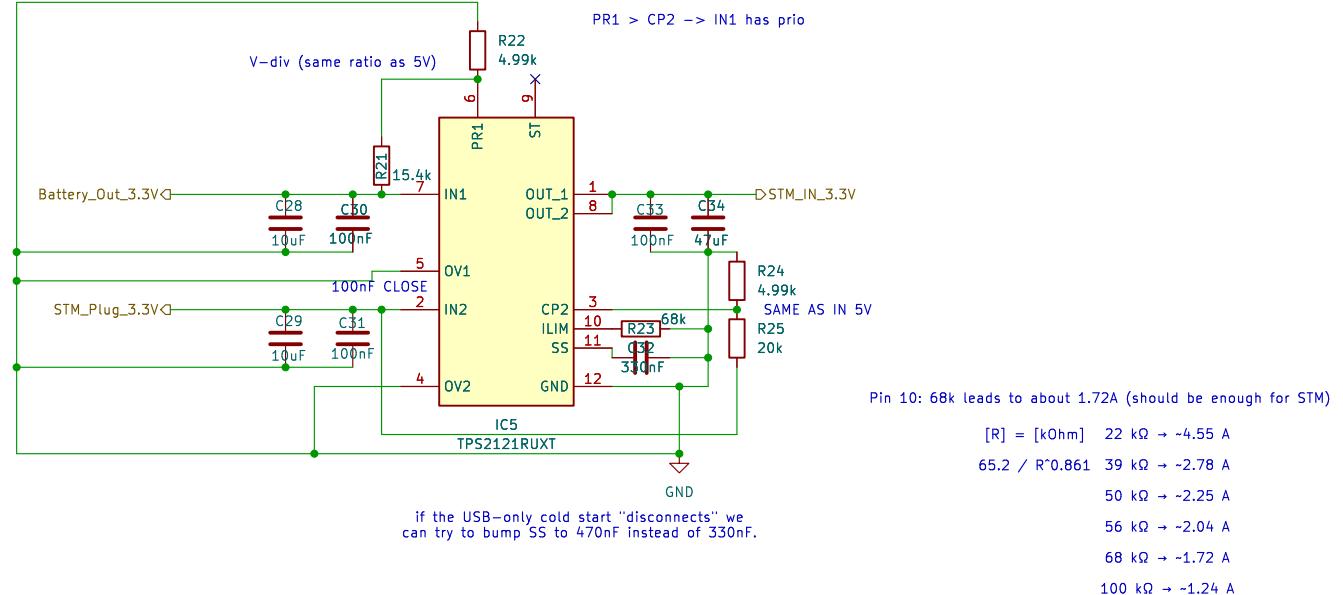
B

C

C

D

D

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Rev:

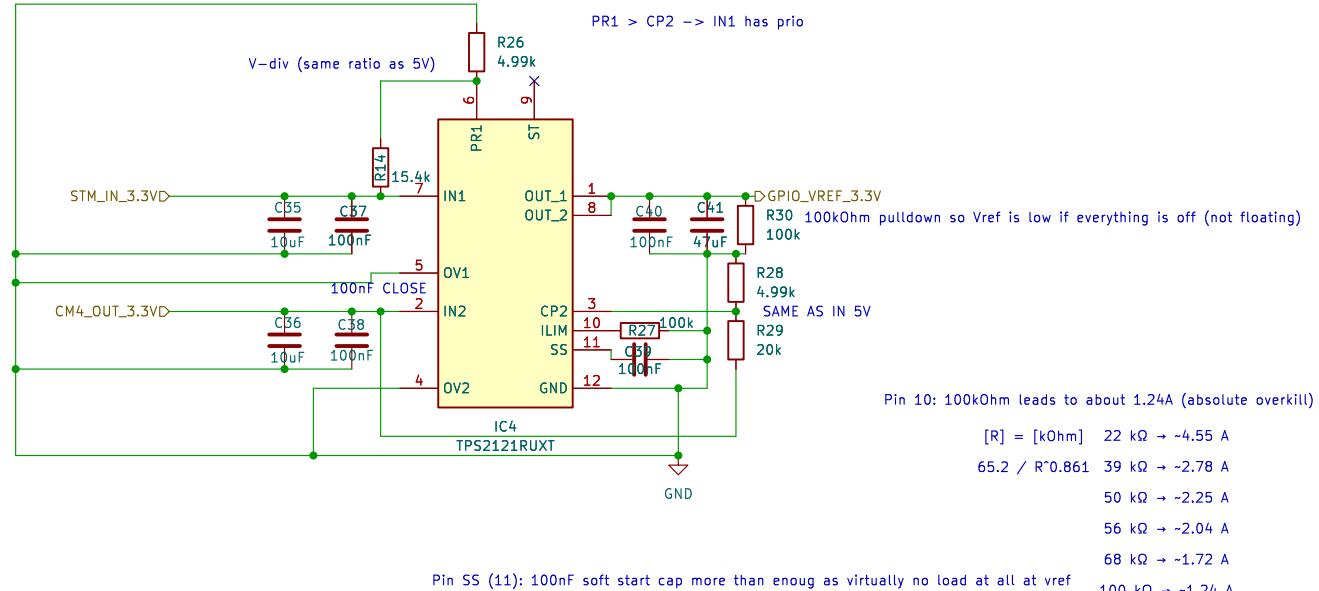
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Date:

Size: A4

Id: 16/20

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Title

Sheet: /Power logic/GPIO REF3.3V/

Rev:

Author:

Data:

File: GPIO_REF3_3V.kicad.sch

Id: 17/20

A

A

B

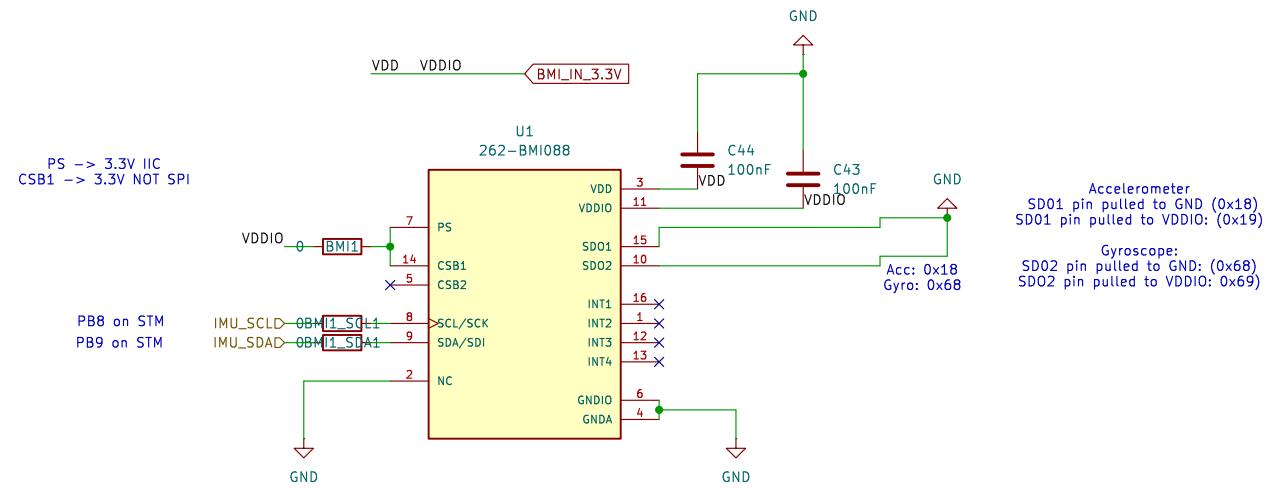
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C

D

D

**Title:**

Sheet: /IMU/IMU1/

Rev:

Author:

Date:

Size: A4

Id: 19/20

File: IMU1.kicad_sch

A

A

B

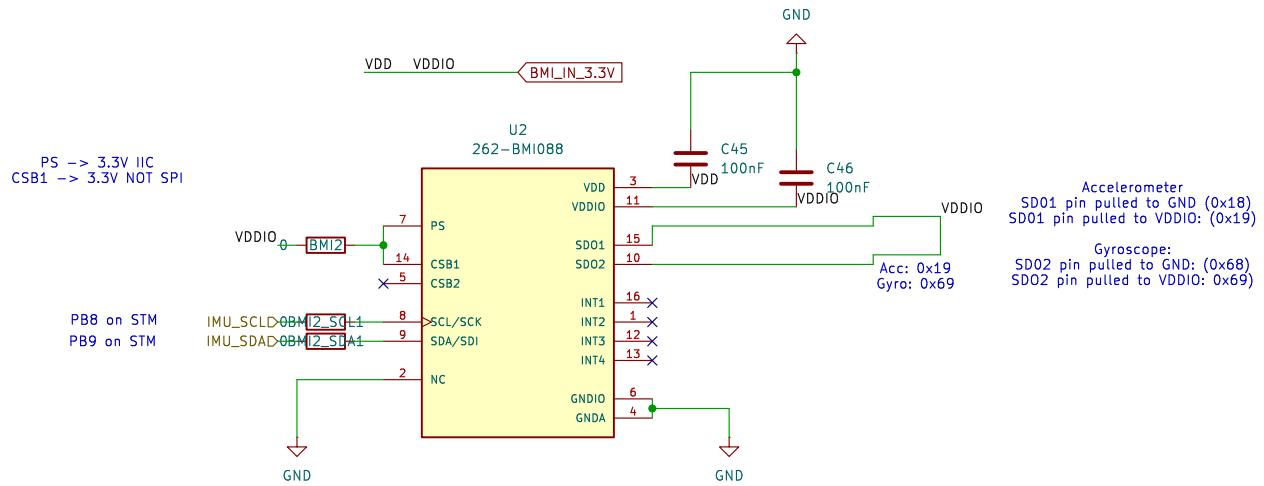
B

C

C

D

D

**Title:**

Sheet: /IMU/IMU2/

Rev:

Author:

Date:

Size: A4

Id: 20/20

File: IMU2.kicad_sch

A

A

B

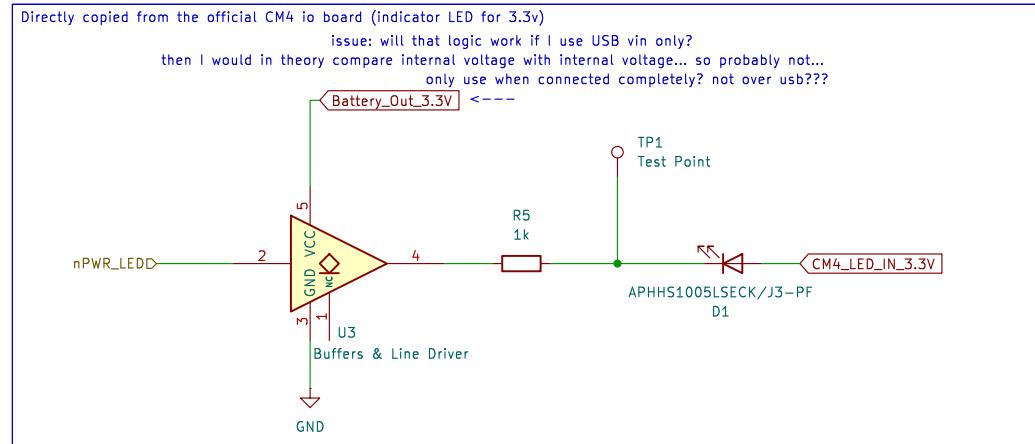
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C

C

D

D

**Title:**

Sheet: /CM4/CM4_Module1A/CM4_LED1/

Rev:

Author:

Date:

Size: A4

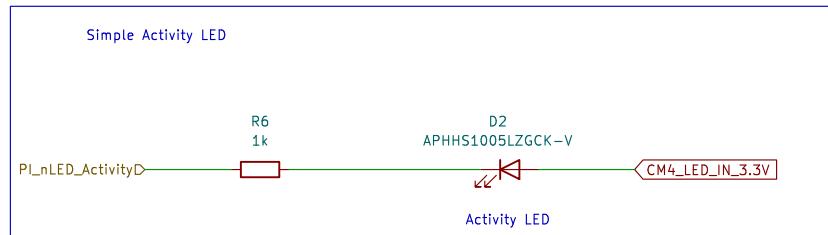
Id: 8/20

File: CM4_LED1.kicad_sch

1 2 3 4 5 6

A

A



B

B

C

C

D

D



Title:

Sheet: /CM4/CM4_Module1A/CM4_LED2/

Rev:

Author:

Date:

Size:

A4

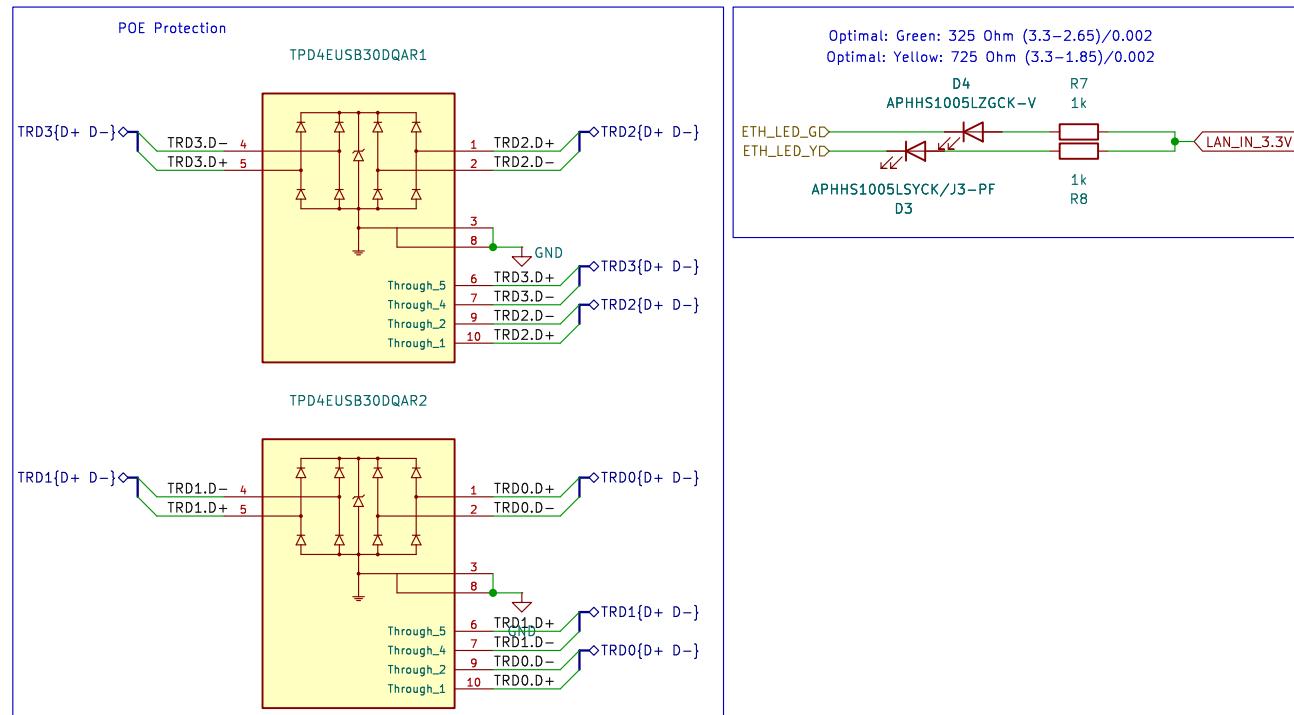
Id: 9/20

File: CM4_LED2.kicad_sch

1 2 3 4 5 6

A

A



B

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D

**Title:**

Sheet: /CM4/CM4_Module1A/CM4_Ethernet/

Rev:

Author:

Date:

Size: A4

Id: 10/20

File: CM4_Ethernet.kicad_sch