

We should consider that we NEVER want the CM4 to power the unpowered STM over the TX pin. Found a neat part for that:

<https://www.mouser.ch/ProductDetail/Texas-Instruments/SN74LVC1G126DBVR?qs=pajglaoyDUI3T2WgNNfd3w%3D%3D>

connections:

Pin 5: VCC → CM4_3V3

Pin 2: A → CM4 TX (PLTX)

Pin 4: Y → STM_UART_RX

Pin 1: OE → STM_IN_3.3V

Pin 3: GND

0.1uF decoupling cap VCC-GND



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Author: /

Date: /

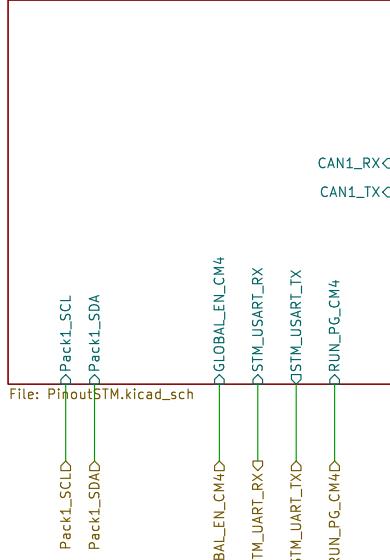
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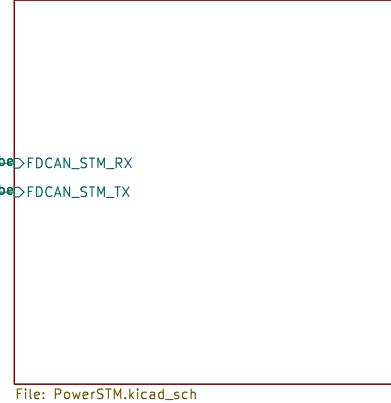
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220 Ohm series at Y (to STM). (current limiting)

PinoutSTM



CAN_Interface



A

A

B

B

C

C

D

D

**Title:**

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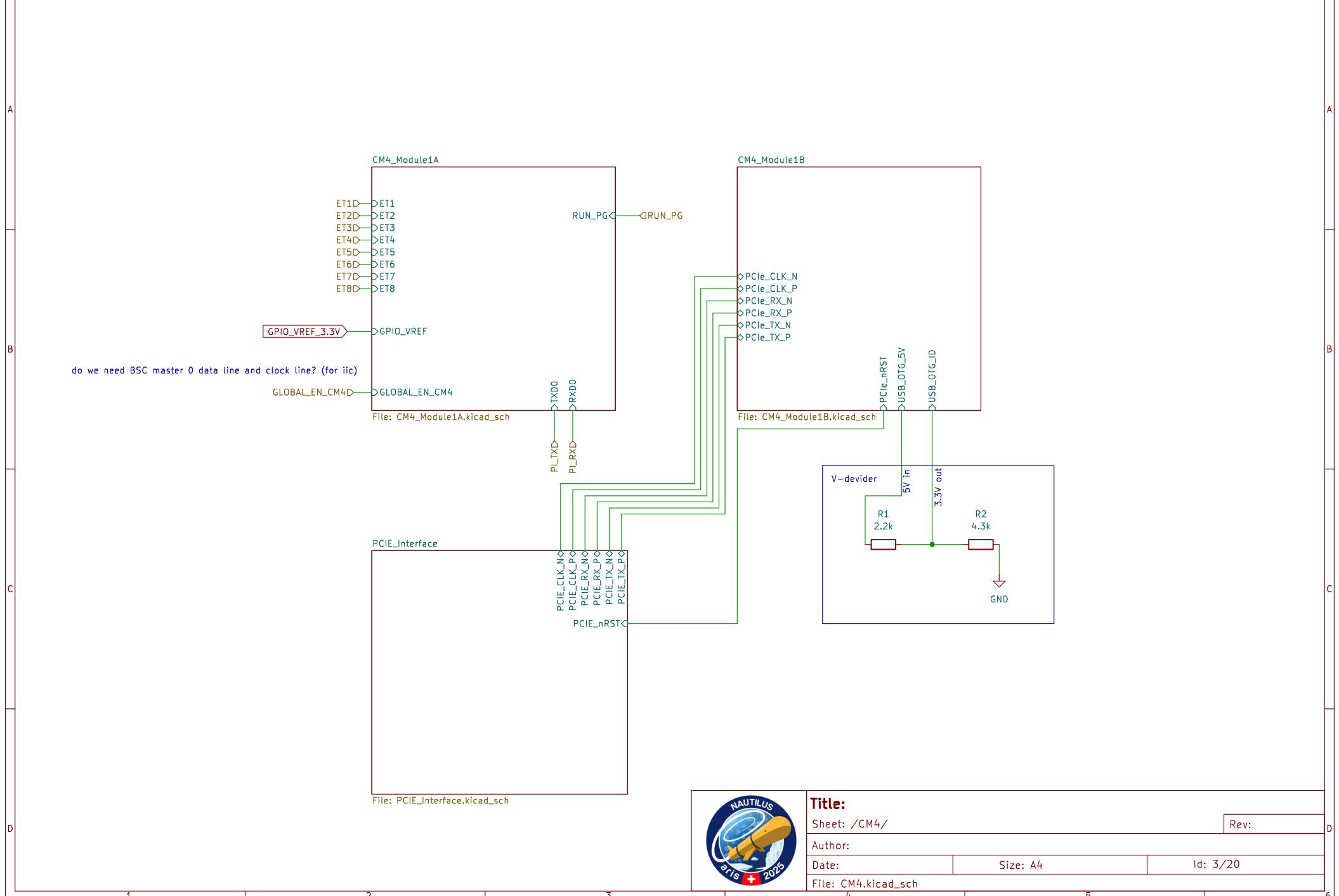
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A

A

B

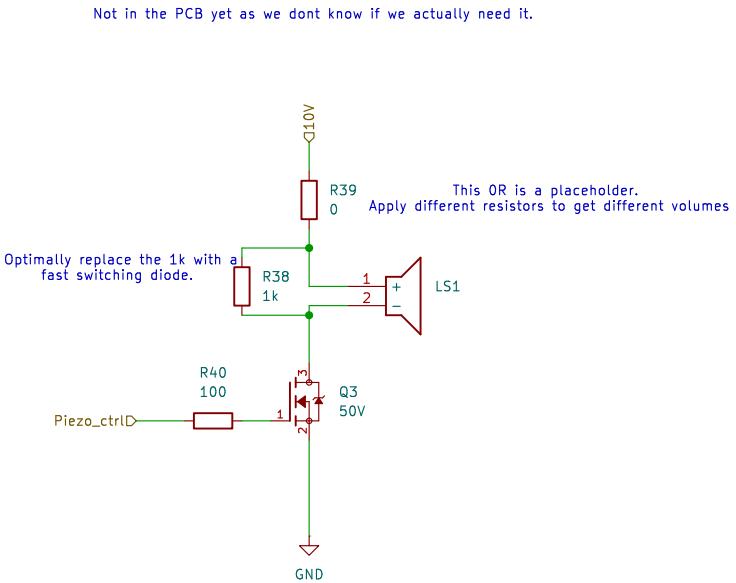
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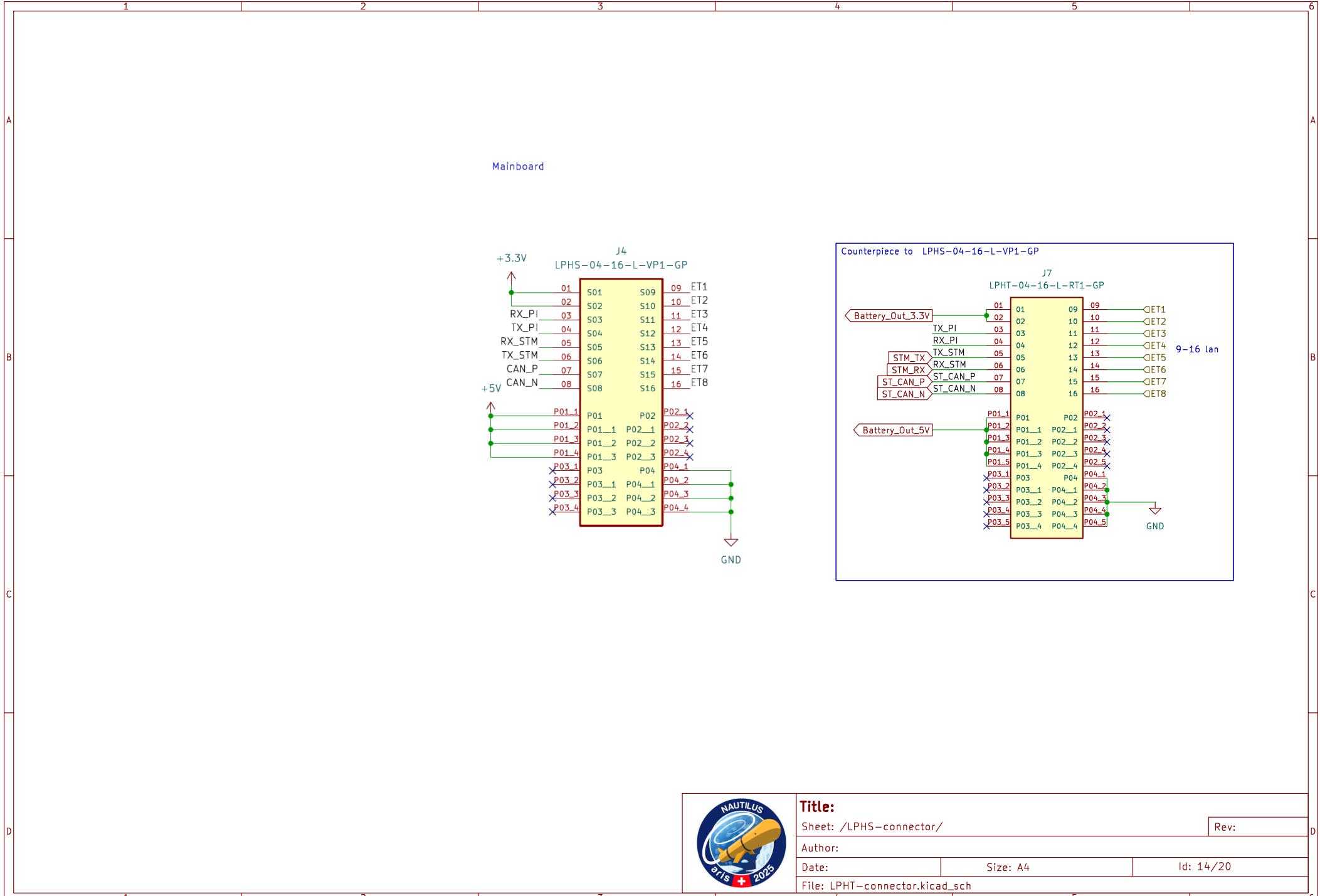
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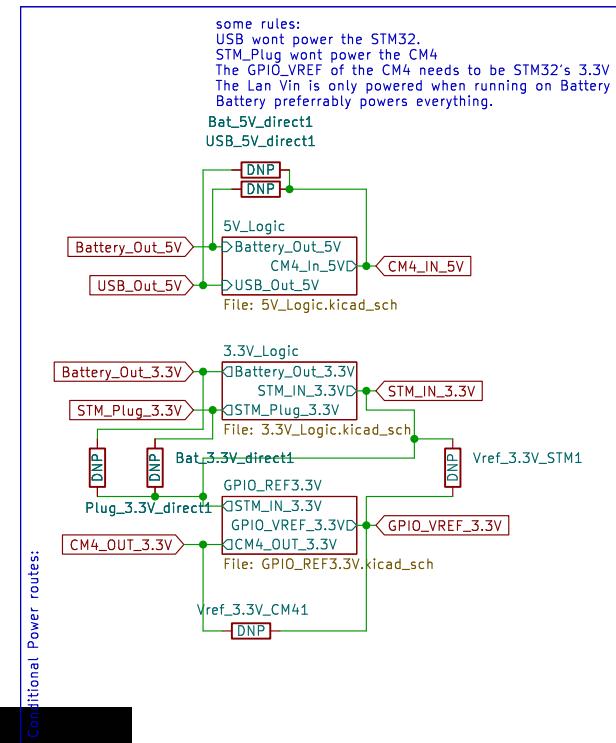
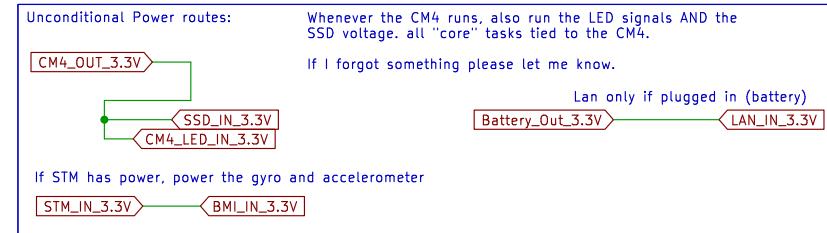
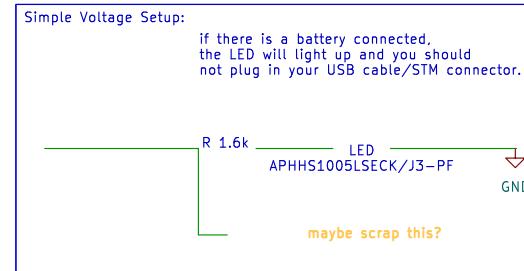
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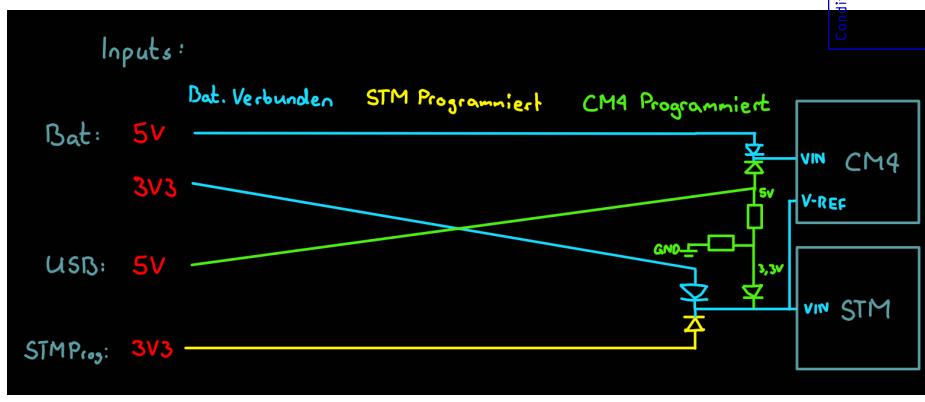
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Wont work... diodes are not perfect...



Title:

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Author:

Date:

Size: A4

Rev:

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A

A

B

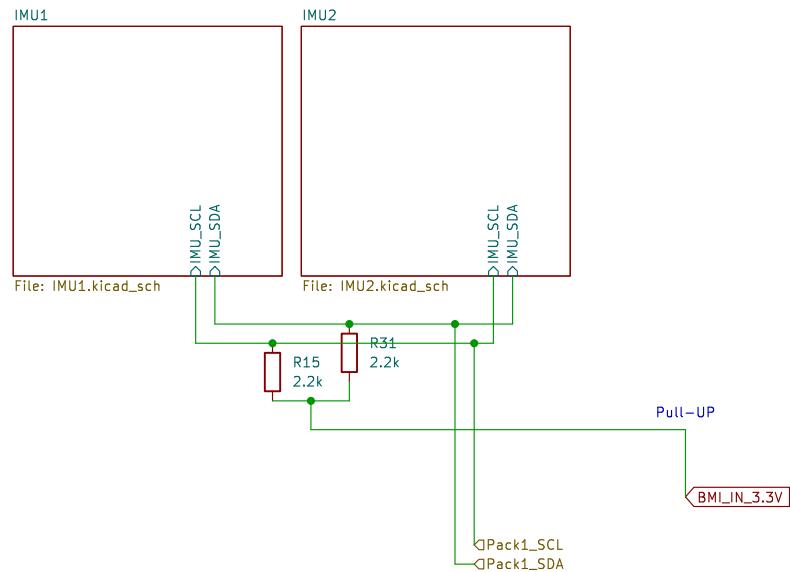
B

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D

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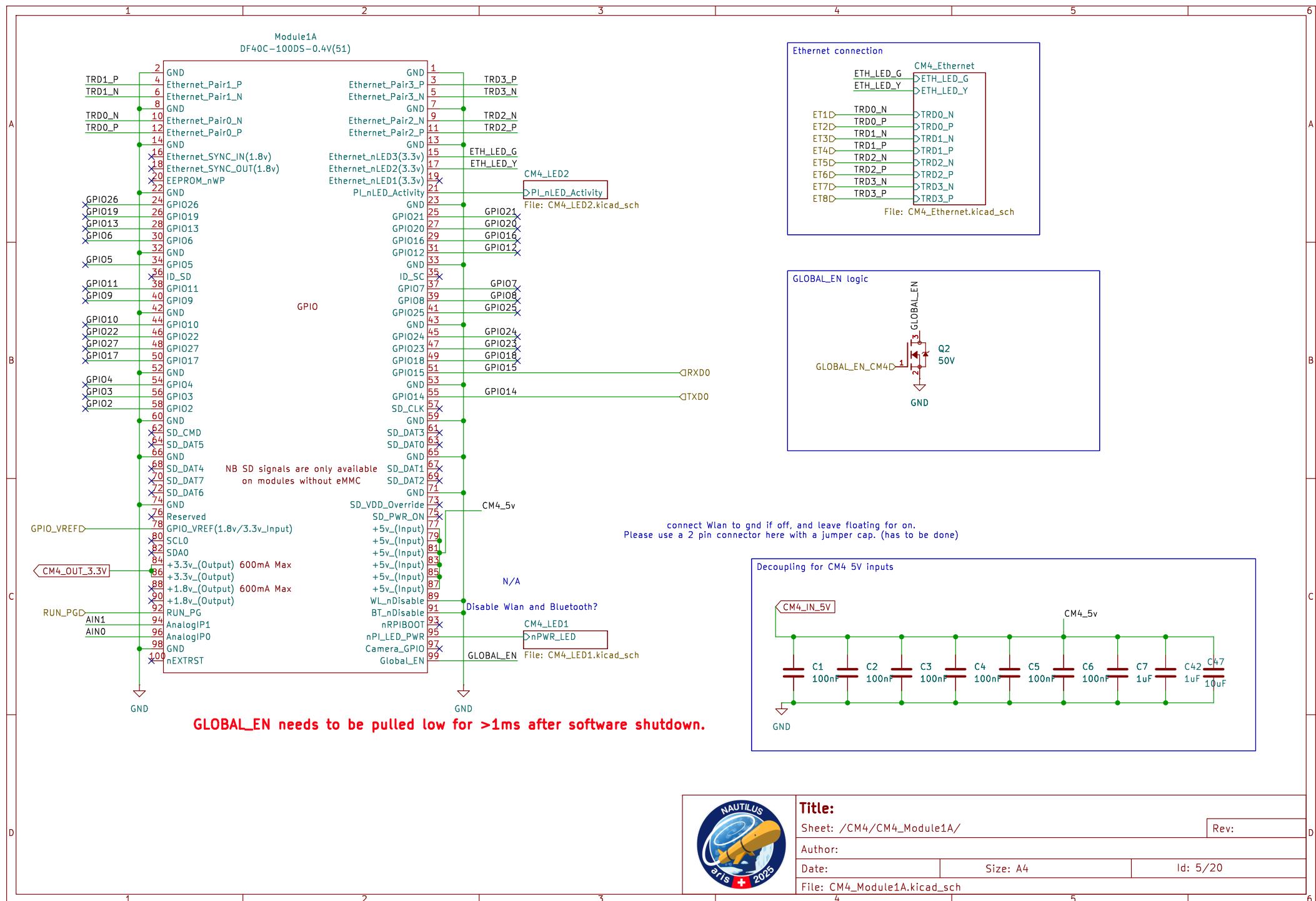
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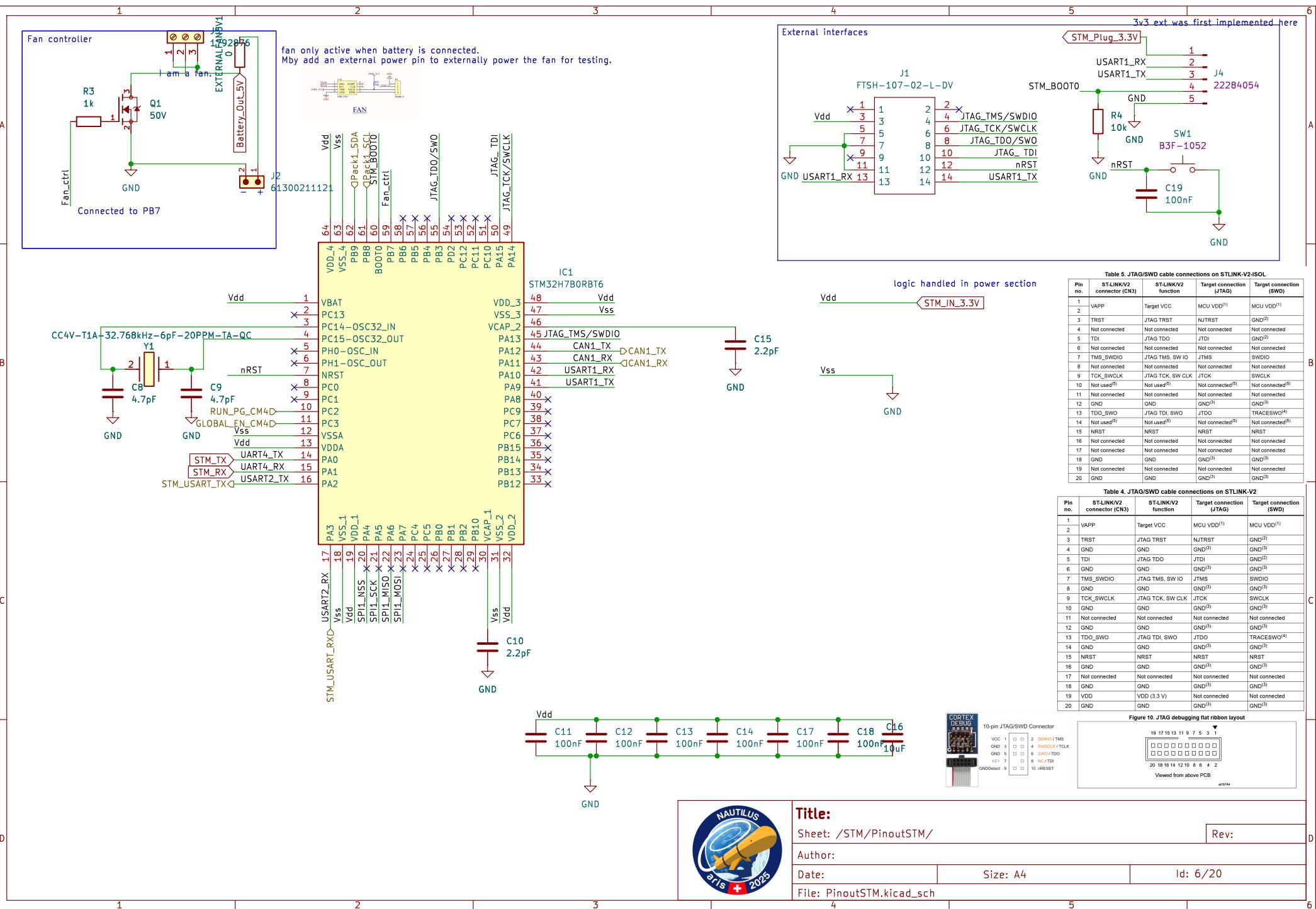
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A

A

B

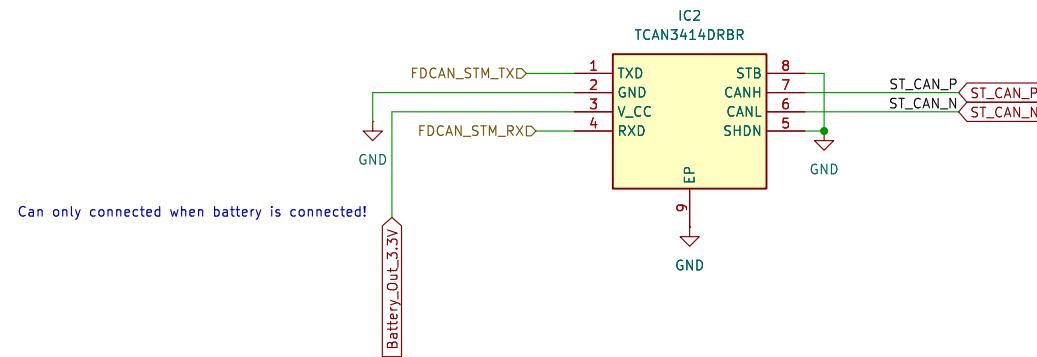
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C

D

D

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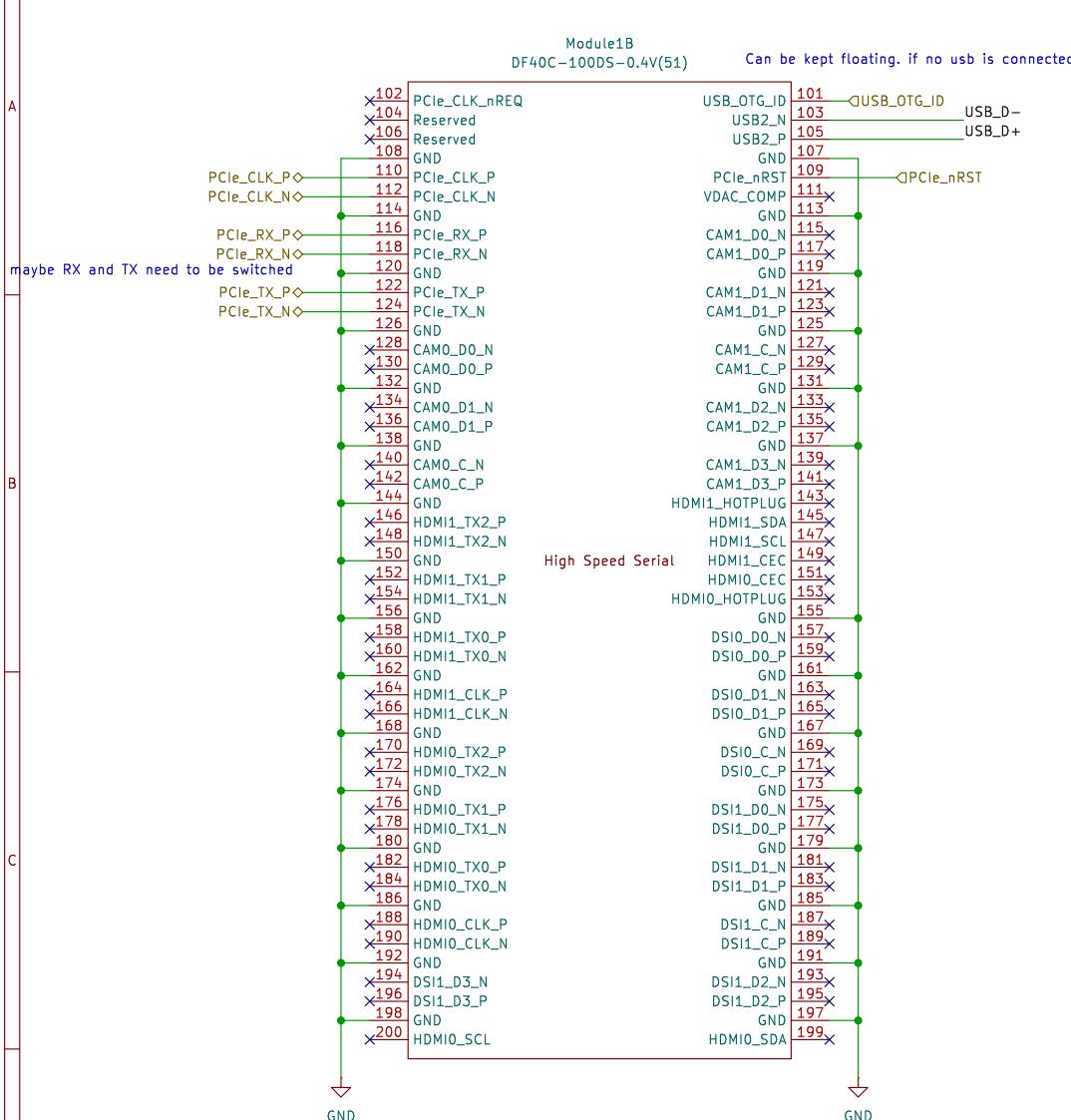
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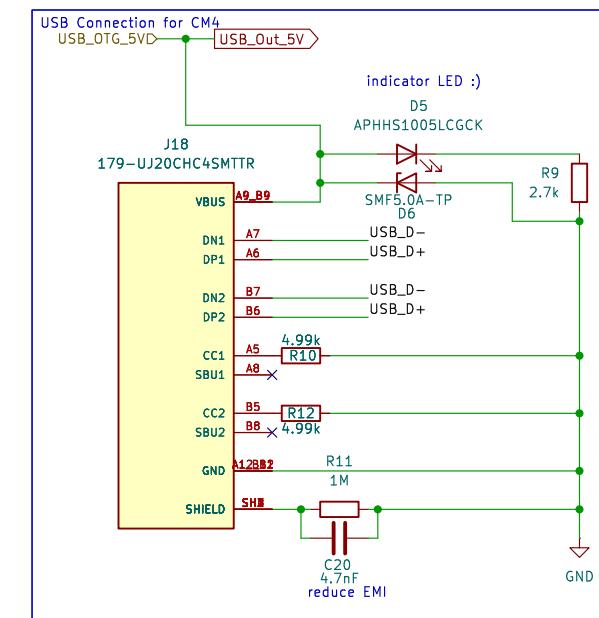
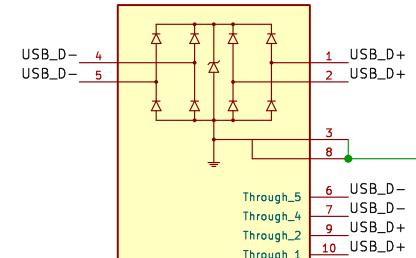
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ESD/EMP protection for the USB
Super important to not differ lengths or curve a lot with D+ and D-.
Also should have same hole counts (vias) and same length.

TPD4EUSB30DQAR3

**Title:**

Sheet: /CM4/CM4_Module1B/

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Author:

Date: Size: A4

Id: 11/20

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1 2 3 4 5 6

A

A

B

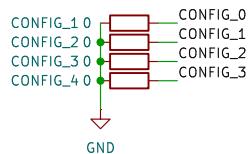
B

C

C

D

D



PCIE_RX_N ◇

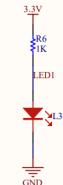
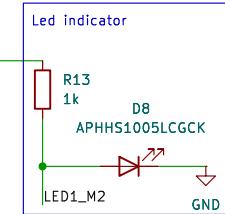
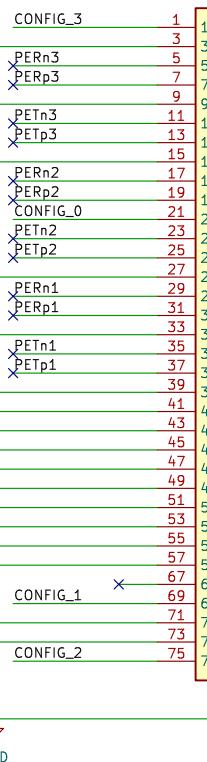
PCIE_RX_P ◇

PCIE_TX_N ◇

PCIE_TX_P ◇

PCIE_CLK_N ◇

PCIE_CLK_P ◇

MDT275M02001
J6

Title:

Sheet: /CM4/PCIE_Interface/

Rev:

Author:

Date: Size: A4

Id: 13/20

File: PCIE_Interface.kicad_sch



1 2 3 4 5 6

A

A

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for questions about wiring etc please consult the datasheet..
<https://www.ti.com/lit/ds/symlink/tps2120.pdf?ts=1761678178328>

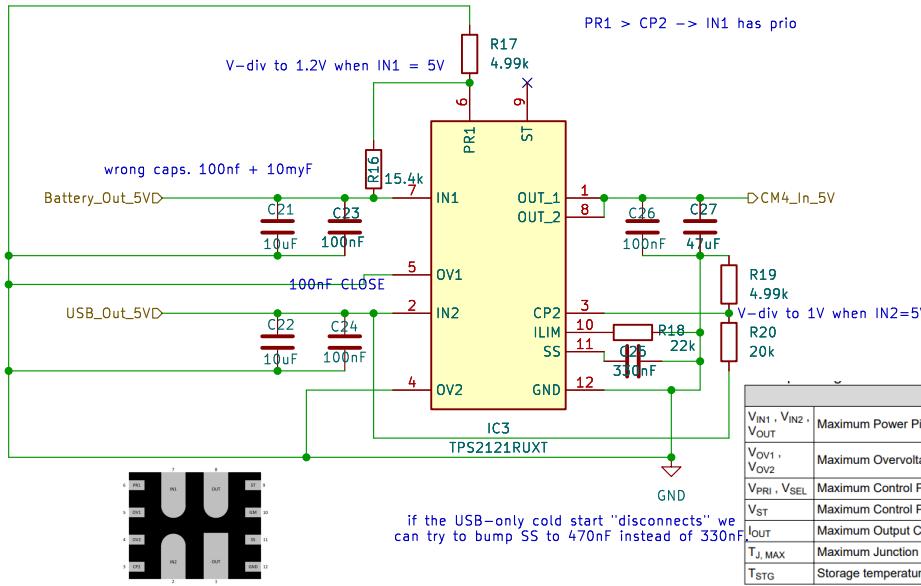


Figure 6-2. TPS2121 (RUX) Package 12-Pin VQFN-HR Bottom View

Pin Functions			
NAME	TPS2120	TPS2121	
PIN	TPS2120	TPS2121	
NAME	TPS2120	TPS2121	
IO	VQFN-HR		
DESCRIPTION			
PIN1	B1, B2, C1	1	Power Input for Source 1
IN2	B3, B4, C4	2	Power Input for Source 2
OUT	C2, C3, D1, D2	1, 8	Power Output
GND	D3, D4	3	Ground
ST	E1	9	Status output indicating which channel is selected. Connect to GND if not required.
ILIM	E2	10	Output Current Limiting for both channels.
SS	E3	11	Adjusts Input Setting Delay Time and Output Soft Start Time
GND	E4	12	Ground
PR1	A1	—	Enables Priority Operation. Connect to IN1 to set switchover voltage. Connect to GND if not required.
OV1	A2	5	Active Low Enable Supervisor for IN1 Overvoltage Protection. Connect to GND if not required.
OV2	A3	4	Active Low Enable Supervisor for IN2 Overvoltage Protection. Connect to GND if not required.
SEL	A4	—	Active Low Enable for IN1. Allows GPIO to override priority operation and manually select IN2. TPS2120 only.
CP2	—	3	Enables Comparator Operation and is compared to PR1 to set switchover voltage. Connect to GND if not required. TPS2121 only.

**Title:**

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Rev:

Author:

Date:

Size: A4

Id: 15/20

File: 5V_Logic.kicad_sch

A

A

B

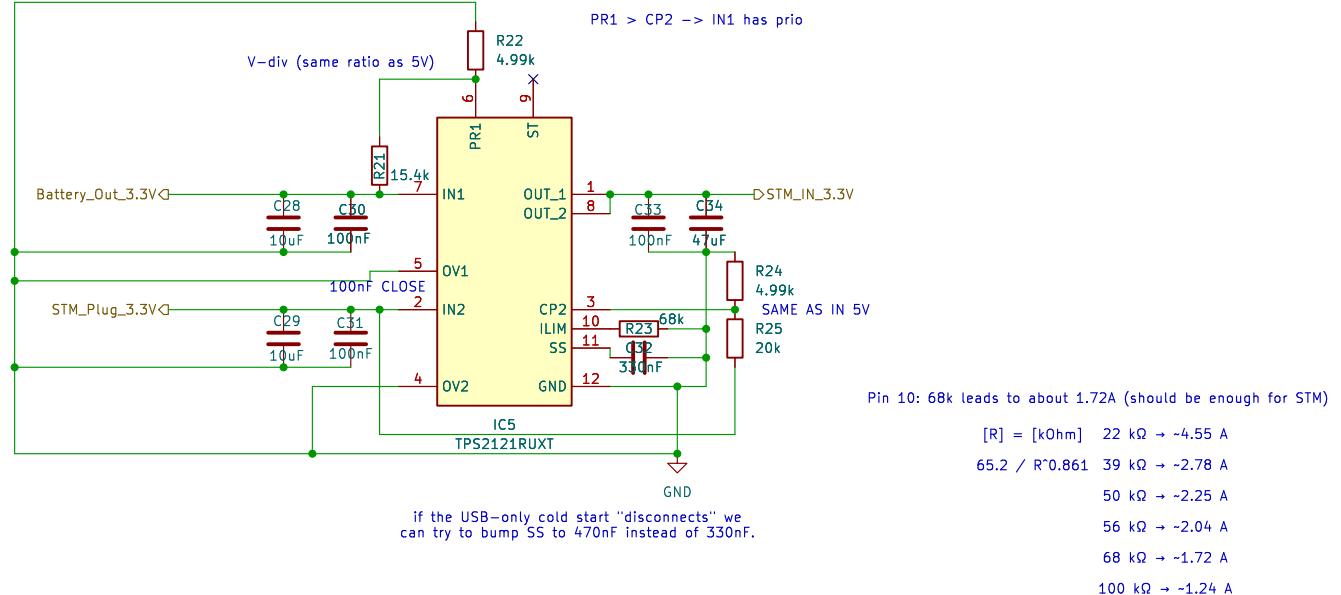
B

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D

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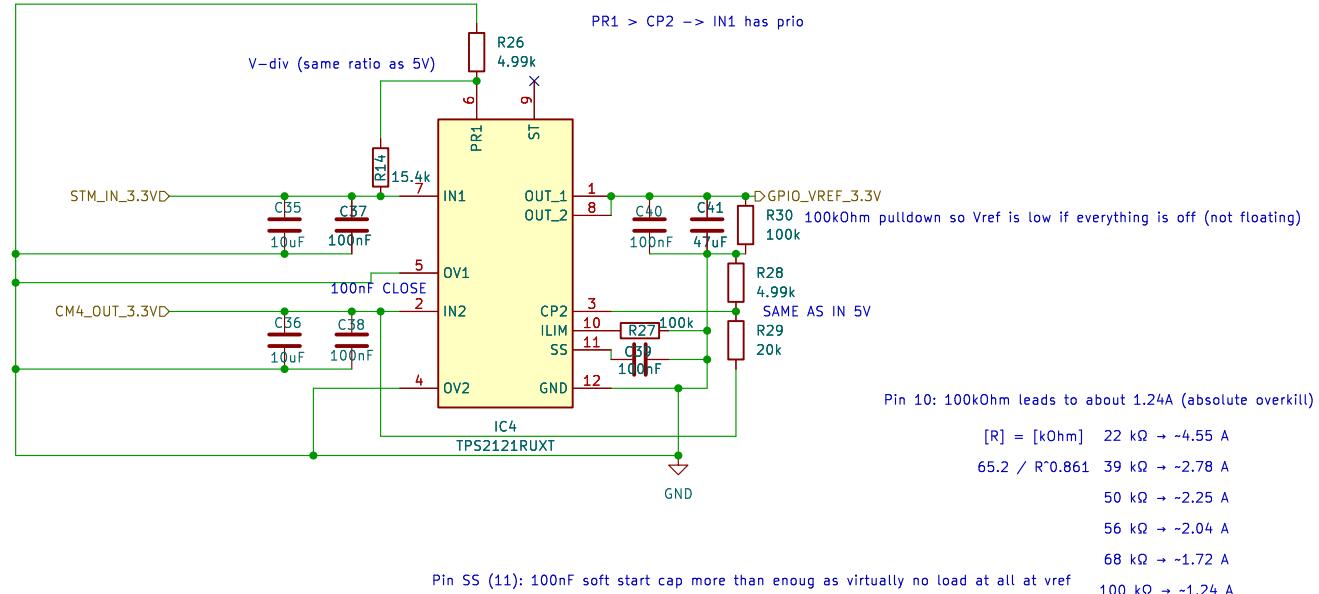
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Date:

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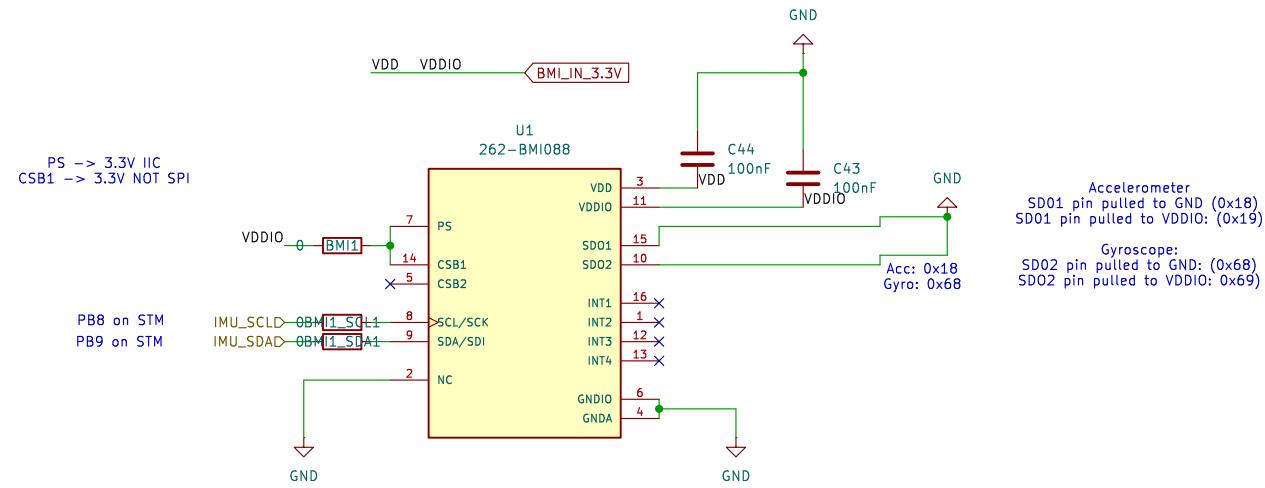
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Title

Sheet: /IMU/IMU1/

Author:

Date:

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Rev:

D

A

A

B

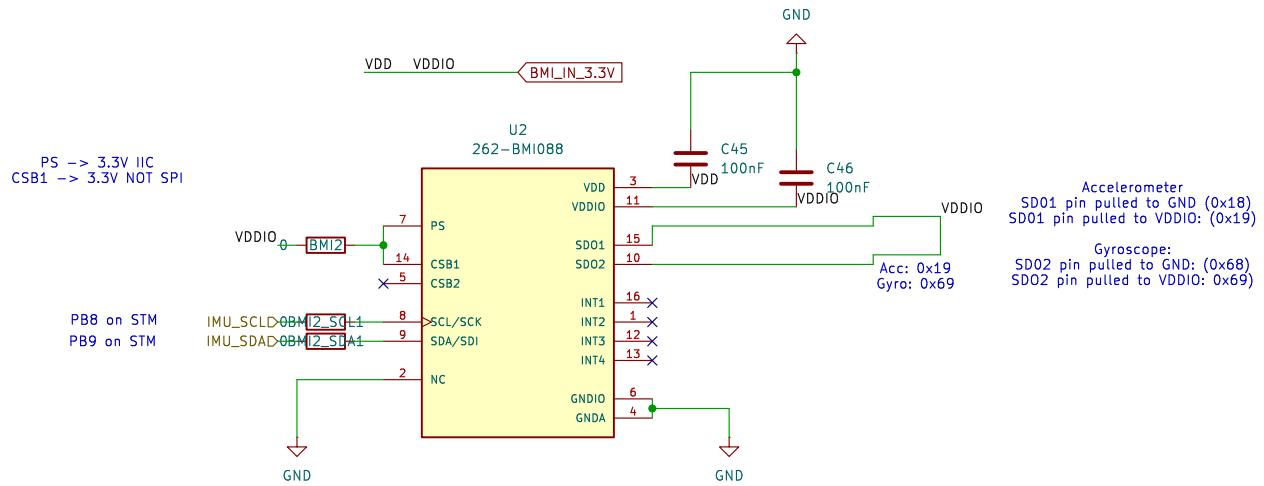
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D

**Title:**

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Rev:

Author:

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A

A

B

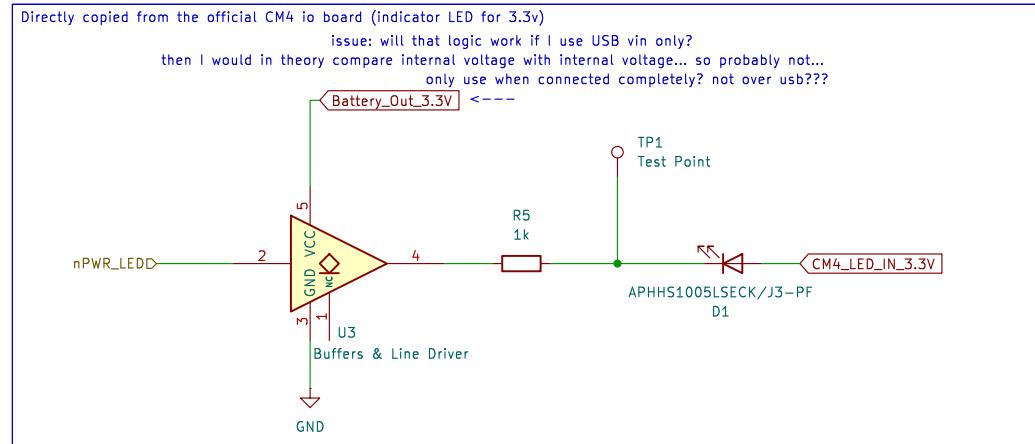
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Rev:

Author:

Date:

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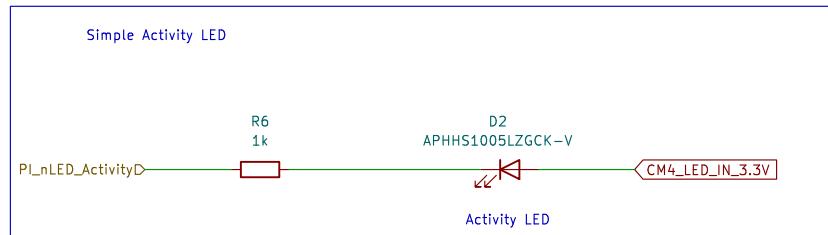
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1 2 3 4 5 6

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A



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Rev:

Author:

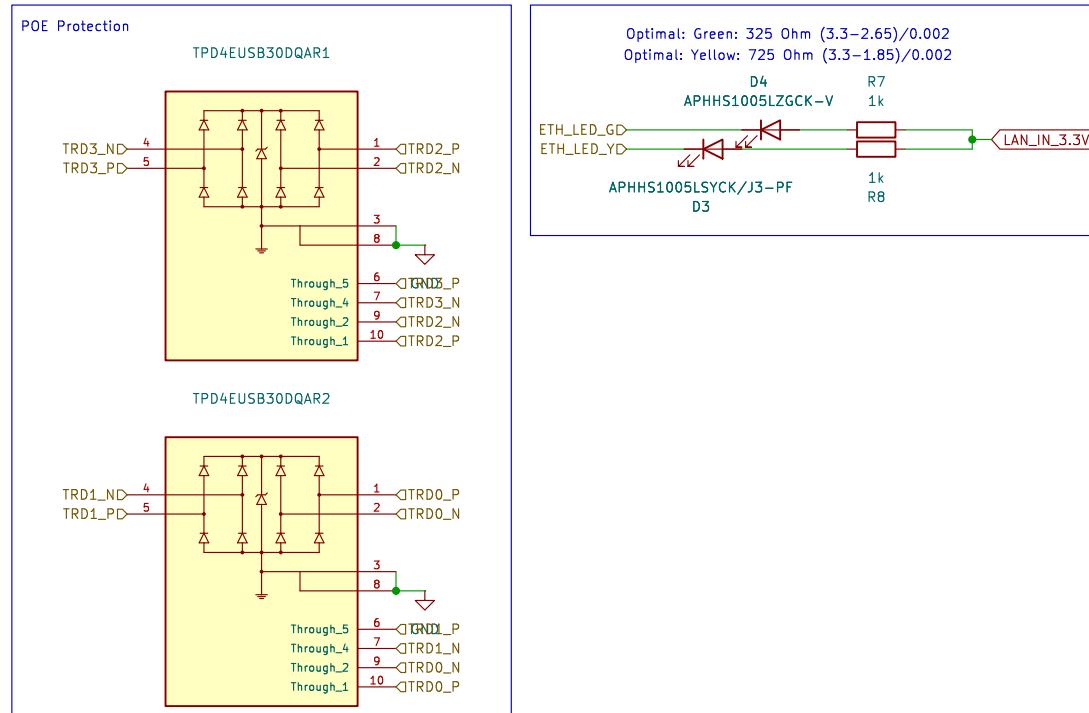
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1 2 3 4 5 6

A

A



B

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Rev:

Author:

Date:

Size: A4

Id: 10/20

File: CM4_Ethernet.kicad_sch