

We should consider that we NEVER want the CM4 to power the unpowered STM over the TX pin. Found a neat part for that:

<https://www.mouser.ch/ProductDetail/Texas-Instruments/SN74LVC1G126DBVR?qs=pajglaoyDUI3T2WgNNfd3w%3D%3D>

connections:

Pin 5: VCC → CM4_3V3

Pin 2: A → CM4 TX (PLTX)

Pin 4: Y → STM_UART_RX

Pin 1: OE → STM_IN_3.3V

Pin 3: GND

0.1uF decoupling cap VCC-GND



Title:

Sheet: /

Rev: D

Author:

Date:

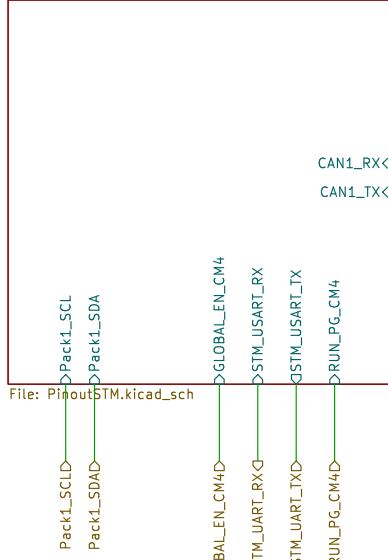
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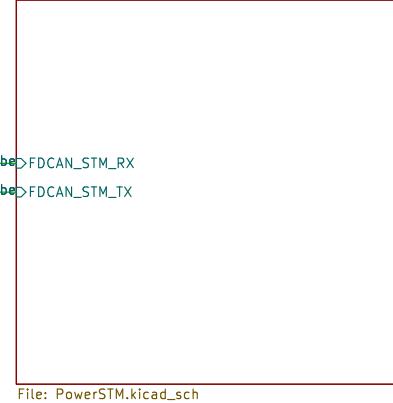
File: nautilus_mainboard.kicad_sch

220 Ohm series at Y (to STM). (current limiting)

PinoutSTM



CAN_Interface



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**Title:**

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Rev:

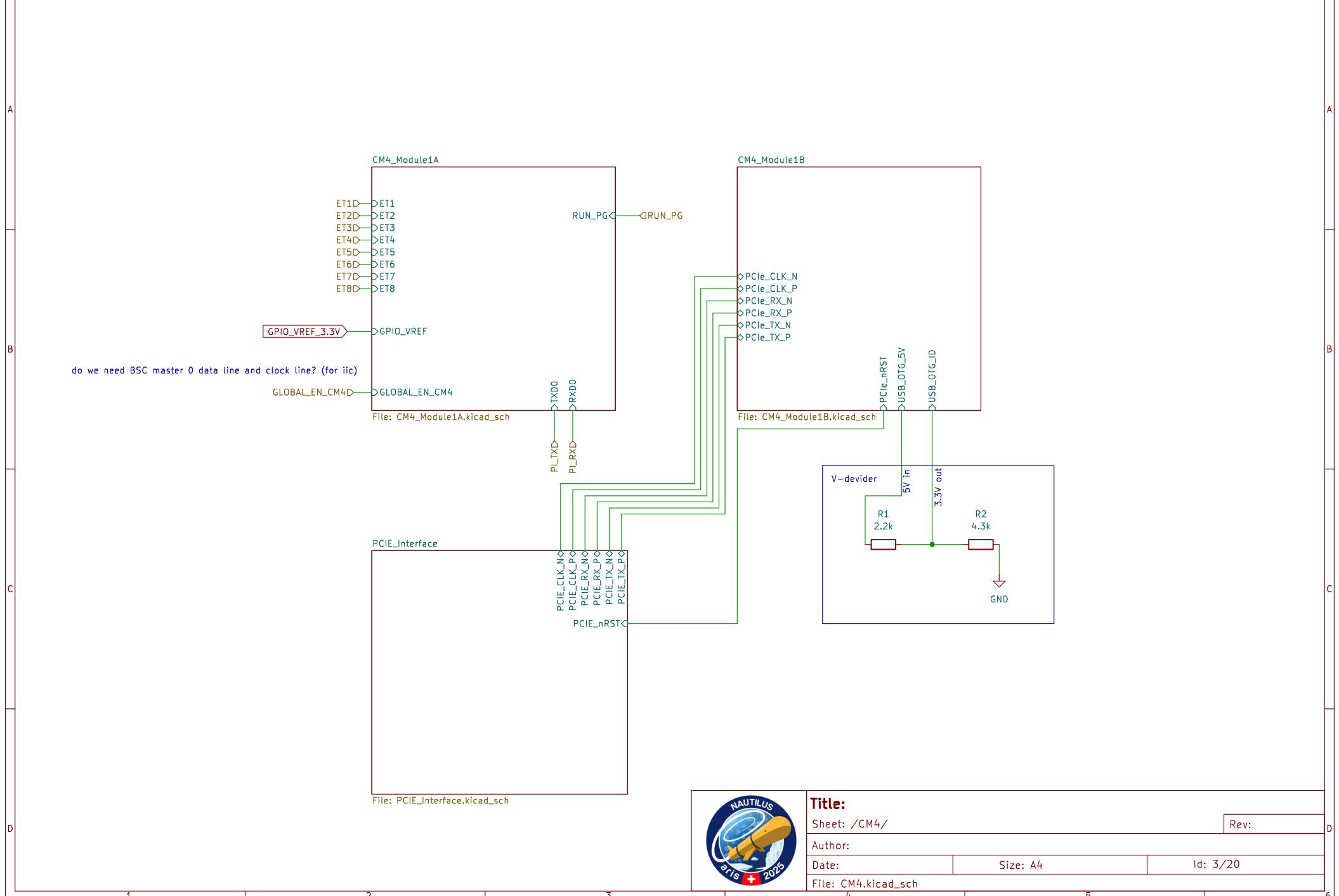
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A

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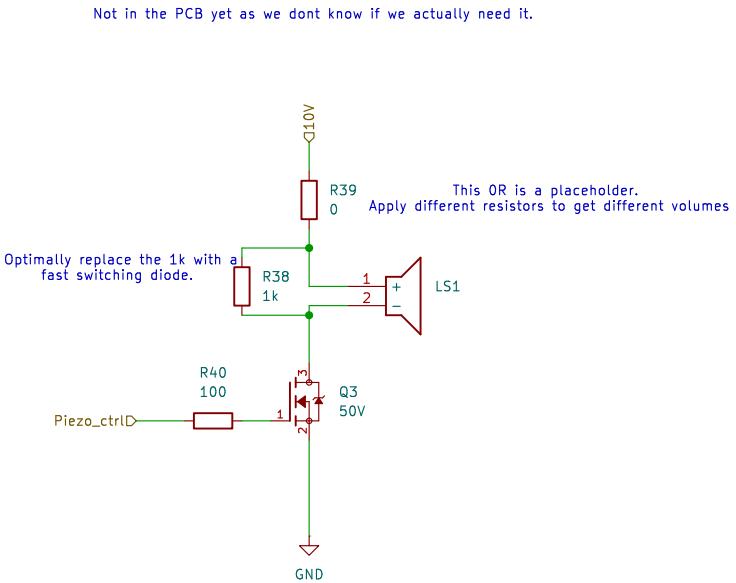
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Rev:

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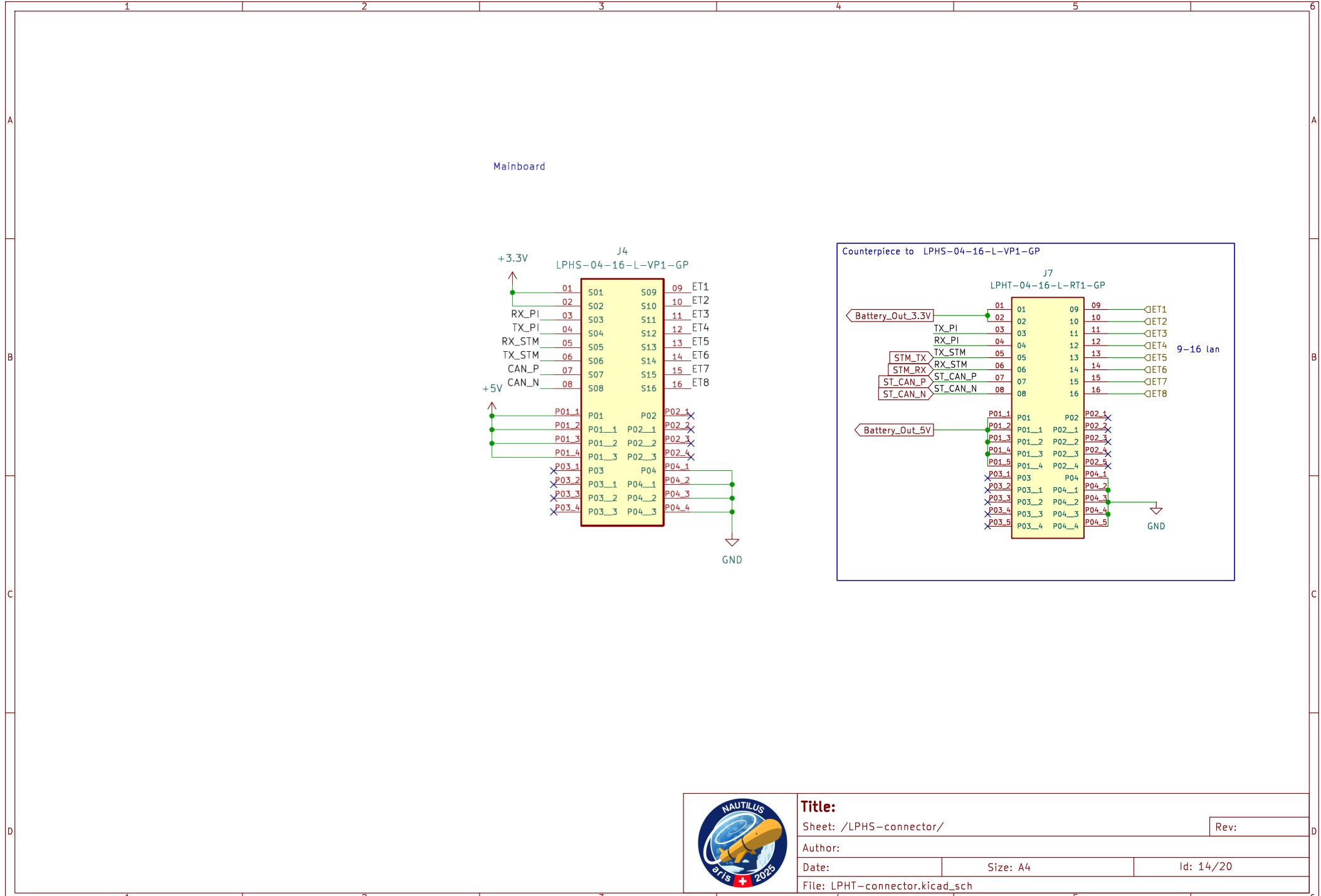
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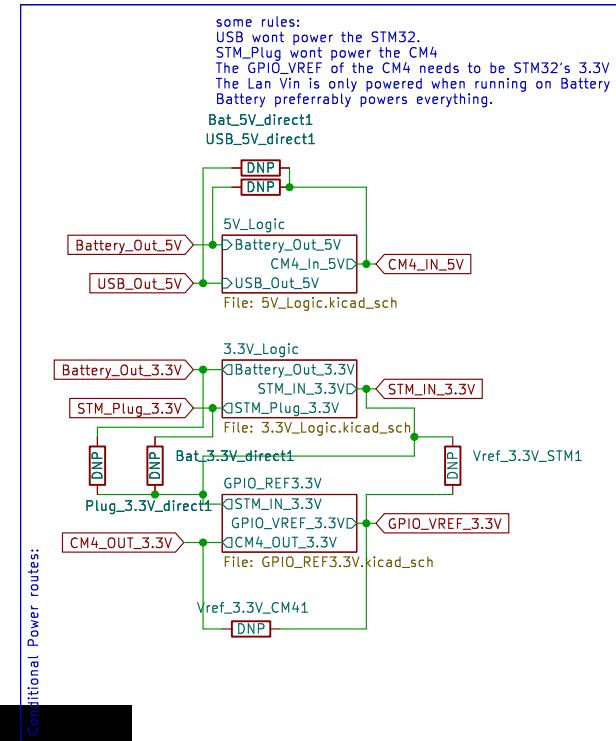
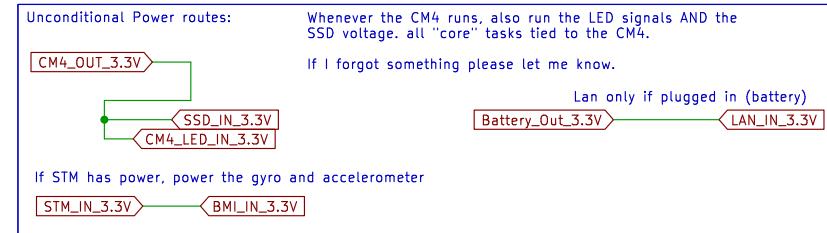
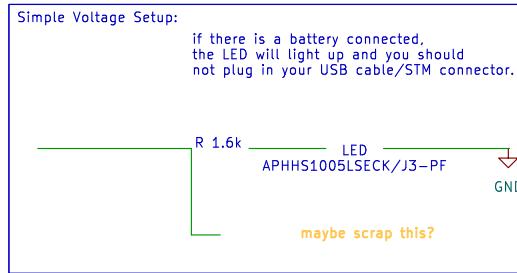
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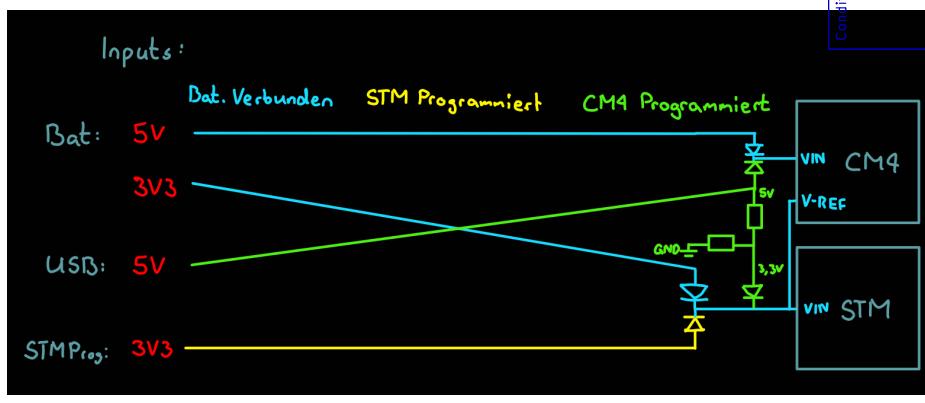
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Wont work... diodes are not perfect...



Title:

Sheet: /Power_logic/

Author:

Date:

Size: A4

Rev:

Id: 14/20

File: Power_logic.kicad_sch

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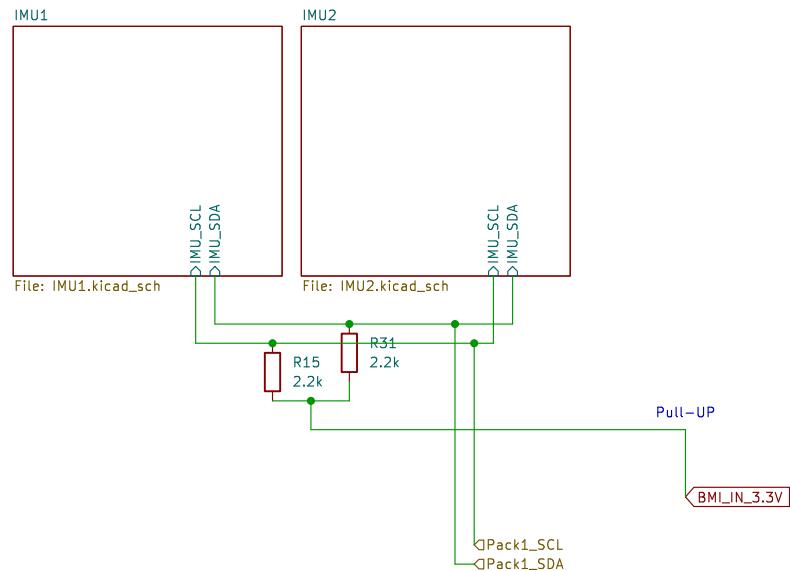
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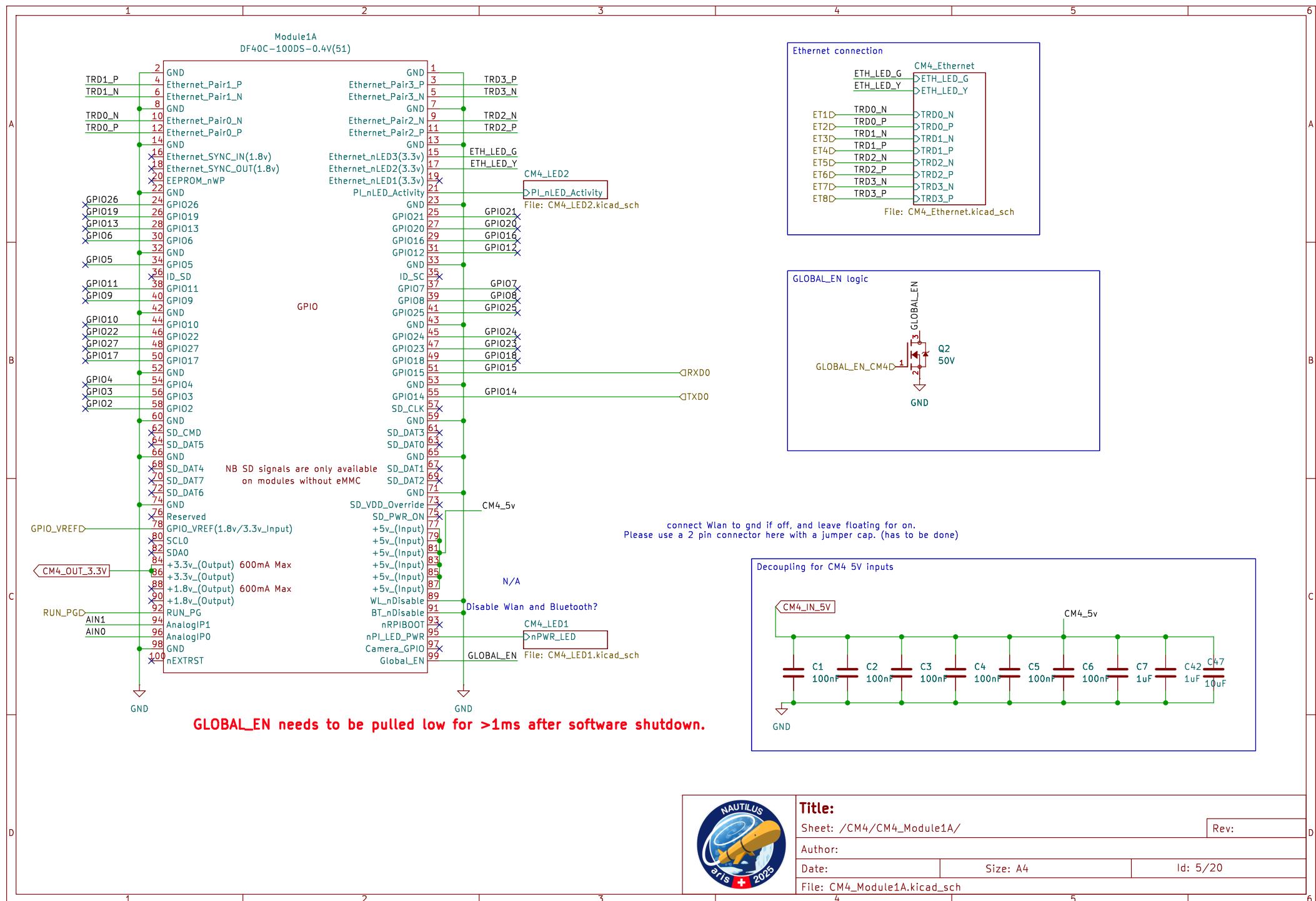
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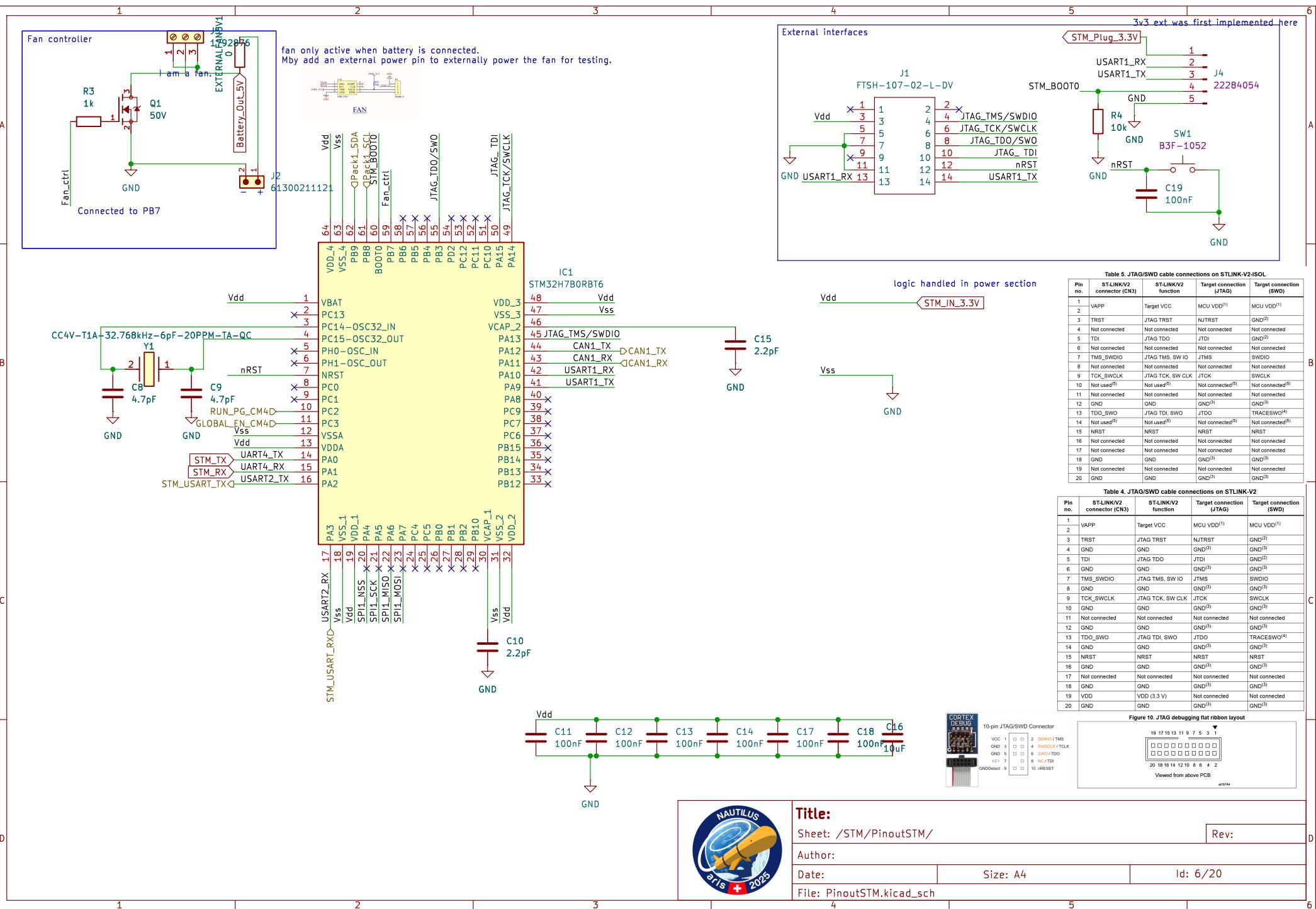
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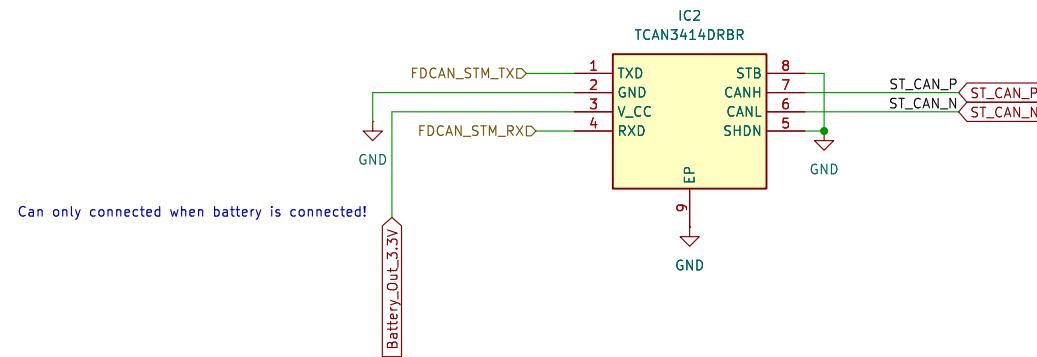
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**Title:**

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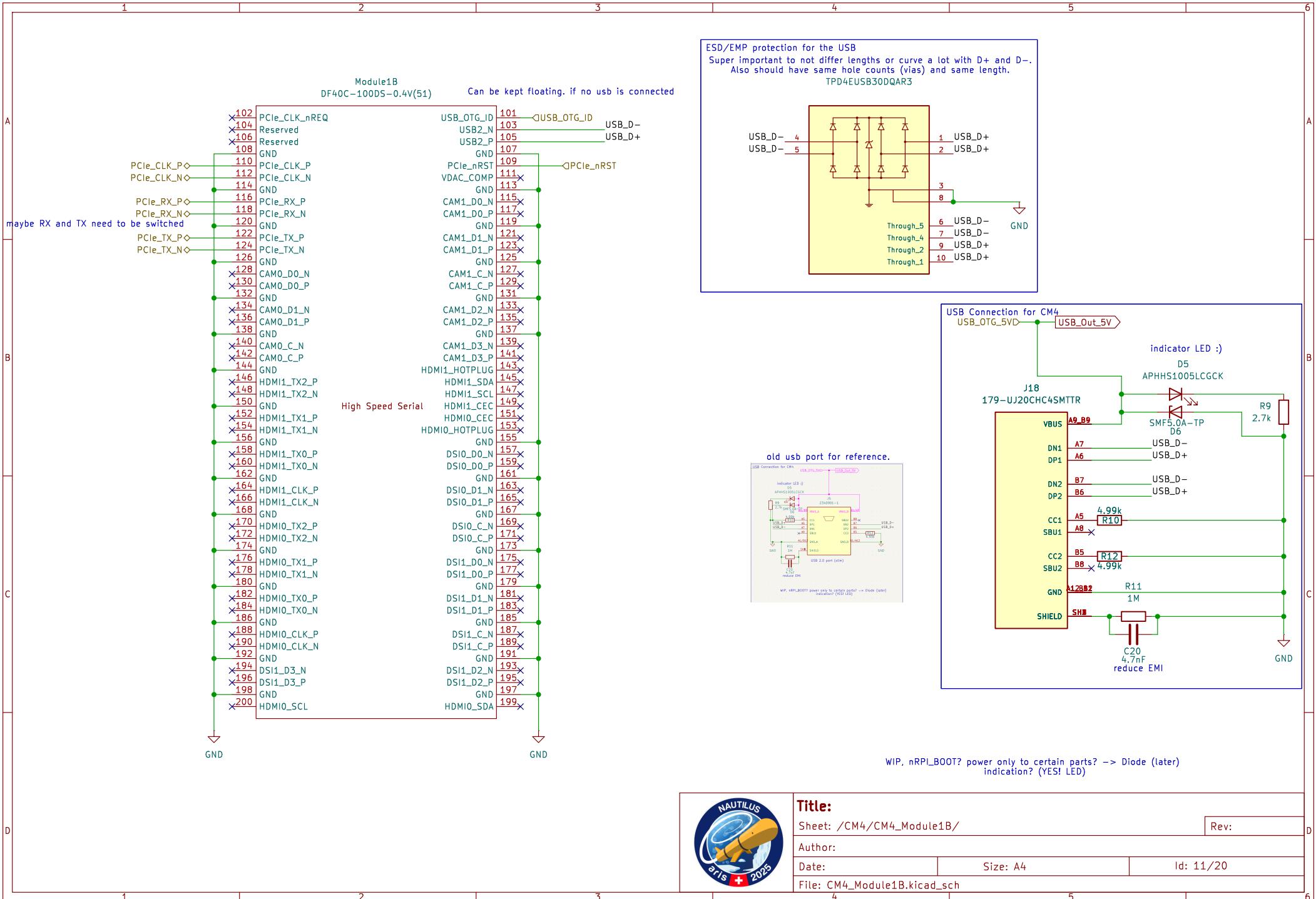
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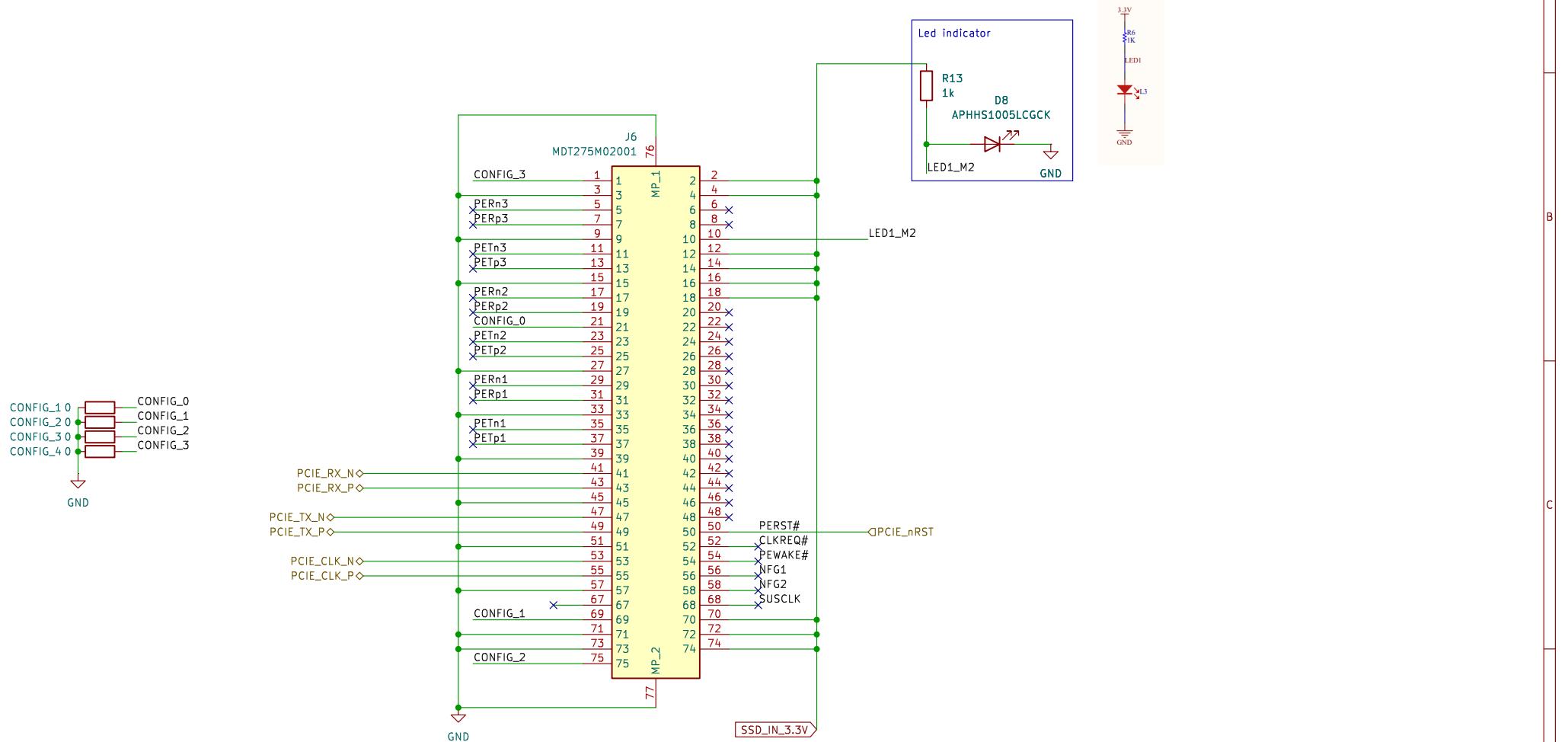
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Sheet: /CM4/PCIE Interface/

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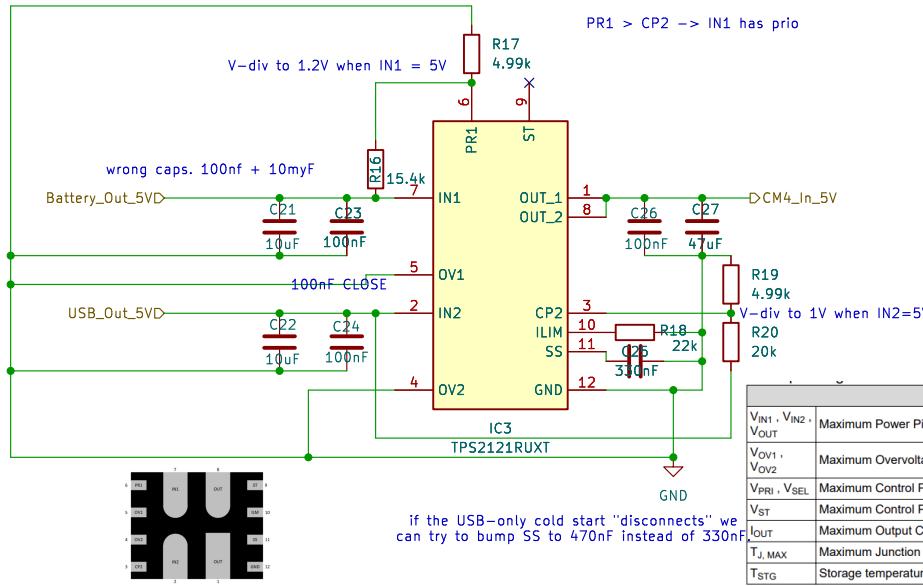
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A

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for questions about wiring etc please consult the datasheet..
<https://www.ti.com/lit/ds/symlink/tps2120.pdf?ts=1761678178328>



	Pins	MIN	MAX	UNIT
V _{IN1} , V _{IN2} , V _{OUT}	IN1, IN2, OUT	-0.3	24	V
V _{OV1} , V _{OV2}	OV1, OV2	-0.3	6	V
V _{PRI} , V _{SEL}	PRI, SEL	-0.3	6	V
V _{ST}	ST	-0.3	6	V
I _{OUT}	OUT			Internally Limited
T _{J, MAX}				Internally Limited
T _{STG}		-65	150	°C

Pin Functions		
NAME	TPS2120	TPS2121
V _{IN1}	B1, B2, C1	1 Power Input for Source 1
V _{IN2}	B3, B4, C4	2 Power Input for Source 2
OUT	C2, C3, D1, D2	1, 8 Power Output
GND	D3, D4	— Ground
ST	E1	9 O Status output indicating which channel is selected. Connect to GND if not required.
ILIM	E2	10 O Output Current Limiting for both channels.
SS	E3	11 O Adjusts Input Setting Delay Time and Output Soft Start Time
SEL	E4	12 —
PR1	A1	6 I Enables Priority Operation. Connect to IN1 to set switchover voltage. Connect to GND if not required.
OV1	A2	5 I Active Low Enable Supervisor for IN1 Overvoltage Protection. Connect to GND if not required.
OV2	A3	4 I Active Low Enable Supervisor for IN2 Overvoltage Protection. Connect to GND if not required.
CP2	A4	— I Active Low Enable for IN1. Allows GPIO to override priority operation and manually select IN2. TPS2120 only.



Title:

Sheet: /Power_logic/5V_Logic/

Rev:

Author:

Date:

Size: A4

Id: 15/20

File: 5V_Logic.kicad_sch

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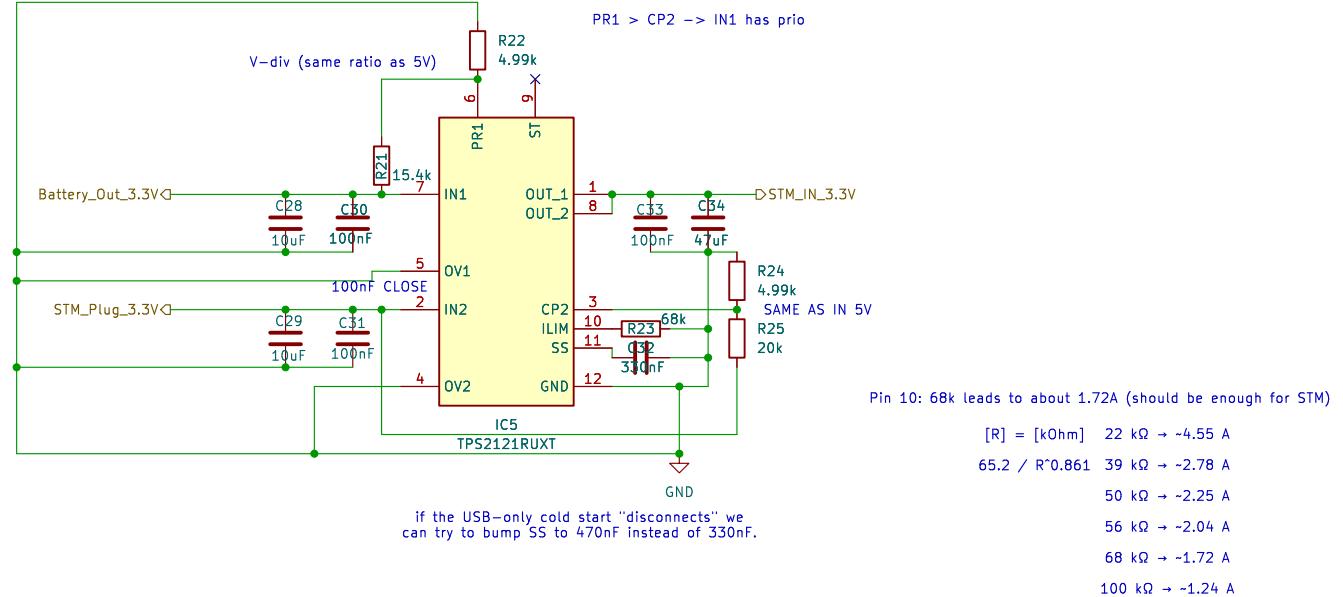
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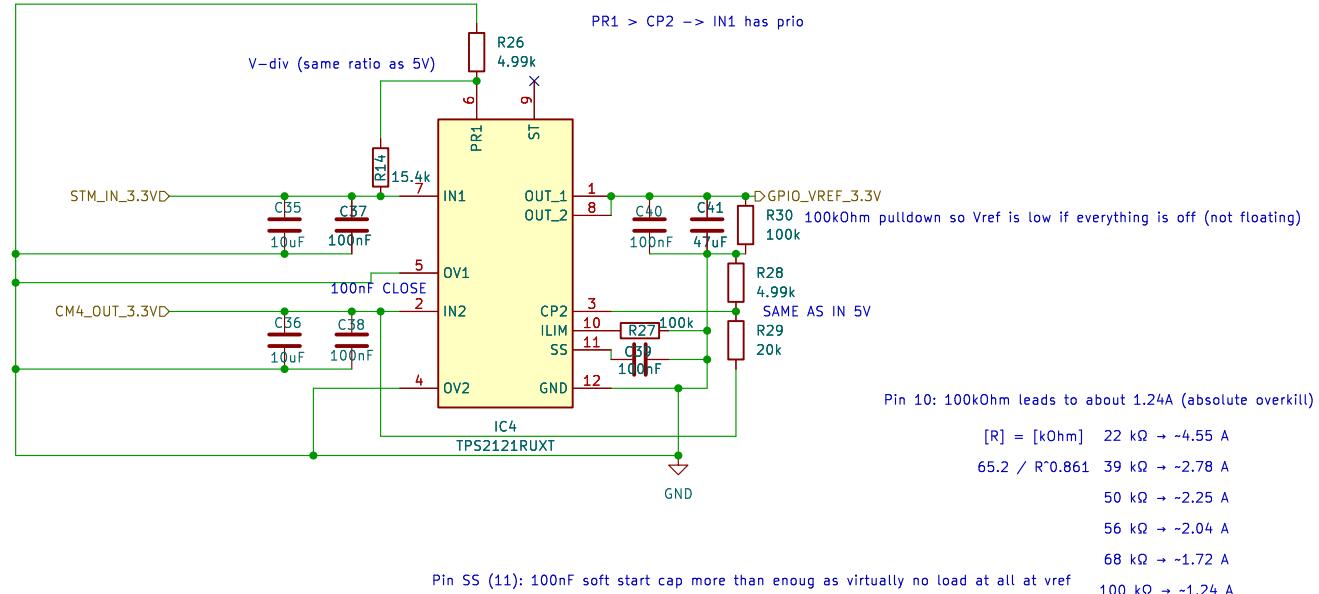
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Title

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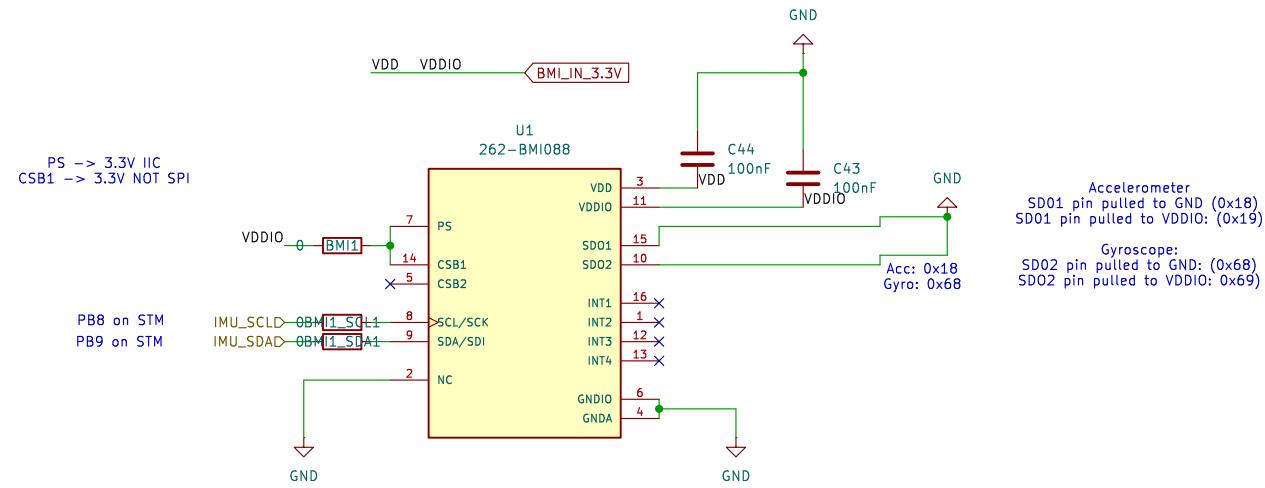
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Title

Sheet: /IMU/IMU1/

Author:

Date:

File: IMU1.kicad_sch

Rev:

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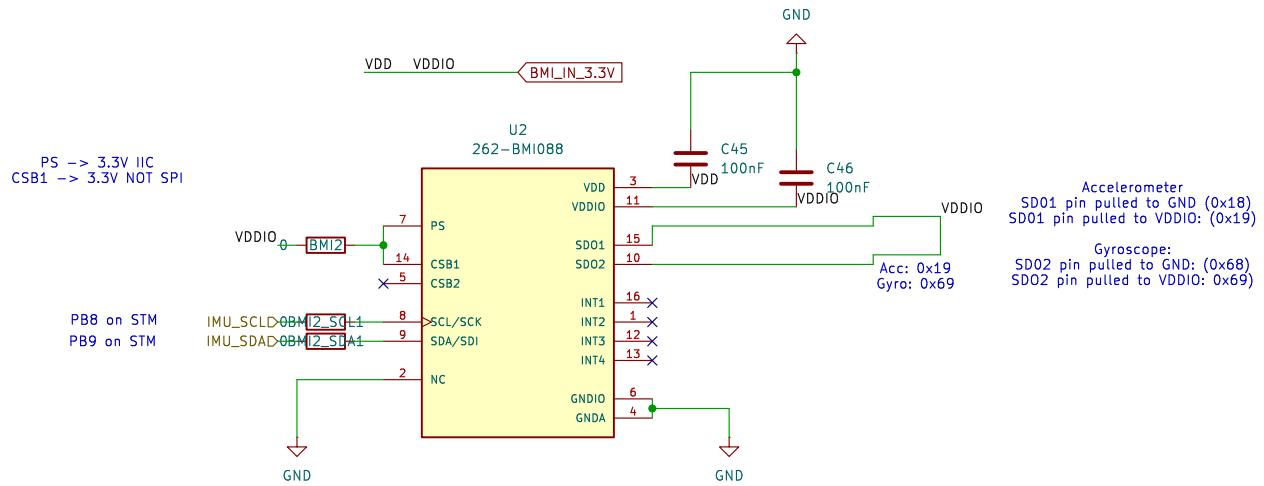
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Sheet: /IMU/IMU2/

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Author:

Date:

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Id: 20/20

File: IMU2.kicad_sch

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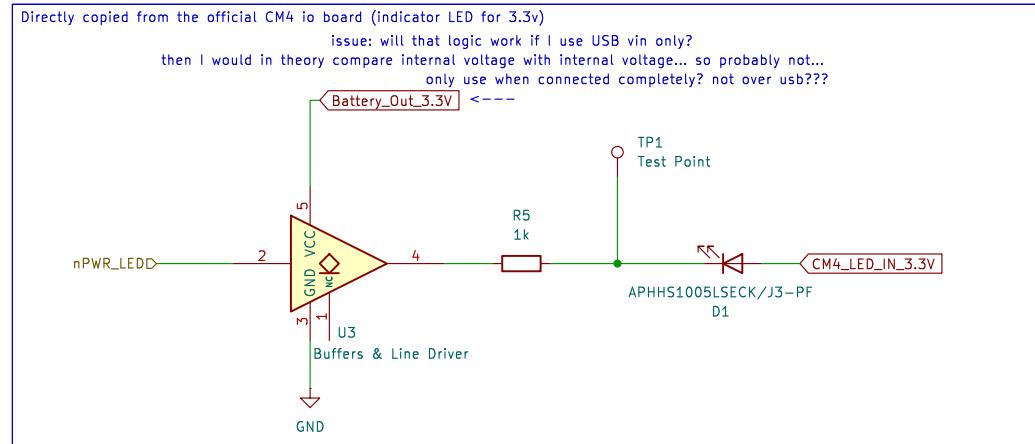
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Author:

Date:

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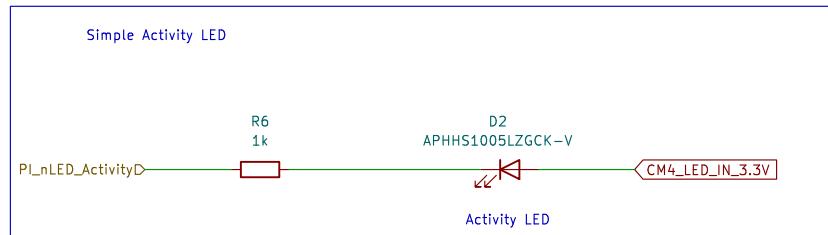
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Rev:

Author:

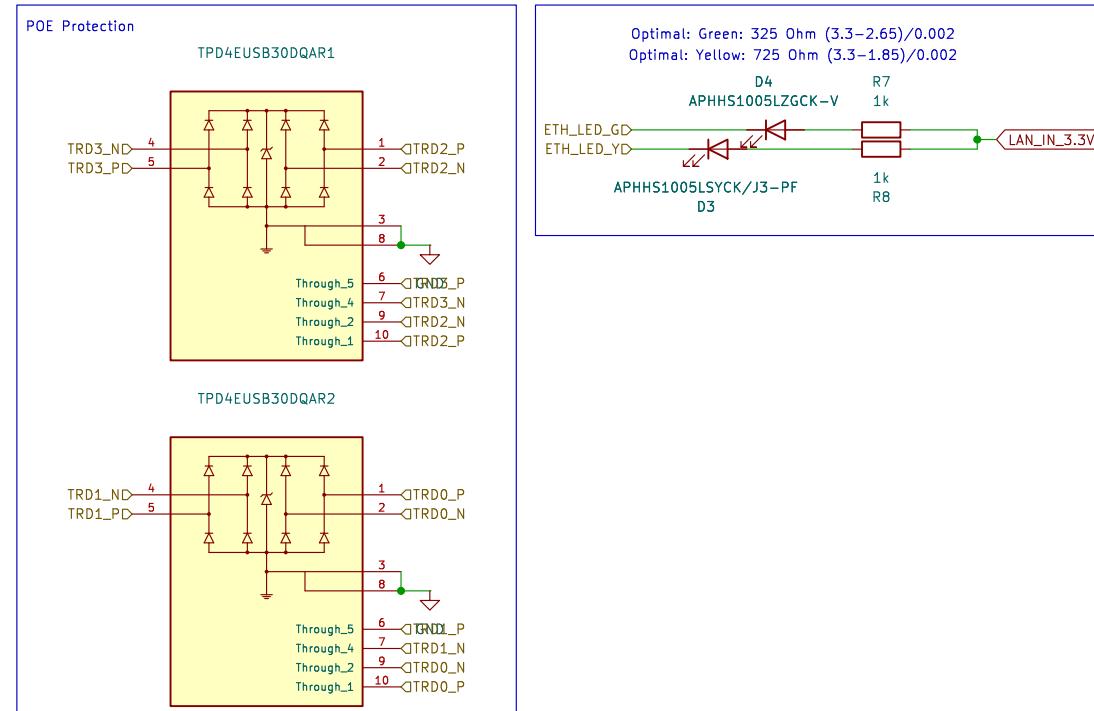
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1 2 3 4 5 6

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Rev:

Author:

Date:

Size: A4

Id: 10/20

File: CM4_Ethernet.kicad_sch