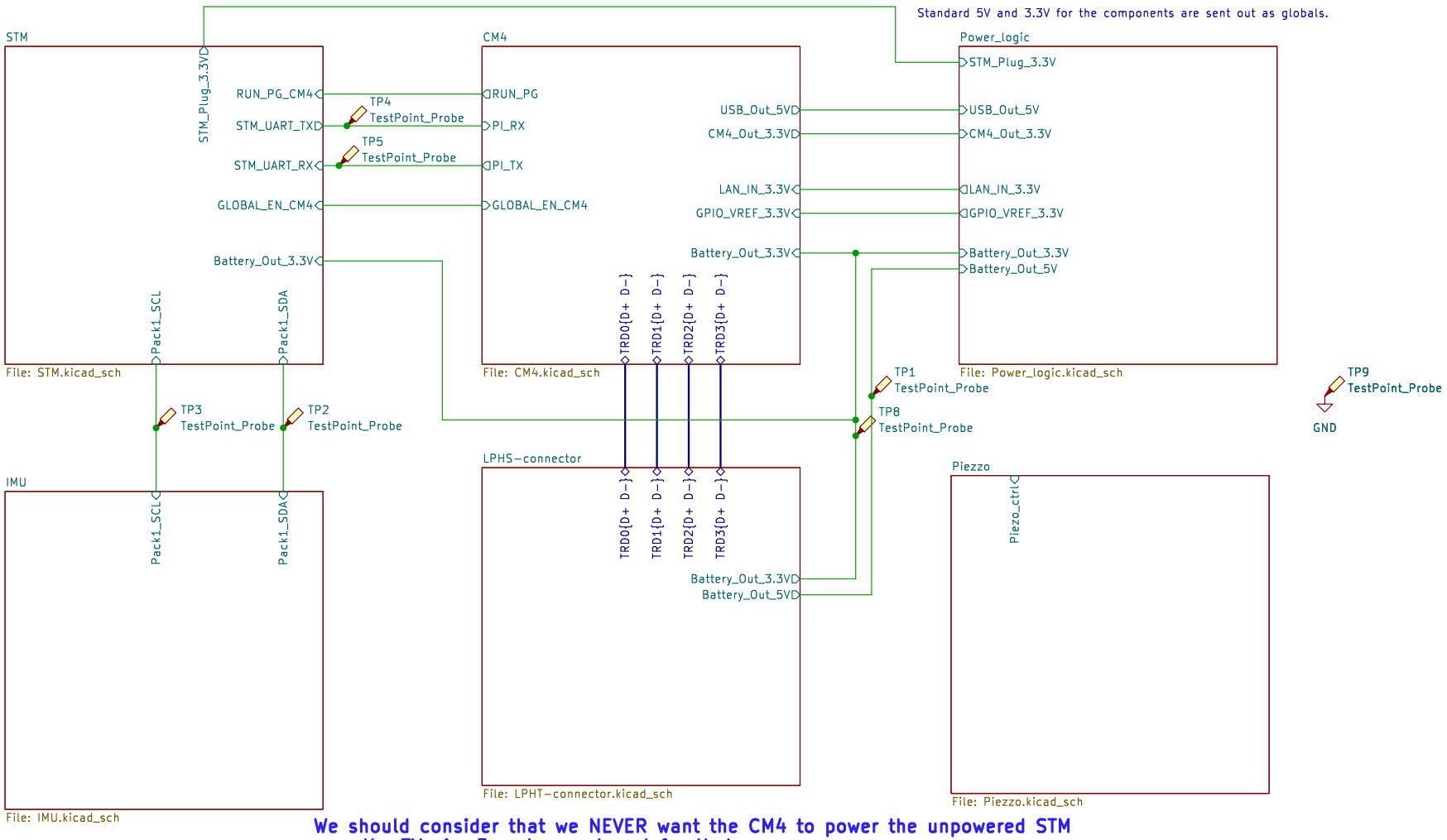


We should consider that we NEVER want the CM4 to power the unpowered STM over the TX pin. Found a neat part for that: https://www.mouser.ch/ProductDetail/Texas-Instruments/SN74LVC1G126DBVR?qs=pajglaoyDUi3T2WgNNfd3w%3D%3D

connections:
Pin 5: VCC -> CM4_3V3

Pin 2: A -> CM4 TX (PLTX)

Pin 4: Y -> STM_UART_RX

Pin 1: OE -> STM_IN_3.3V

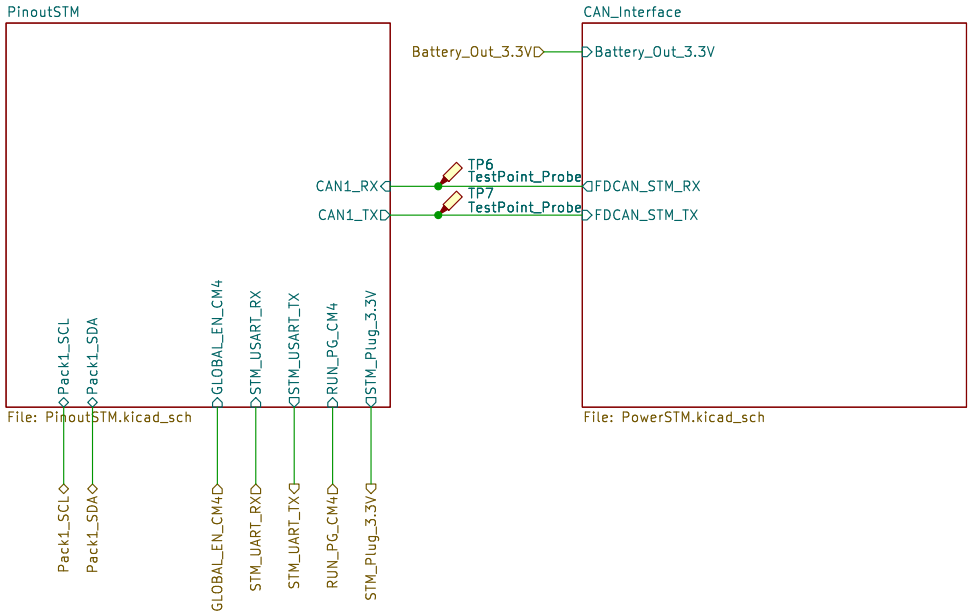
Pin 3: GND

0.1uF decoupling cap VCC-GND

220 Ohm series at Y (to STM). (current limiting)

Title:

Sheet: /		Rev:
Author:		
Date:	Size: A4	Id: 1/20
File: nautilus_mainboard.kicad_sch		



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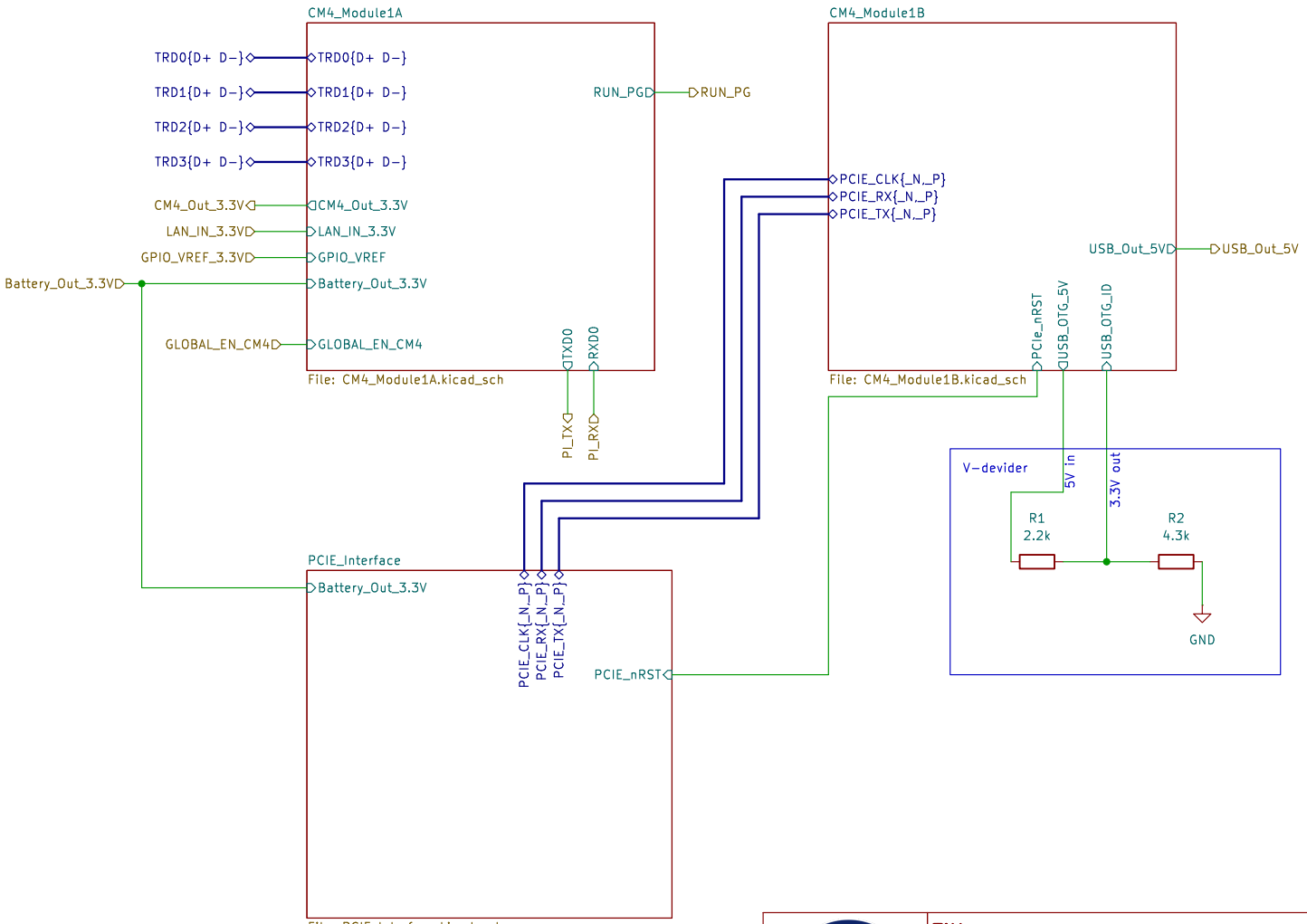
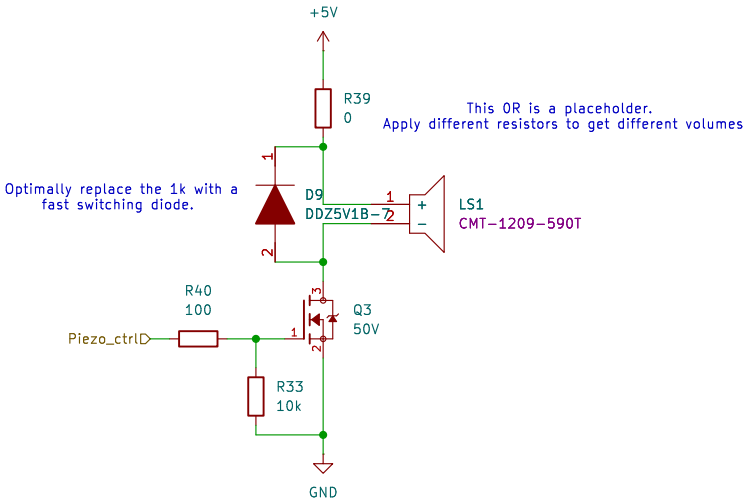
Sheet: /STM/		Rev:
Author:		
Date:	Size: A4	Id: 2/20
File: STM.kicad_sch		



Title:		
Sheet: /CM4/		Rev:
Author:		
Date:	Size: A4	Id: 3/20
File: CM4.kicad_sch		

Not in the PCB yet as we dont know if we actually need it.



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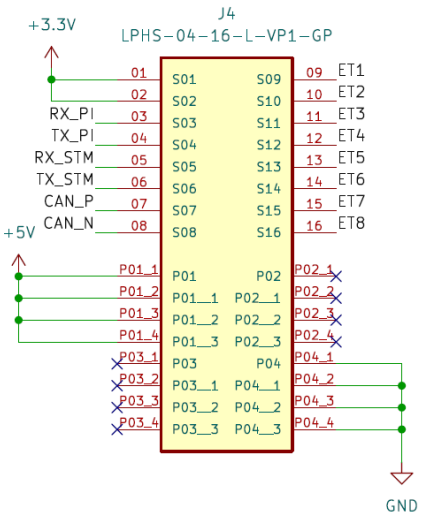
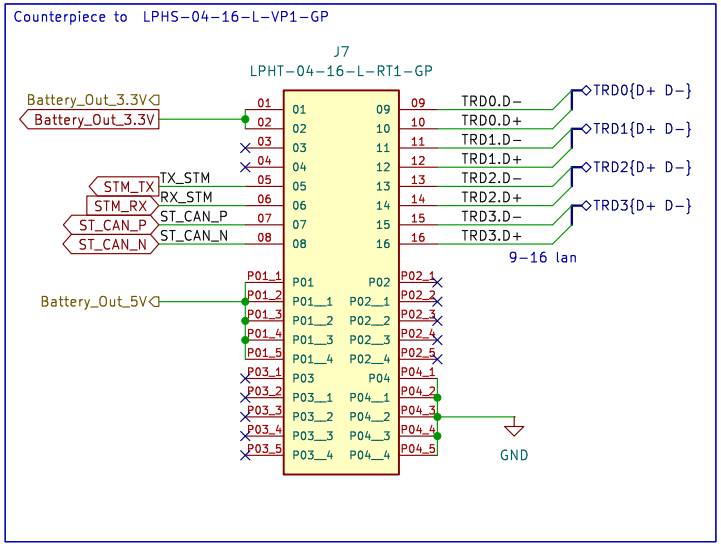
Sheet: /Piezzo/		Rev:
Author:		
Date:	Size: A4	Id: 4/20
File: Piezzo.kicad_sch		

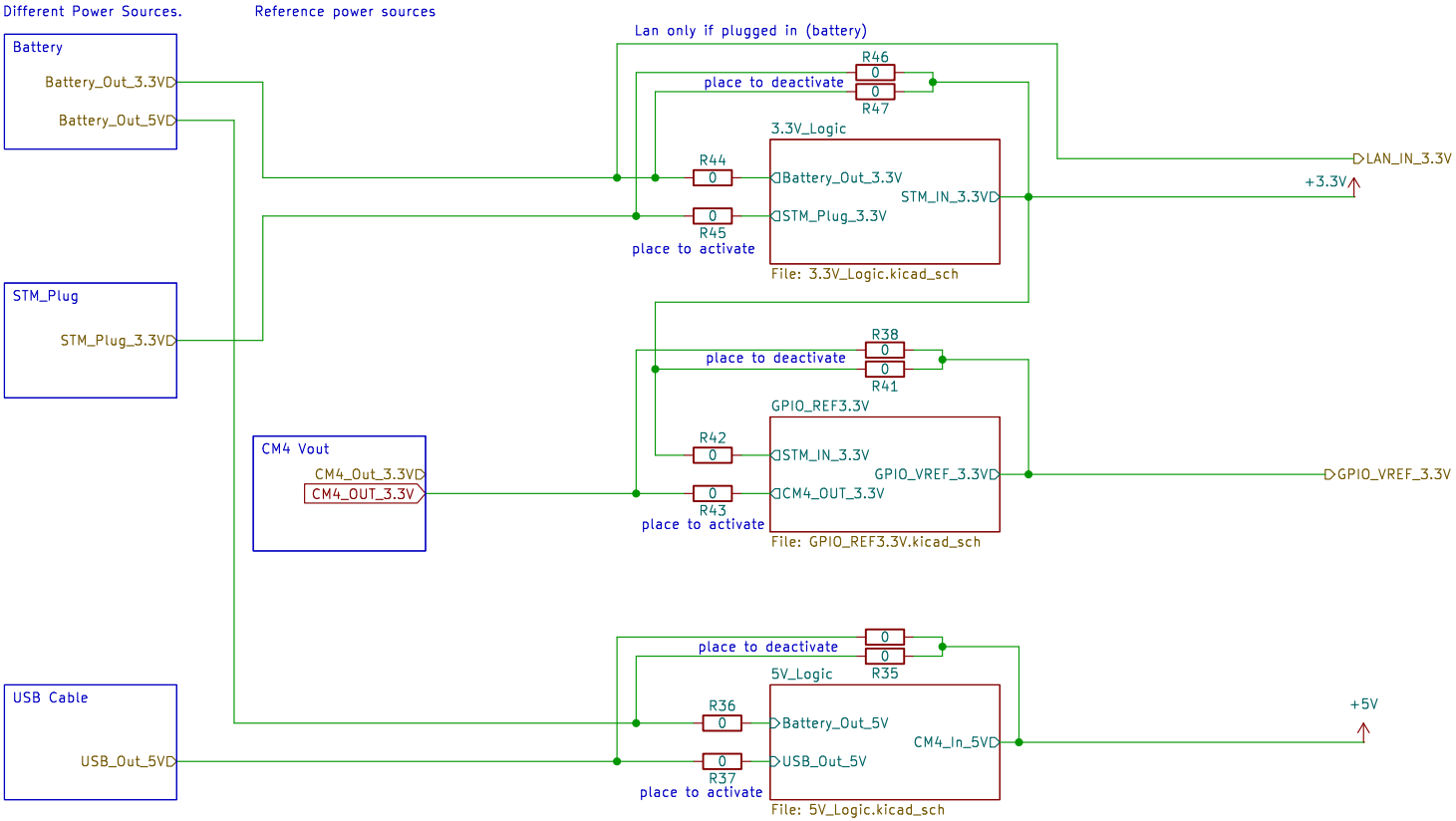
Mainboard



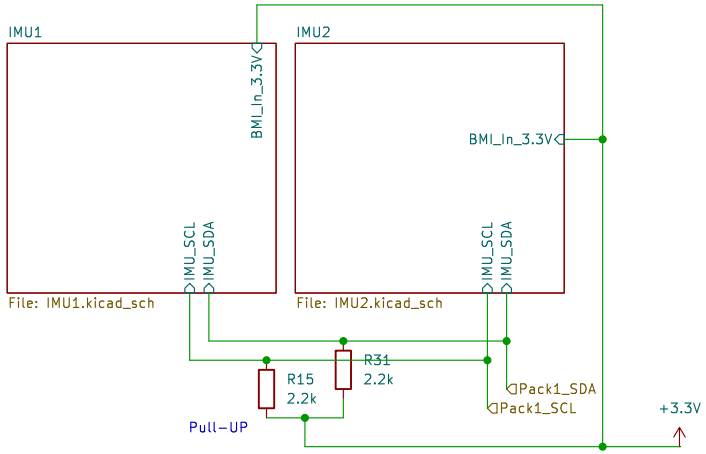


Title:		
Sheet: /LPHS-connector/		Rev:
Author:		
Date:	Size: A4	Id: 14/20
File: LPHT-connector.kicad_sch		

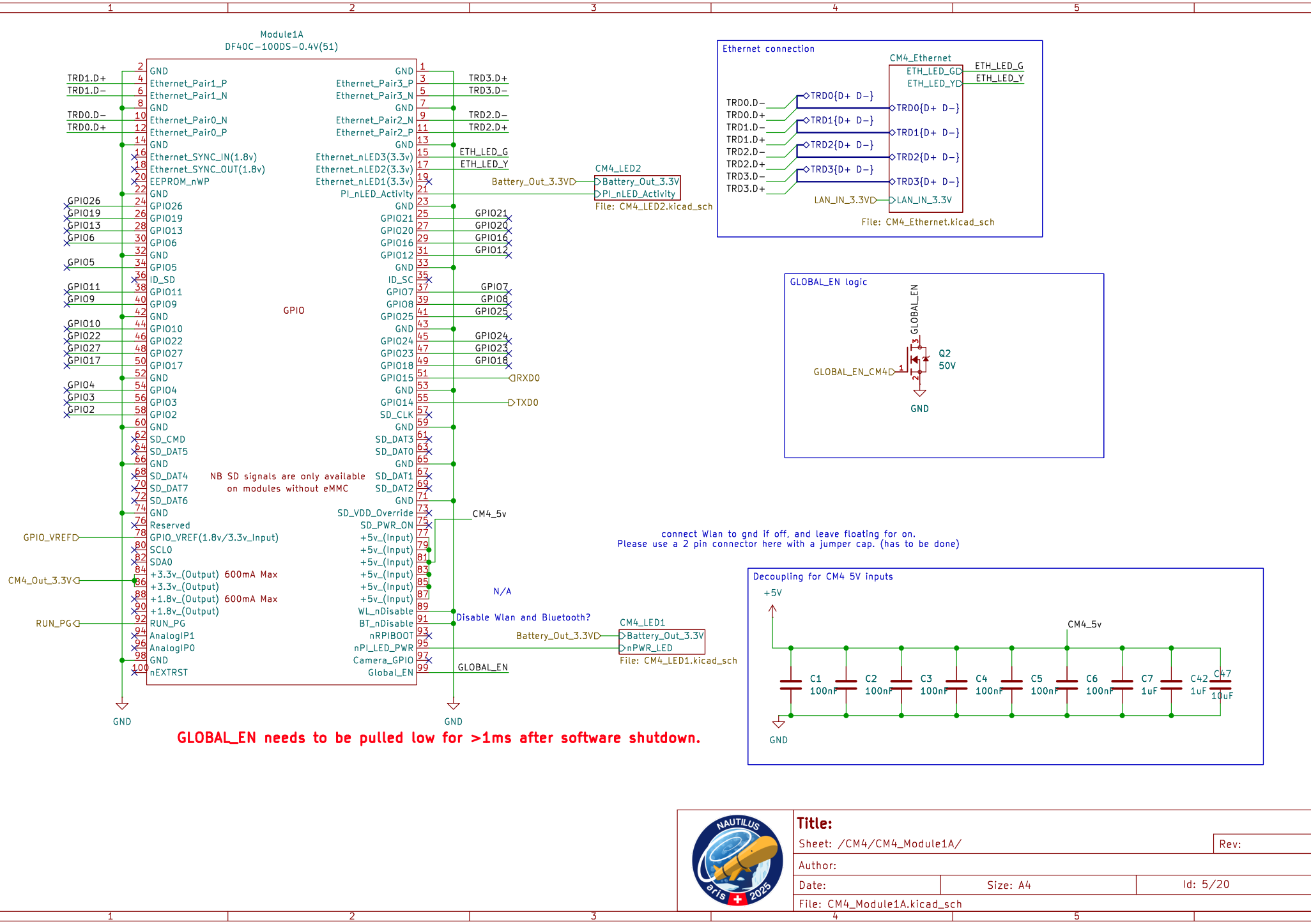
some rules:
USB wont power the STM32.
STM_Plug wont power the CM4
The GPIO_VREF of the CM4 needs to be STM32's 3.3V
The Lan Vin is only powered when running on Battery
Battery preferrably powers everything.
Whenever the CM4 runs, also run the LED signals AND the SSD voltage. all "core" tasks tied to the CM4.



Title:		
Sheet: /Power_logic/		Rev:
Author: dcarocci		
Date: 2025-11-18	Size: A4	Id: 14/20
File: Power_logic.kicad_sch		



Title:		
Sheet: /IMU/		Rev:
Author:		
Date:	Size: A4	Id: 18/20
File: IMU.kicad_sch		


Module1A
DF40C-100DS-0.4V(51)
GPIO
NB SD signals are only available on modules without eMMC
Ethernet connection
CM4_Ethernet
File: CM4_Ethernet.kicad_sch
CM4_LED2
File: CM4_LED2.kicad_sch
GLOBAL_EN logic
Q2
50V
connect Wlan to gnd if off, and leave floating for on.
Please use a 2 pin connector here with a jumper cap. (has to be done)
Disable Wlan and Bluetooth?
CM4_LED1
File: CM4_LED1.kicad_sch
Decoupling for CM4 5V inputs
GLOBAL_EN needs to be pulled low for >1ms after software shutdown.
Title:
Sheet: /CM4/CM4_Module1A/
Rev:
Author:
Date:
Size: A4
Id: 5/20
File: CM4_Module1A.kicad_sch

EXTERNALFAN5V1

Fan controller

J5
1792876

I am a fan.

R3
1k

Q1
50V

+5V

GND

Fan_ctrl

Connected to PB7

J2
61300211121

fan only active when battery is connected.
Mby add an external power pin to externally power the fan for testing.

FAN

3v3 ext was first implemented here

External interfaces

J1
FTSH-107-02-L-DV

Vdd
GND
USART1_RX
JTAG_TMS/SWDIO
JTAG_TCK/SWCLK
JTAG_TDO/SWO
JTAG_ TDI
nRST
USART1_TX

STM_Plug_3.3V
USART1_RX
USART1_TX
STM_BOOT0
GND

J4
22284054

R4
10k

SW1
B3F-1052

nRST
C19
100nF

IC1
STM32H7B0RBT6

Vdd
Vss
Pack1_SDA
Pack1_SCL
STM_BOOT0
Fan_ctrl
JTAG_TDO/SWO
JTAG_ TDI
JTAG_TCK/SWCLK

VBAT
PC13
PC14-OSC32_IN
PC15-OSC32_OUT
PH0-OSC_IN
PH1-OSC_OUT
NRST
PC0
PC1
PC2
PC3
VSSA
VDDA
PA0
PA1
PA2

VDD_3
VSS_3
VCAP_2
PA13
PA12
PA11
PA10
PA9
PA8
PC9
PC7
PC6
PB15
PB14
PB13
PB12

PA3
VSS_1
VDD_1
PA4
PA5
PA6
PA7
PC4
PC5
PB0
PB1
PB2
PB10
VCAP_1
VSS_2
VDD_2

CC4V-T1A-32.768kHz-6pF-20PPM-TA-QC
Y1
C8
4.7pF
C9
4.7pF
C15
2.2pF
C10
2.2pF

nRST
RUN_PG_CM4
GLOBAL_EN_CM4
Vss
Vdd

must be hirarchical lable RX,TX
STM_TX
STM_RX
STM_USART_TX
UART4_TX
UART4_RX
USART2_TX

CAN1_TX
CAN1_RX
USART1_RX
USART1_TX

USART2_RX
SPI1_NSS
SPI1_SCK
SPI1_MISO
SPI1_MOSI

+3.3V
logic handled in power section

C11 100nF
C12 100nF
C13 100nF
C14 100nF
C17 100nF
C18 100nF
C16 10uF

STDC14 for STLINK-V3MINI (STM32 JTAG/SWD and VCP)

Figure 11. CN5 STDC14 connector (Top view)

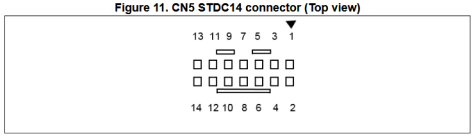


Table 4. CN5 STDC14 connector pinout

STDC14 Pin #	ARM10 Pin #	Pin description	Type
1	-	Reserved(1)	-
2	-	Reserved(1)	-
3	1	T_VCC(2)	I
4	2	T_JTMS/T_SWDIO	I/O
5	3	GND	S
6	4	T_JCLK/T_SWCLK	O
7	5	GND	S
8	6	T_JTDO/T_SWO(3)	I
9	7	T_JCLK	O
10	8	T_JTDI/NC(4)	O
11	9	GNDDetect	O
12	10	T_NRST	O
13	-	T_VCP_RX	O
14	-	T_VCP_TX	I

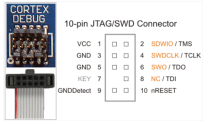
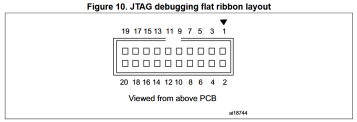


Figure 10. JTAG debugging flat ribbon layout



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Sheet: /STM/PinoutSTM/

Rev:

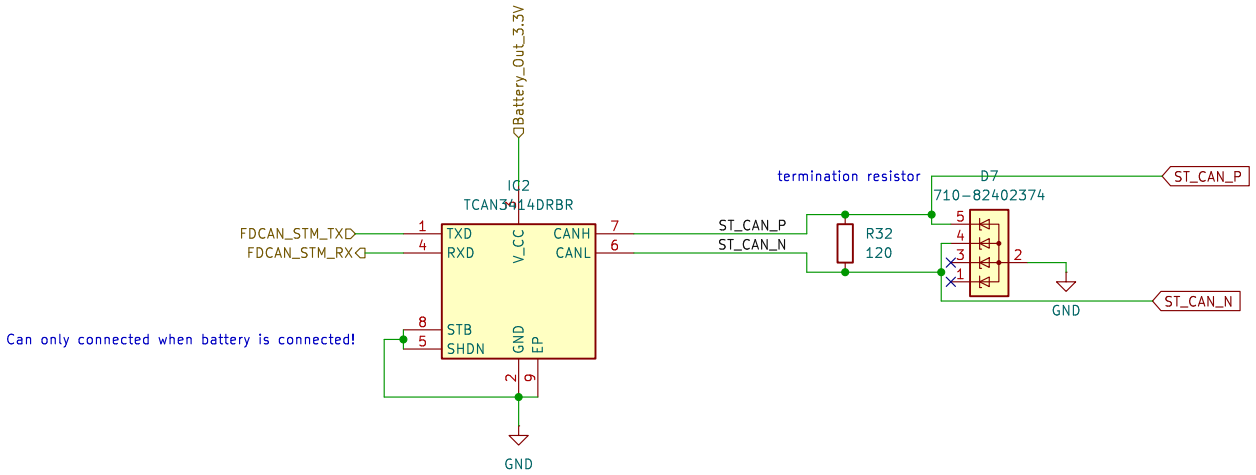
Author:

Date:

Size: A4

Id: 6/20

File: PinoutSTM.kicad_sch



Title:		
Sheet: /STM/CAN_Interface/		Rev:
Author:		
Date:	Size: A4	Id: 7/20
File: PowerSTM.kicad_sch		

Module1B
DF40C-100DS-0.4V(51)

Can be kept floating. if no usb is connected

PCIE_CLK{_N,_P}
PCIE_CLK._P
PCIE_CLK._N
PCIE_RX{_N,_P}
PCIE_RX._P
PCIE_RX._N
PCIE_TX{_N,_P}
PCIE_TX._P
PCIE_TX._N

maybe RX and TX need to be switched

102	PCIe_CLK_nREQ	USB_OTG_ID	101
104	Reserved	USB2_N	103
106	Reserved	USB2_P	105
108	GND	GND	107
110	PCIe_CLK_P	PCIe_nRST	109
112	PCIe_CLK_N	VDAC_COMP	111
114	GND	GND	113
116	PCIe_RX_P	CAM1_D0_N	115
118	PCIe_RX_N	CAM1_D0_P	117
120	GND	GND	119
122	PCIe_TX_P	CAM1_D1_N	121
124	PCIe_TX_N	CAM1_D1_P	123
126	GND	GND	125
128	CAM0_D0_N	CAM1_C_N	127
130	CAM0_D0_P	CAM1_C_P	129
132	GND	GND	131
134	CAM0_D1_N	CAM1_D2_N	133
136	CAM0_D1_P	CAM1_D2_P	135
138	GND	GND	137
140	CAM0_C_N	CAM1_D3_N	139
142	CAM0_C_P	CAM1_D3_P	141
144	GND	HDMI1_HOTPLUG	143
146	HDMI1_TX2_P	HDMI1_SDA	145
148	HDMI1_TX2_N	HDMI1_SCL	147
150	GND	HDMI1_CEC	149
152	HDMI1_TX1_P	HDMI0_CEC	151
154	HDMI1_TX1_N	HDMI0_HOTPLUG	153
156	GND	GND	155
158	HDMI1_TX0_P	DSI0_D0_N	157
160	HDMI1_TX0_N	DSI0_D0_P	159
162	GND	GND	161
164	HDMI1_CLK_P	DSI0_D1_N	163
166	HDMI1_CLK_N	DSI0_D1_P	165
168	GND	GND	167
170	HDMI0_TX2_P	DSI0_C_N	169
172	HDMI0_TX2_N	DSI0_C_P	171
174	GND	GND	173
176	HDMI0_TX1_P	DSI1_D0_N	175
178	HDMI0_TX1_N	DSI1_D0_P	177
180	GND	GND	179
182	HDMI0_TX0_P	DSI1_D1_N	181
184	HDMI0_TX0_N	DSI1_D1_P	183
186	GND	GND	185
188	HDMI0_CLK_P	DSI1_C_N	187
190	HDMI0_CLK_N	DSI1_C_P	189
192	GND	GND	191
194	DSI1_D3_N	DSI1_D2_N	193
196	DSI1_D3_P	DSI1_D2_P	195
198	GND	GND	197
200	HDMI0_SCL	HDMI0_SDA	199

High Speed Serial

USB_OTG_ID
USB_D-
USB_D+
PCIe_nRST

GND
GND

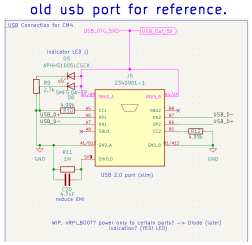
ESD/EMP protection for the USB

Super important to not differ lengths or curve a lot with D+ and D-.
Also should have same hole counts (vias) and same length.

TPD4EUSB30DQAR3

USB_D- 4
USB_D- 5
1 USB_D+
2 USB_D+
3
8
GND
Through_5 6 USB_D-
Through_4 7 USB_D-
Through_2 9 USB_D+
Through_1 10 USB_D+

old usb port for reference.



USB Connection for CM4

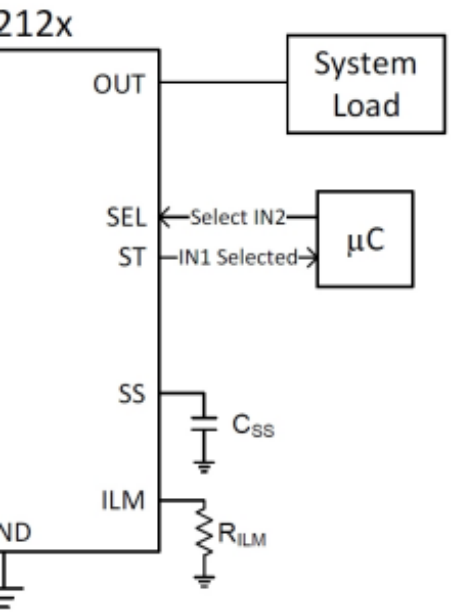
J3
179-UJ20CHC4SMTTR

USB_OTG_5V
USB_Out_5V
D5 APHHS1005LCGCK
R9 2.7k
SMF5.0A-TP
D6
GND

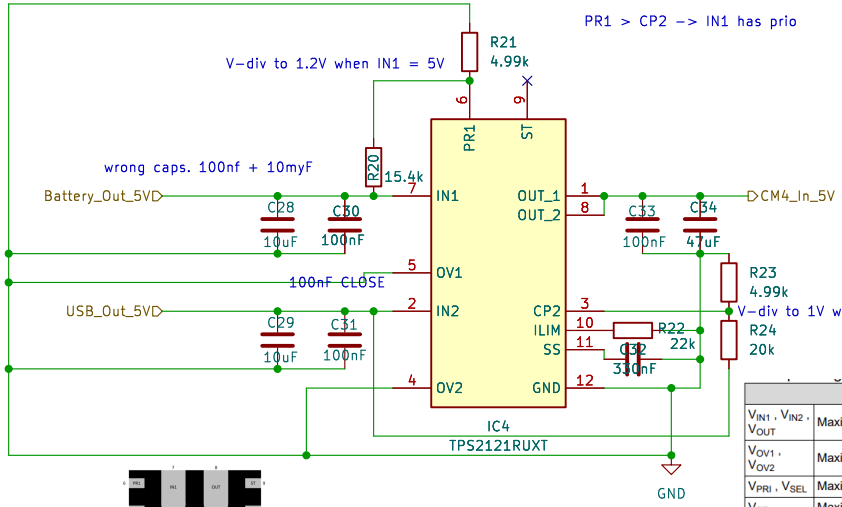
A9_B4
A4_B9
VBUS
VBUS
DN1 A7 USB_D-
DP1 A6 USB_D+
DN2 B7 USB_D-
DP2 B6 USB_D+
CC1 A5 4.99k R10
SBU1 A8
CC2 B5 R12 4.99k
SBU2 B8
GND
GND
SHIELD
SHIELD
SHIELD
SHIELD
A12_B1
B12_A1
SH1
SH2
SH3
SH4
R11 1M
C20 4.7nF
GND
GND

WIP, nRPI_BOOT? power only to certain parts? -> Diode (later)
indication? (YES! LED)

Title:		
Sheet: /CM4/CM4_Module1B/		Rev:
Author:		
Date:	Size: A4	Id: 11/20
File: CM4_Module1B.kicad_sch		



for questions about wiring etc please consult the datasheet...
https://www.ti.com/lit/ds/symlink/tps2120.pdf?ts=1761678178328



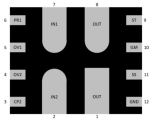


Figure 6-2. TPS2121 (RUX) Package 12-Pin VQFN-HR Bottom View

	Pins	MIN	MAX	UNIT
V_{IN1} , V_{IN2} , V_{OUT}	Maximum Power Pin Voltage	IN1, IN2, OUT	-0.3	24	V
V_{OV1} , V_{OV2}	Maximum Overvoltage Pin Voltage	OV1, OV2	-0.3	6	V
V_{PRI} , V_{SEL}	Maximum Control Pin Voltage	PRI, SEL	-0.3	6	V
V_{ST}	Maximum Control Pin Voltage	ST	-0.3	6	V
I_{OUT}	Maximum Output Current	OUT	Internally Limited		
$T_{J, MAX}$	Maximum Junction Temperature		Internally Limited		
T_{STG}	Storage temperature		-65	150	°C

Pin Functions

PIN			I/O	DESCRIPTION
NAME	TPS2120 WCSP	TPS2121 VQFN-HR		
IN1	B1, B2, C1	7	I	Power Input for Source 1
IN2	B3, B4, C4	2	I	Power Input for Source 2
OUT	C2, C3, D1, D2, D3, D4	1, 8	I	Power Output
ST	E1	9	O	Status output indicating which channel is selected. Connect to GND if not required.
ILIM	E2	10	O	Output Current Limiting for both channels.
SS	E3	11	O	Adjusts Input Setting Delay Time and Output Soft Start Time
GND	E4	12	—	Device Ground
PR1	A1	6	I	Enables Priority Operation. Connect to IN1 to set switchover voltage. Connect to GND if not required.
OV1	A2	5	I	Active Low Enable Supervisor for IN1 Overvoltage Protection. Connect to GND if not required.
OV2	A3	4	I	Active Low Enable Supervisor for IN2 Overvoltage Protection. Connect to GND if not required.
SEL	A4	—	I	Active low Enable for IN1. Allows GPIO to override priority operation and manually select IN2. TPS2120 only.
CP2	—	3	I	Enables Comparator Operation and is compared to PR1 to set switchover voltage. Connect to GND if not required. TPS2121 only.

Title:
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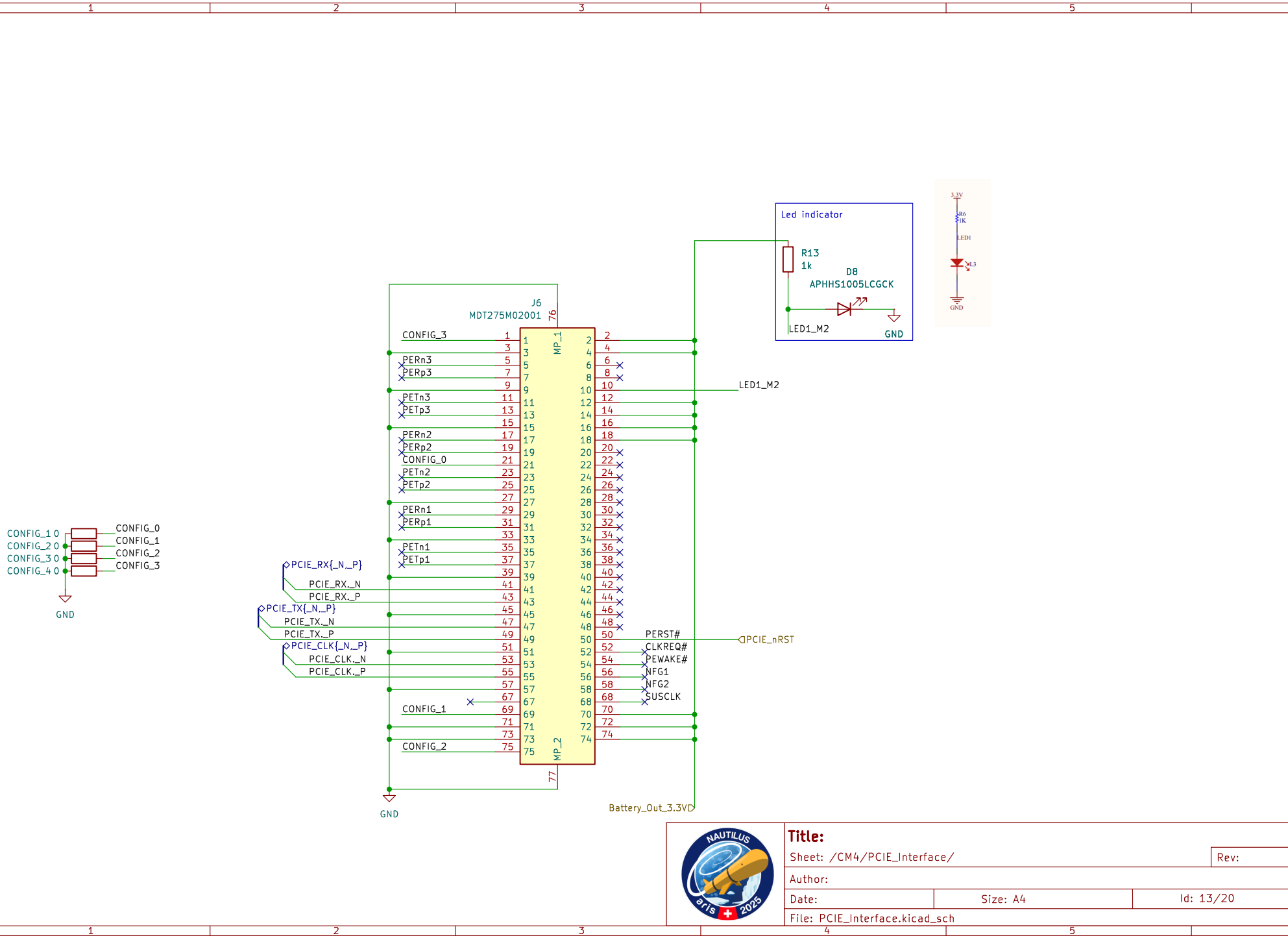
Rev:
Author:
Date:
Size: A4
Id: 12/20
File: 5V_Logic.kicad_sch



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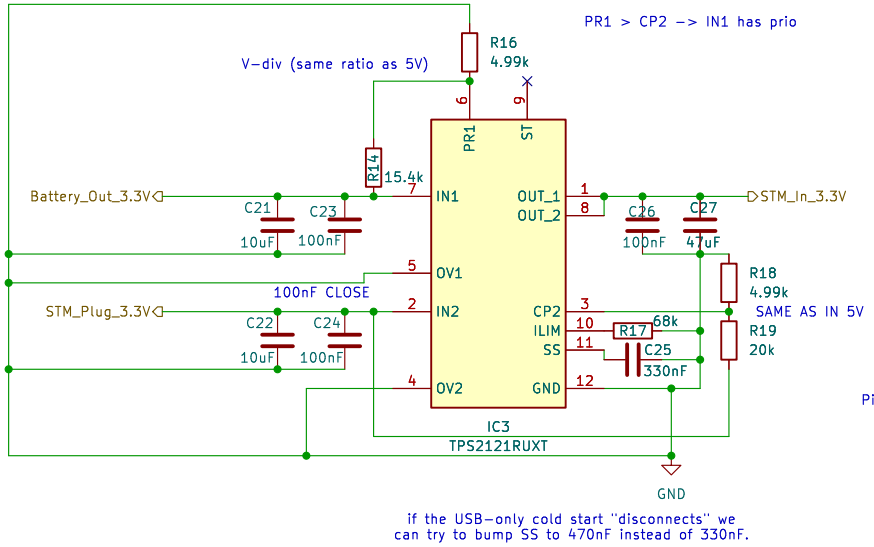
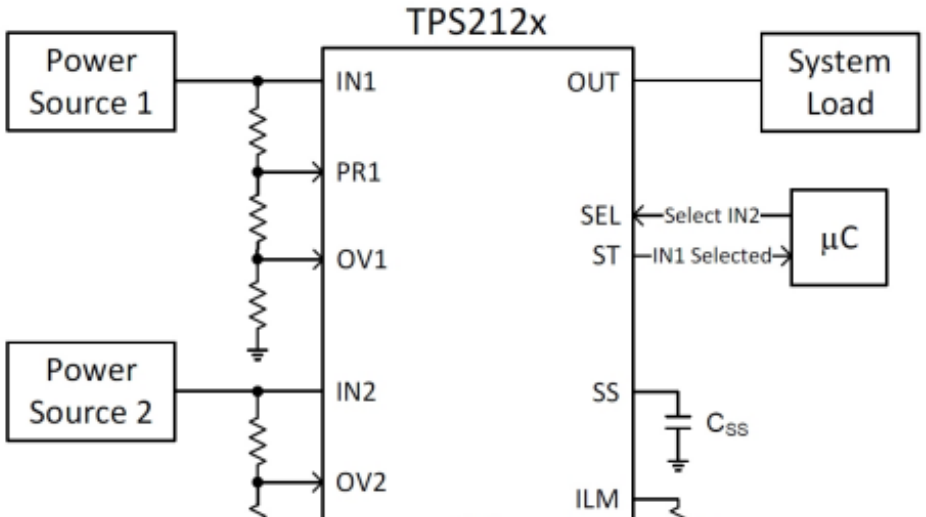
Sheet: /CM4/PCIE_Interface/		Rev:
Author:		
Date:	Size: A4	Id: 13/20
File: PCIE_Interface.kicad_sch		



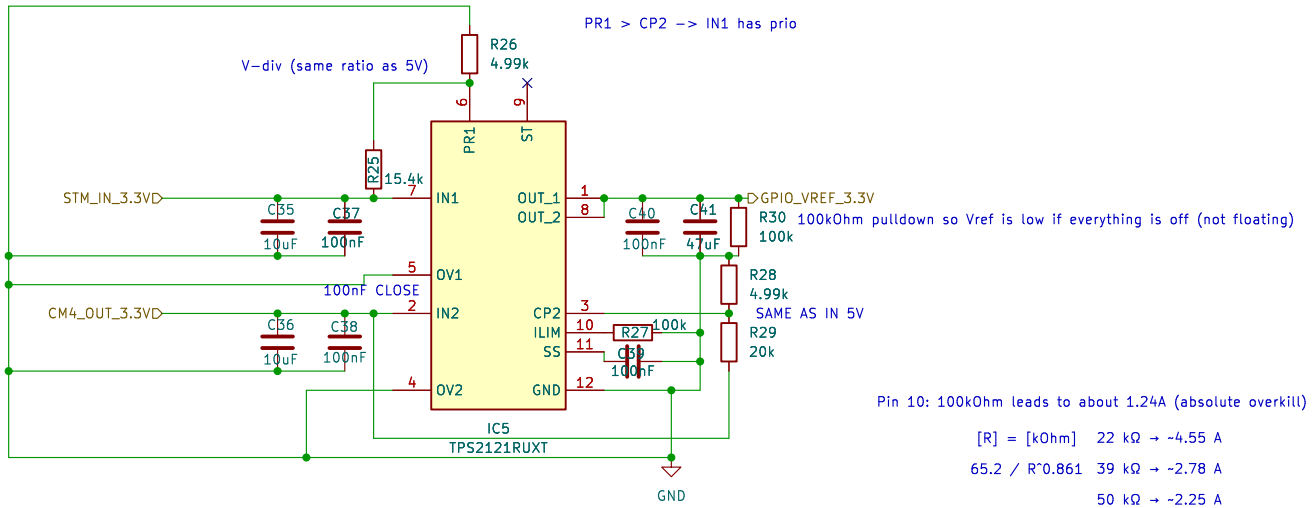
Pin 10: 68k leads to about 1.72A (should be enough for STM)

[R] = [kOhm]	22 kΩ → ~4.55 A
65.2 / R^0.861	39 kΩ → ~2.78 A
	50 kΩ → ~2.25 A
	56 kΩ → ~2.04 A
	68 kΩ → ~1.72 A
	100 kΩ → ~1.24 A



_Logic/ | Rev:

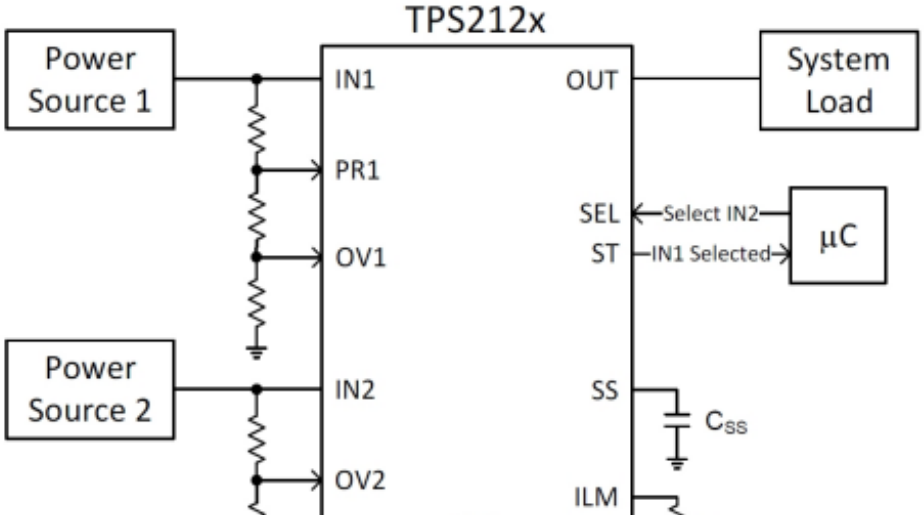
Size: A4 | Id: 15/20



Pin 10: 100kOhm leads to about 1.24A (absolute overkill)

[R] = [kOhm]	22 kΩ → ~4.55 A
65.2 / R^0.861	39 kΩ → ~2.78 A
	50 kΩ → ~2.25 A
	56 kΩ → ~2.04 A
	68 kΩ → ~1.72 A
	100 kΩ → ~1.24 A

Pin SS (11): 100nF soft start cap more than enoug as virtually no load at all at vref

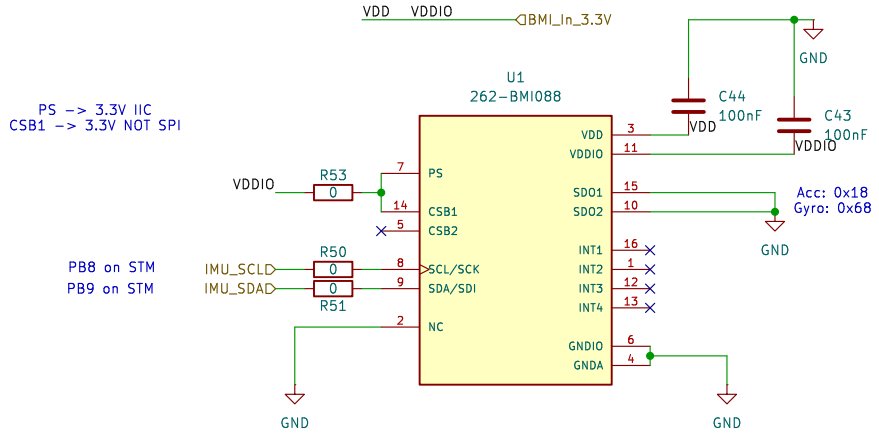


3V/

Rev:

Size: A4

Id: 16/20



Accelerometer
SDO1 pin pulled to GND (0x18)
SDO1 pin pulled to VDDIO: (0x19)

Gyroscope:
SDO2 pin pulled to GND: (0x68)
SDO2 pin pulled to VDDIO: 0x69)

Title:

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Author:		
Date:	Size: A4	Id: 19/20
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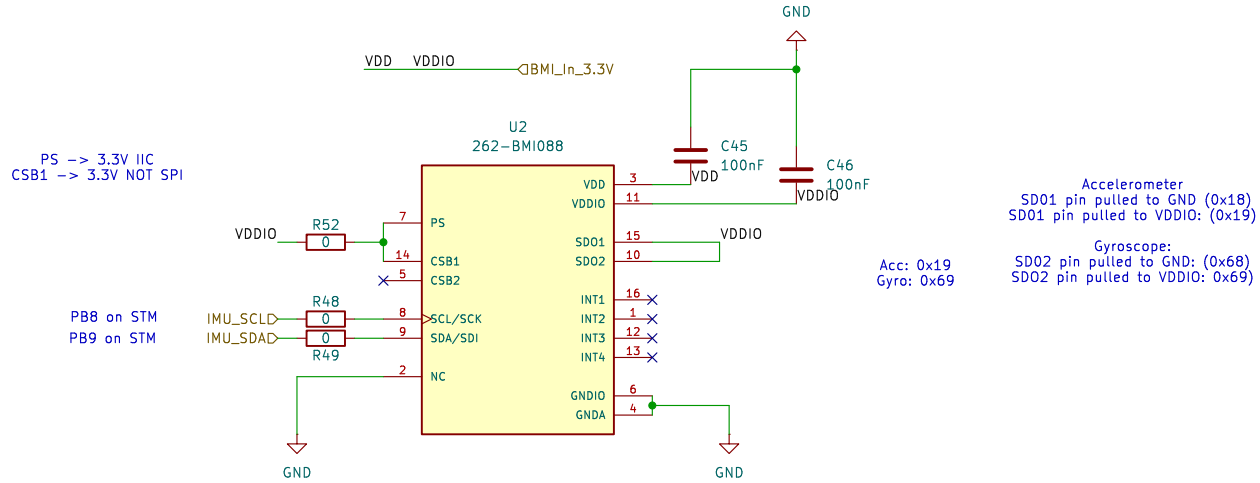

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Date:	Size: A4	Id: 20/20
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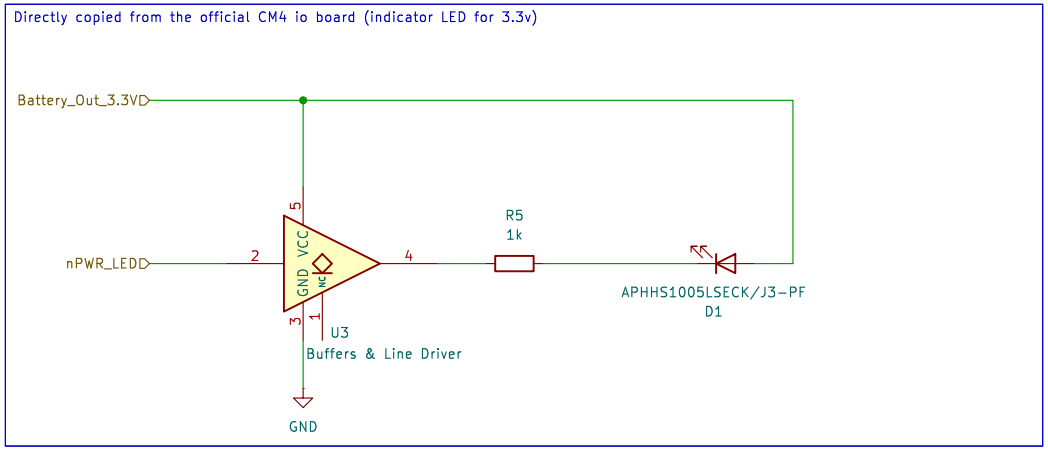
Directly copied from the official CM4 io board (indicator LED for 3.3v)



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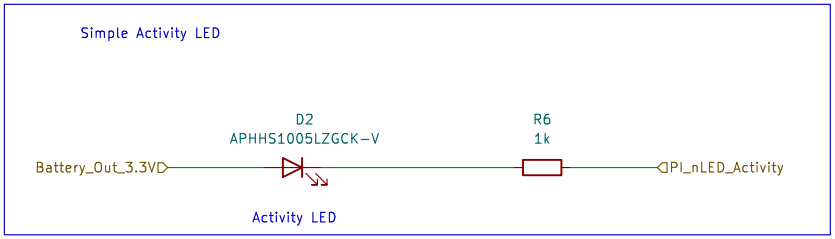

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Date:	Size: A4	Id: 9/20
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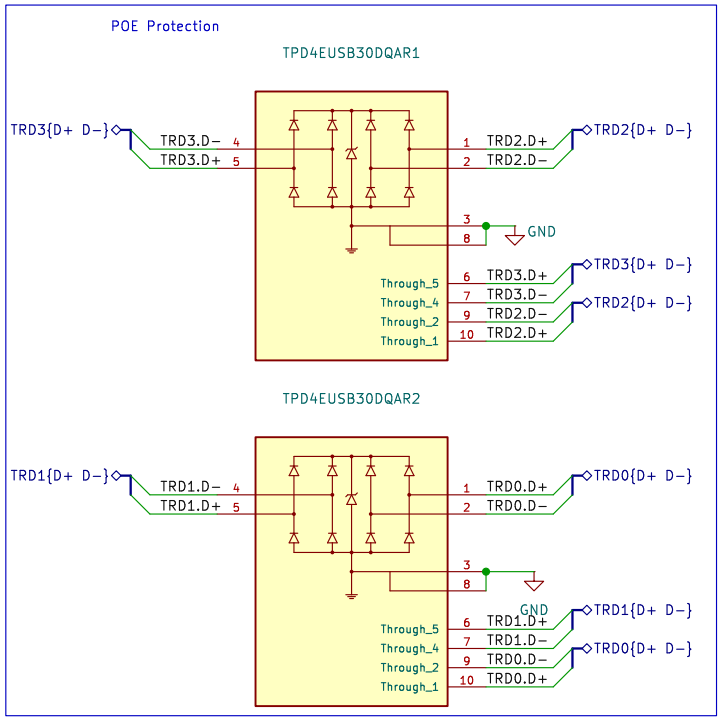

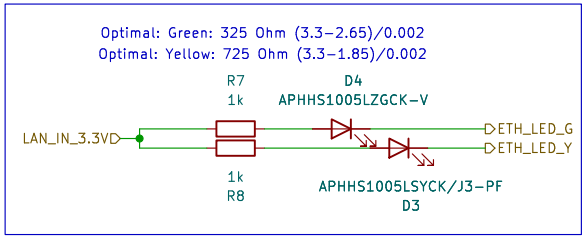

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File: CM4_Ethernet.kicad_sch		