Capacitive Micromachined Ultrasound Transducers (CMUT) for Distance Measurement

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***Abstract*—Capacitive Micromachined Ultrasound Transducers (CMUT) have been widely used by the industry owing to its numerous advantages such as easy fabrication process, higher bandwidth, better integration etc. In this project a CMUT cell is designed for distance measurement with frequency in the 100-150 kHz range. The entire design and analysis were performed considering that the CMUT was to be fabricated using PolyMUMPs technology. Various analyses were done in ANSYS software tools (Workbench, Mechanical APDL, Twin Builder) and MATLAB that included FEM, modal analysis, reduced order modelling (ROM) etc. Graphs and results from these simulations showed the CMUT characteristics and confirmed the calculations. The desired result was achieved and compared with the FEM model having minor variation from the analytical model. To drive the CMUT, a Voltage control ring oscillator was designed. A frequency divider and voltage-controlled voltage source (VCVS) and was also employed to get the voltage signal at the desired frequency and amplitude. A digital logic that generates a Pulse Width Modulated voltage of required frequency based on a constant clock frequency was implemented as input to the analog system.**

Keywords—CMUT, FEM, linear perturbation, modal analysis, coupled simulation, ANSYS Twin Builder, Cadence Virtuoso, VHDL, ModelSim

I. Introduction

Capacitive Micromachined Ultrasound Transducers or CMUTs is a breakthrough ultrasound technology that has emerged as a viable mechanism for generating stable ultrasound signals. CMUTs are MEMS devices that can generate and receive acoustic signals falling within the ultrasonic range of the spectrum (>20 kHz). They are increasingly being employed in a wide variety of industrial and medical applications such as in microscopy, printer inkjet, portable scanners and many others. In comparison to traditional ultrasound transducers, CMUTs deliver number of advantages such as easier fabrication process for large arrays, large bandwidth and better integration with driver circuitry. They have also recently emerged as a possible substitute to piezoelectric transducers due their advantages mentioned above. The basic structure and typical working modes of a CMUT is shown at Fig. 1 [1].

This project is aimed for the design of a CMUT for range sensor development that would enable the estimation of objects/obstacles close to the sensor using acoustic signals for the application of a smart shoe guidance system. This smart system can detect obstacles, fall detection, level difference and other smart features. The purpose of the smart integrated system or the smart shoe is to guide the user while moving. The guidance system includes the features mentioned above. There are other features such as GPS monitoring, analyzing user's movement and create an analysis report to monitor the health condition. As a part of these all function these CMUT transducer plays an important role where this can be integrated in the system which will provide necessary data not only for instantaneous guidance during movement but also data for analyzing and generating the health conditioning report of the user. Therefore, this project is focused on CMUT design, simulation and results for later to be included in the integrated system.

CMUT cells generally consist of electrodes, diaphragms (membranes), and cavities in a parallel capacitor plate arrangement. When the CMUT is in operation, a DC bias voltage is frequently given to cause the film to sink into the cavity due to the force generated between the parallel plates, increasing the transducer's sensitivity [2]. The AC signal should be superimposed on the applied DC bias voltage when transmitting ultrasound, and the driving frequency of the AC signal then becomes the ultrasound transmission frequency. On the other hand, the diaphragm is responsible for converting mechanical energy into electrical signals when receiving the ultrasonic signals. For establishing the CMUT based sensor idea, a single element circular CMUT in vacuum can be considered for development and the parameters can be designed as in [3] with a resonance frequency and operational voltage which shall be decided based on commercial standards.

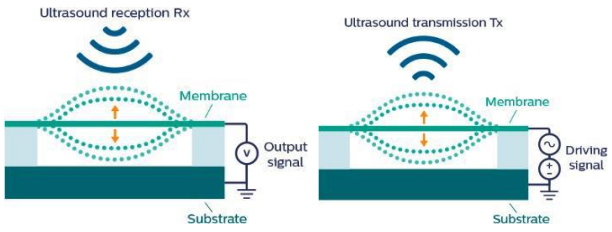

Fig. 1 Basic structure and typical working modes of a CMUT [1]

The purpose of this project is to make simulations on ANSYS software tools in order to create a model of CMUT and study effects of different mechanical and electrical parameters on the frequency output of the device. Moreover,

analytical calculations and proper comparison between simulation results are also presented.

II. Reduced Order Modelling of the MEMS Device

A. Simulation outline

- FEM Simulation – provides numerically solved solutions for mechanical and electrical problems of the CMUT model. By analyzing the results of FEM, we can troubleshoot existing flaws and do required optimization. Moreover, FEM simulation also creates a base for the next procedures such as modal analysis and Twin Builder simulation. The main emphasis in the FEM simulation is meshing, which was done after numerous adjustments of local and global mesh parameters (element size, method, edge sizing etc.) to find the most optimal combination.
- Modal Analysis – is performed to detect the dynamic properties of our MEMS device and detect the resonant frequencies and resonant vibration mode shapes to see how it reacts under harmonic excitations. Furthermore, these results are used to generate a reduced order model (ROM), which is required for Twin Builder simulation. The main emphasis in the modal analysis is setting required simulation parameters (loads, constraints, perturbation etc.) in the form of APDL codes which was also adjusted several times to achieve and ideal simulation.
- Harmonic response simulation – is done to obtain steady-state response of the structure subjected to a force vector. The simulation outputs are frequency response plots of phase angle and amplitude.
- Twin Builder simulation – is done to provide digital twin of the device, where we can apply electrical signals at the input and plot mechanical output. Later this mechanical output is analyzed to study the behavior of the transducer.

B. Material properties

The materials as well as key geometrical parameters were chosen based on the Polysilicon - Multi-User MEMS (PolyMUMPs) process rules [4] which specifically highlights possible materials and critical dimensions. The top and bottom plate are made of polysilicon. As an insulating material, silicon-oxide is used between two plates, and silicon-nitride is used at the bottom layer. The properties of these materials (Table I) are set based on a detailed paper review, except for the young modulus of air which was calculated based on maximum value of bias voltage and minimum value of the distance between plates. Adjusting this value was very important because as we have experienced during the simulation it highly affects the value of membrane deflection. For the calculation the following formula is used [5].

$$E_{air} = 0.01 * \frac{1}{2} * \varepsilon_0 * \frac{U_{max}^2}{d_{min}^2} \qquad (1)$$

Here E_{air} is the Young's Modulus of air, U_{max} is maximum bias voltage between the plates, d_{min} is the minimum distance between the plates.

It is important to mention that for the silicon oxide the parameter values were extracted from the default library of COMSOL Multiphysics.

Table I. Key Material Properties

	Air [6]	Polysilicon [7]	Silicon-Oxide*	Silicon-Nitride [8]
Density (kg·m^{-3})	1.23	2230	2200	3270
Young modulus (GPa)	1.44E-7	160	70	320
Poisson number	0	0.22	0.17	0.263
Relative permittivity	1	-	-	-

**Reference mentioned in ANNEX*

C. Geometry

For the CMUT structure, the top and bottom membranes are polysilicon and in between (at the edge) there is silicon oxide which is acting as the sacrificial layer. The bottom layer is the silicon nitride which is used as the insulating layer. Between the membranes there is also a layer of air to make the top membrane vibrate.

As shown in Fig. 2 the radius of the membrane is 286 µm and this radius is maintained for the other layers as well. The thickness for both the top and bottom membrane is 2 µm, t_g the thickness of the gap and the silicon oxide is 3.5 µm. The thickness of the silicon nitride layer is 3.5 µm.

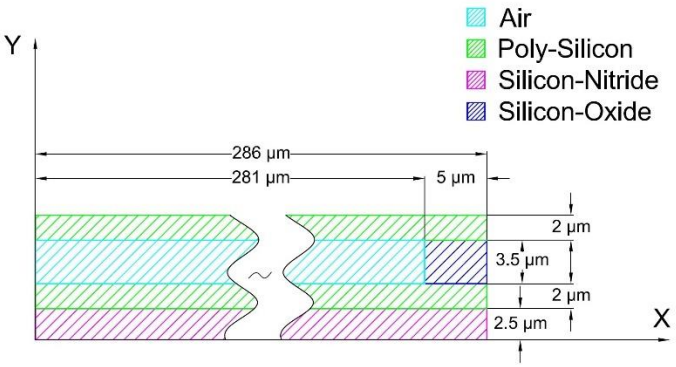

Fig. 2 Material and the structure of CMUT cell

For the geometry structure 2D axisymmetric type was used. Initially we tried with the 3D analysis but later changed our model to 2D. Fig. 2 and Fig. 3 show the structure of the CMUT cell with its material and dimension.

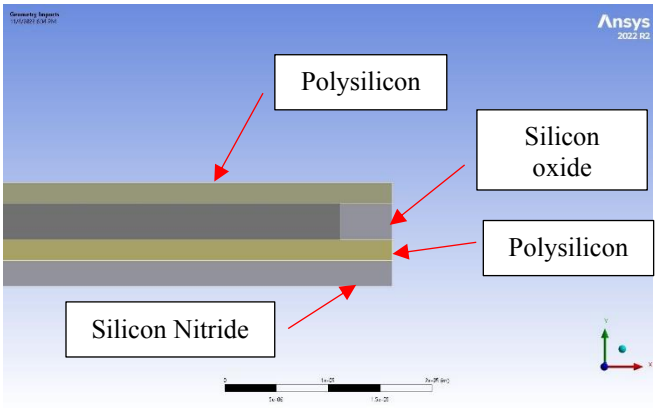

Fig. 3 Structure of the CMUT in ANSYS Simulation

The thickness shown above were estimated in order to obtain the desired range of eigenfrequency. As for the gap

thickness, during the value estimation phase in MATLAB modelling we obtained which illustrates (Fig. 4) the relation between membrane thickness with different radius and gap thickness modelling. The radius of the membrane is related to the collapse voltage and increasing the radius eventually decreases the voltage value and to overcome the situation the gap thickness plays a good role. For this model specifically, it was determined that the thickness of gap must be more than 3 µm to keep the spring constant, K valid with respect to the radius of 286 µm. Otherwise, the system collapses much earlier than expected. Table II summarizes the parameters for CMUT.

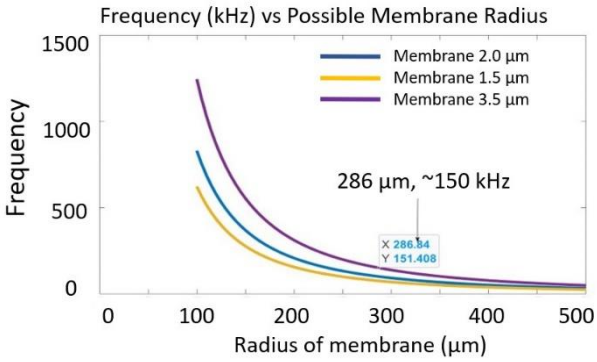

Fig. 4 Graph for resonance frequency vs membrane radius for predicting the range

TABLE II IMPLEMENTED PARAMETERS FOR CMUT

Parameter	Values (µm)
Membrane thickness, t_m	2
Gap Thickness, t_g	3.5
Radius of gap layer	281
Bottom polysilicon thickness	2
Radius of the membrane, a	286
Silicon Nitride thickness	2.5
Silicon oxide thickness	3.5

D. Meshing

The global mesh setting was in the Nonlinear Mechanical, Element Order was Linear, and the element size was 2 µm. For the meshing of the whole structure, Multizone Quad/Tri Method was used. The layer edge sizing are set in the y-direction. Surface mesh method was Program Controlled, and Element Order was Linear. The feature size was 2 µm. The MultiZone mesh method provides automatic decomposition of geometry into mapped (structured/ sweepable) regions and free (unstructured) regions. It automatically generates a pure hexahedral mesh where possible and then fills the more difficult to capture regions with unstructured mesh [9]. The overview of the mesh geometry can be seen in Fig. 5 and the sideview of mesh with edge sizing can be seen in Fig. 6.

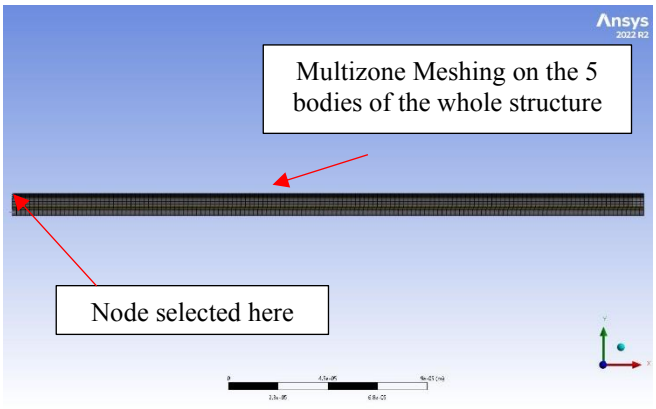

Fig. 5 Overview of the mesh geometry

As the structure is 2D axisymmetric, edge sizing was used for each of the edge. For the edge sizing the top membrane was given 8 number of divisions and the other layers were given 6. For the insulator i.e., the silicon nitride layer, the behavior of the edge sizing was chosen as hard and for other layers it was selected as soft. The significance of selecting the behavior as hard is the priority order in the meshing. The edge sizing had a default growth rate of 1.5.

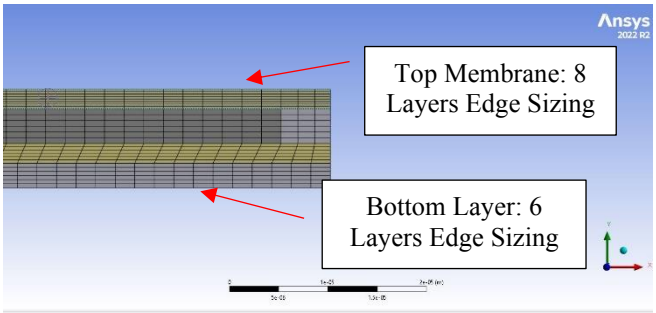

Fig. 6 Sideview of mesh with edge sizing

TABLE III MESH PARAMETERS & STATISTICS

Mesh Parameters	Values/Settings
Element Size	2 µm
Nodes Numbers	3915
Element Numbers	3744
Coupled Elements Number	846
Growth Rate	1.5
Physical Preference	Nonlinear Mechanical
Element Order	Linear

From Table III the mesh parameters and the mesh statistics can be found. Nodes number was 3915 and elements number was 3744 from the simulation.

E. Test load simulation

The Capacitive Micromachined Ultrasonic Transducer (CMUT) functions as a capacitive cell. The upper membrane of the cell gets attracted to the bottom electrode by the electrostatic forces when a DC voltage is applied between the upper and lower electrodes. When an AC signal is given, this drives the top membrane to vibrate and responses to generate ultrasound. This action of CMUT acts as a transmitter. In this project we will focus on the transmission part [10].

As the CMUT operation involves the combination of mechanical and electrical domain analysis, the coupled simulation was performed. As mentioned within the material section the top membrane which undergoes physical deflection has polysilicon material type and it shares its boundary with the air domain which corresponds to the cavity inside. The membrane which is a solid domain is mapped to SOLID185 element type, which defines an eight-node structural solid element with three degrees of freedom at each node, with default key option 0 corresponding to homogenous structural solid element. As described in the meshing section, the air domain was divided into multiple layers for accurately modelling the domain interfaces. Since the layers in the air domain that shares a boundary with the top and bottom membranes experience a force due to the voltage applied on membrane, an electrostatic structural analysis is performed (with field key 1001) by mapping these layers as elastic air with electrostatic force applied at air-structure interface using the key option 4 with value 1. The remaining layers in the air domain are mapped to elastic air with no electrostatic forces using a third element type number. The element type numbers assigned based on the layers in the model are shown in Fig. 7.

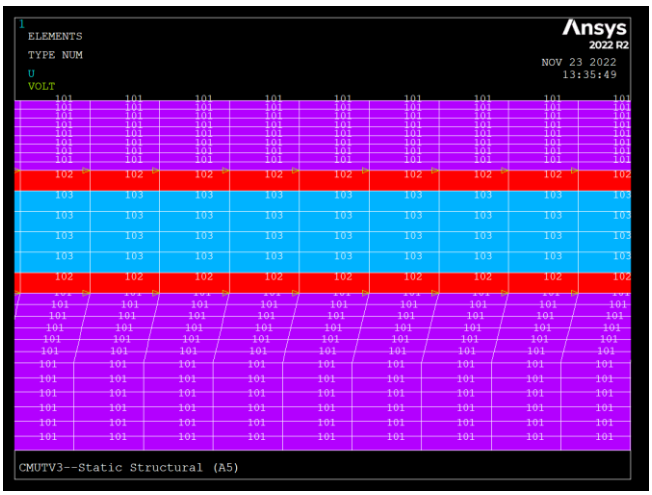

Fig. 7 CMUT geometry showing the element type numbers in APDL

Boundary conditions were applied over the defined geometry to allow the membrane to deflect only along the y-direction, which corresponds to the z-axis displacement in 3D structure. This was done by first adding a fixed support at the side walls of the CMUT structure to prevent any deformation at that edge (axis of symmetry). A predefined DC voltage was supplied to the CMUT by biasing the top plate at 20 V and the bottom plate at 0 V using APDL *cmsel* command by referencing the required named selections created in ANSYS Mechanical. The settings for the solver include activating large-deflection effects for the static analysis, increasing the number of equilibrium iterations from default value to 50 to prevent un-converging solutions, making the voltage load ramped and configuring a sparse direct equation solver which is suited for such non-linear analysis having multiple mesh layers of air.

For the simulation, a solver setting was defined for the analysis of the CMUT structure under the given DC voltage of 20 V. Ideally, the best point to operate the device to achieve maximum deflection would be near its pull-in or collapse voltage. From the analytical calculations, the pull-in voltage of the membrane was roughly 47 V for the given dimension and material properties. But considering that the very high voltage is not feasible as the application of the designed CMUT is for the smart shoe project, a trade-off had to be made between the bias voltage and membrane deflection, after which the currently used bias voltage was defined. The next part was the application of an additional voltage that will correspond to the AC voltage required for membrane deflection to produce the acoustic waves. This was performed by applying the ROM load which is discussed in the coming chapter. The analysis of the CMUT is challenging as it involves several physical domains in its operation. One way to study its process is to do the analytical calculation to find different parameters.

This part will have the discussion about the analytical calculations involved in this CMUT project. For the first calculation the estimated electrostatic force is found under a given bias of 20 V:

$$F_e = \frac{1}{2}\frac{\varepsilon_0 \varepsilon_r A V^2}{d^2} \tag{2}$$

Here, F_e is the electrostatic force, ε_0 is the relative permittivity in vacuum, ε_r is the relative permittivity of air, A is the area of the structure, V is the bias voltage set and d is the gap between the membranes.

Under the given electrostatic force and the mechanical loads, the deflection is represented as

$$w(r) = \frac{1}{64}\frac{F}{AD}(r^2 - a^2) \tag{3}$$

Where F is the force applied, A is the area r is the radius and a is the deflection from the center, D is the flexural rigidity which is calculated by dividing Young's modulus with membrane radius [11].

For the natural frequency, E is the Young's modulus, T is the intrinsic stress, ρ is the density of the material and σ is the Poisson's ratio. For this calculation intrinsic stress was not present. The equation for the frequency was derived from this paper [12].

$$f_r = \frac{1}{2\pi}\sqrt{\frac{k}{m}} \approx \frac{2t_m}{\pi a^2}\sqrt{\frac{E+T}{1.8\rho(1-\sigma^2)}} \tag{4}$$

For the calculation of the collapse or pull-in voltage, the following equation was used [13] . Here, t_m is the thickness of the membrane, t_g thickness of the gap between the plates and a is the radius of the plate.

$$V_{col} \approx 0.7\sqrt{\frac{128(E+T)t_m^3 t_g^3}{27\varepsilon_0(1-\sigma^2)a^4}} \tag{5}$$

To find the sensing capacitance for the membrane equation 5 [11] was used. Here, w_c is the center deflection of the membrane,

$$C_{w_c} = \frac{\pi a^2 \varepsilon_0}{d} \frac{1}{2\sqrt{w_c/t_g}} ln\left(\frac{\sqrt{w_c/t_g} + (\frac{w_c}{t_g})}{\sqrt{w_c/t_g} - (\frac{w_c}{t_g})}\right) \quad (6)$$

For the actual damping factor (D) of the CMUT the following equation was used, where Z_{air} is the acoustic impedance of air, Q is the quality factor, ρ is the density. Equation 7 and 8 are used from this paper [14].

$$\frac{Q_{air}}{f} \approx \frac{2\pi t \rho}{Z_{air}} \quad (7)$$

$$D = \frac{1}{2Q_{air}} \quad (8)$$

The results for the calculation and simulation are listed in Table IV.

TABLE IV ANALYTICAL AND SIMULATED RESUTS

Parameters	Analytical Calc.	Simulation	% Difference
Deflection at 20V bias	0.135 μm	0.131 μm	~2.96
Pull in voltage	47.5 V	< 52.0 V	~9.34
Natural Frequency	97.6 kHz	106 kHz	~8.61
Sensing Capacitance	0.667 pF	0.635 pF	~3.03

After the initial analysis was performed, the total deformation observed at the polysilicon membrane center was 0.131 µm. This was close to the analytical result which was calculated as 0.135 µm. The error percentage with respect to the simulated and calculated results were close to 3%. For the pull-in voltage, which is the voltage at which the plates of the top membrane sticks to the bottom membrane, the simulated result is approximately 52 V while the calculated pull-in voltage was 47 V. Finally, the resonant frequency of the membrane was compared between the calculated and analytical results which were 97.6 kHz and 106 kHz respectively. The percentage difference between the two calculated and simulated results for all values were within 10% margins. The same results are tabulated in Table IV.

F. Output quantity dependence on bias voltage

Using ANSYS Mechanical, the dependence between the provided bias voltage and the top membrane deflection was compared by parameterizing the bias voltage. The simulated deflection results for each of the bias voltages were exported and plotted against the deflections obtained from the analytical calculations at the same voltages.

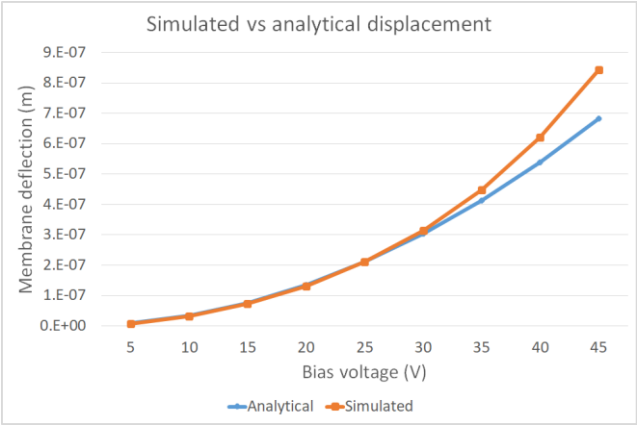

Fig. 8 Comparison of the simulated and analytically calculated membrane displacement (data from Table V)

TABLE V COMPARISON OF ANALYTICAL AND SIMULATED DISPLACEMENT FOR DIFFERENT BIAS VOLTAGE

Bias Voltage (V)	Membrane Displacement (µm)		% Difference
	Analytical Calc.	*Simulation*	
5	0.00843	0.00752	10.8
10	0.03370	0.03163	6.15
15	0.07583	0.07228	4.69
20	0.13482	0.13100	2.83
25	0.21065	0.21100	0.17
30	0.30334	0.31500	3.84
35	0.41288	0.44900	8.75
40	0.53927	0.62000	14.9
45	0.68251	0.84400	23.6
5	0.00843	0.00752	10.8

Table V shows the comparison of analytical calculation and simulation values for different bias voltages. As shown in Fig. 8, the polynomial curve for both the simulated and analytical solutions are similar with variations observed only towards the pull-in voltage. Additionally, to check if the simulated model performs well around the resonant frequency, a harmonic analysis was performed, which requires a pressure load to be supplied corresponding to the pressure induced by sound waves on the membrane. Ultrasound sensors in medical imaging operating around 2 MHz generate close to 100 dB sound pressure which is 2 Pa [15]. At this pressure, the force exerted on the designed CMUT would be the product of area and pressure which is 0.5 µN. As our CMUT has close to one-fifth the ultrasound frequency, 0.1 µN was used as force on the membrane and its response was studied from 65 kHz to 200 kHz.The results obtained as shown in Fig. 10 indicate a good response close to the first resonant frequency.

Fig. 9 shows the total deformation displacement of the membrane with 20 V bias. Simulation was also performed for 10 V to 50 V on the top membrane. Simulation was done up to 50 V because as mentioned previously, pull in voltage was obtained just around 50 V bias. Here, it is important to observe that the displacement on the bottom plate is minimum. The reason may be due to the change of Young's modulus of air with the bias voltage. So, the air rather than acting only as a coupled medium it acts as a high viscous fluid having higher damping factor. Thus, reducing the displacement of the bottom plate as well as the insulating layer.

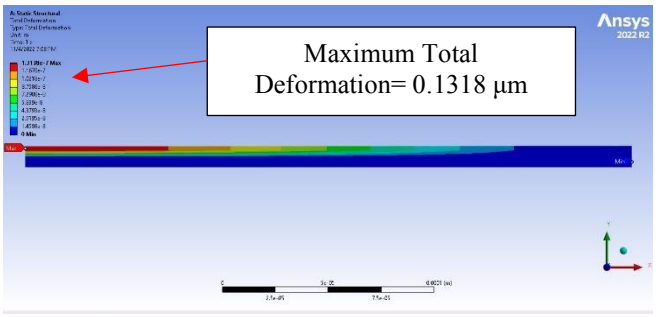

Fig. 9 Total deformation of the membrane for 20 V bias

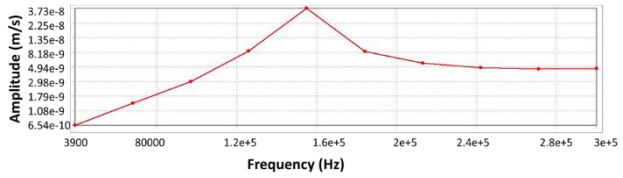

Fig. 10 Frequency response of CMUT around the first resonance frequency

G. *Modal analysis*

With regards to modal analysis, a linear perturbation was performed as the device required coupled analysis. The maximum, number of modes to find were 5. The settings from the static structural analysis were applied here as well but for the supports. As mentioned previously, the calculated value for damping was considered using APDL commands, along with the settings for simulation of multiple layers of mesh in each section. Later, ROM load was added depending on the desired behavior of the model and lastly the model was exported for further simulation. Below, Fig. 11 illustrates the mode shapes for first three frequencies implemented through ANSYS APDL.

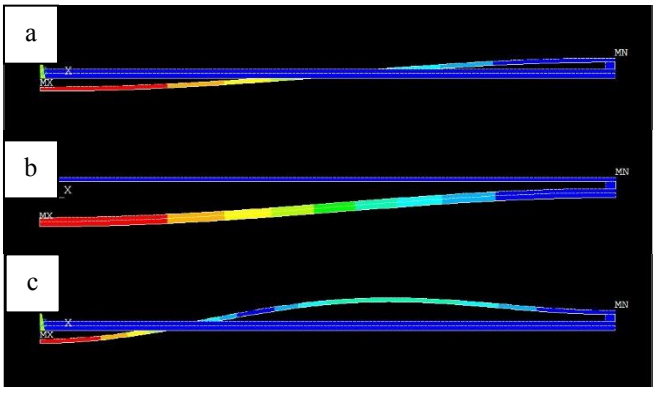

Fig. 11 Modes shapes a) mode 1, b) mode 2, c) mode 3

H. *ROM Generation*

A Reduced Order Model was exported and simulated in Twin Builder to observe the deflections caused by a continuously varying sinusoidal voltage. The ROM loads for the ROM model itself were defined using APDL code. The node with node number 1 (center node shown in Fig. 5) at the membrane was selected, as the deflection was to be calculated around the top membrane center. A voltage load of 10 V ROM load was provided at the top plate of the device so that the voltage on the CMUT would remain within the pull-in limits. A damping factor was introduced for the air domain by setting the damping ratio to 0.074. This value was calculated from the quality factor which in turn was derived based on the acoustic impedance of air, as shown in the analytical calculation section equation (7) The ROM model of the CMUT has only one input which is the input voltage (1 V) applied in addition to the bias voltage present in the linear perturbation analysis and one output which is the displacement of the membrane, which are defined using the APDL commands.

The natural frequencies of the model which were collected from the solution information of modal analysis are listed in Table VI. The resonance frequency 106 kHz is close enough to the analytical one as discussed in this report.

TABLE VI NATURAL FREQUENCY OF THE MODEL

Number of Mode	Natural frequency (Hz)
1.	106791
2.	238832
3.	391418
4.	873750
5.	926249

Most of the literature reviewed were for the application of high frequency range i.e in the MHz range. An earlier study [13] where the resonance frequency was approximately 5 MHz and pull in voltage was ~212 V. For the mentioned work the center displacement was around 0.36 µm before the pull in voltage and 0.01 µm for 50 V bias voltage, whereas in our case the displacement for the same situation was 0.62 µm near to pull in and 0.135 µm with only 20 V bias. In terms of the frequency our result was 106 kHz which is less than the mentioned research by few magnitudes.

I. *ROM usage*

The designed model was exported to Twin Builder after ROM generation. As per the designed specification, voltage is provided at input and output corresponds to displacement. Several simulations were carried by changing the ROM loads with 20 V as bias voltage. Other simulations were also performed for different bias voltages with varying the amplitude of the input sine wave as shown in Fig. 12.

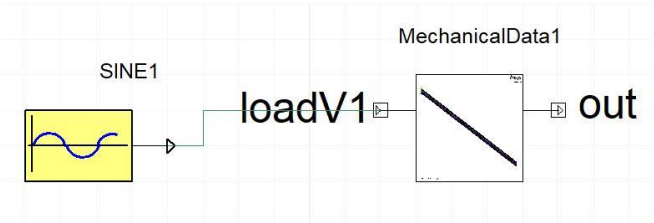

Fig. 12 Twin Builder model for designed device.

As ROM load of 5 V being added, the displacement took place, and which can be observed in Fig. 13.

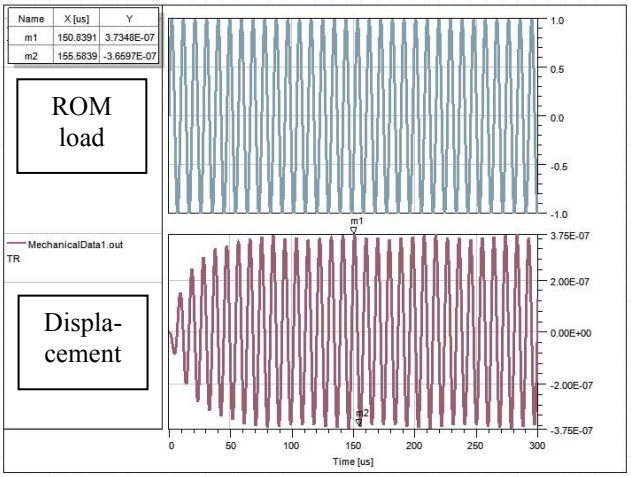

Fig. 13 Displacement for 20V bias and 5 V ROM load at 106 kHz.

The output as seen in Fig. 13 depicts that the displacement is around 0.37 µm for the given load and input voltage. Displacement results based on other ROM load (10 V, 15 V) voltages and different sine wave regarding frequency are illustrated in Fig. 14.

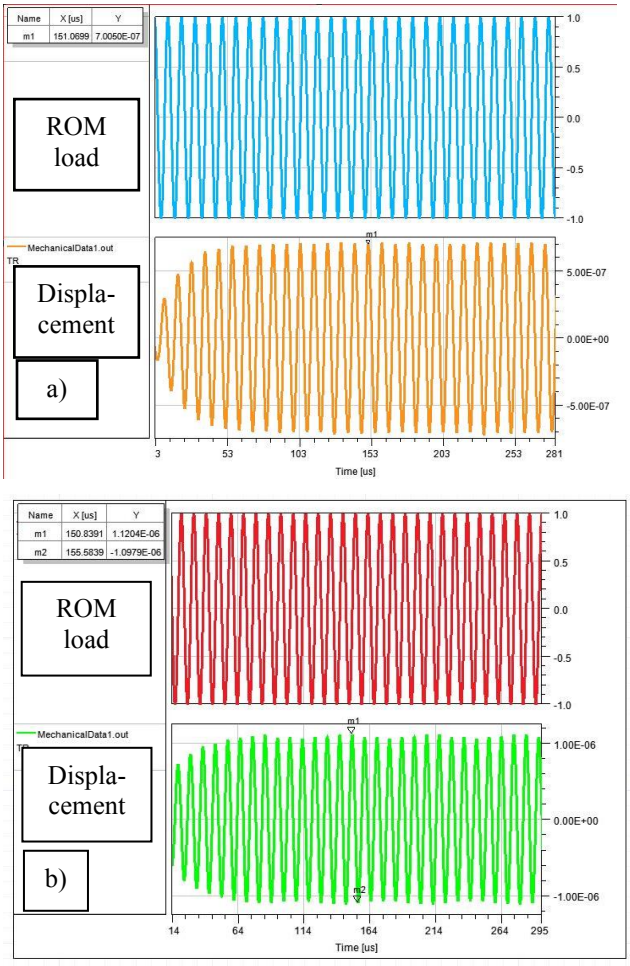

Fig. 14 Output behavior for a) 10 V and b) 15 V ROM loads with 106 kHz sine wave.

From several simulations, it can be observed that the relation of input and output is quite linear as the displacement increases linearly with increasing input until the model reaches the pull in region and the linear relationship is depicted in Fig. 15. This linear behavior can be explained using the mode superposition technique where it uses a linear combination of modes to solve dynamics problems. For this work the mode superposition response analysis express the displacement as a linear combination of mode shapes [16]. Thus, depicting a linear relation between the input and the output.

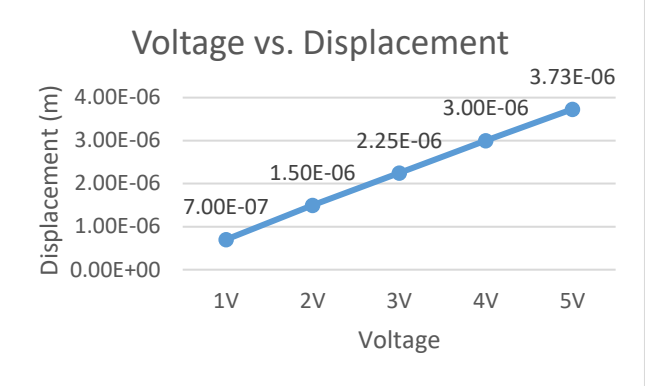

Fig. 15 Displacement at different sine input at 106 kHz frequency

Finally, the model was set with ROM load 10 V amplitude and in Twin Builder we implemented sine wave with 106 kHz frequency and 1 V amplitude to obtain reasonable displacement of 0.7 µm which would aid in proceeding further with the project. This displacement is much higher than the simulation observed in workbench before. The reason could be the implementation of natural frequency as input. Therefore, the model displacement increases significantly at the operating resonance or natural frequency. However, the in-Twin Builder the output can be observed for much lesser frequency as well as shown in above figures.

J. ROM of CMUT Conclusion

Analytical calculations and simulation were performed for a CMUT structure for an intended low bias voltage compared to previous studies. The desired output frequency range of ~106 kHz and significant displacement (0.135 µm) was achieved for a lower bias voltage (20 V) but without any sinusoidal signal. To make the model analysis more realistic, ROM was used to obtain the displacement in Twin Builder by continuously varying sinusoidal voltage. Different displacement outputs were obtained for different ROM loads. It was observed that the relation of input and output is quite linear, as the membrane displacement increases linearly with increasing input until the model reaches the pull in region.

III. ANALOG CIRCUIT DESIGN

A. Overall Idea for Analog Circuit

For the air coupled CMUT application, a front circuit plays an important role in the collection of signals and integration of system. There are some requirements that need to be fulfilled for designing the circuit. For the CMUT application, firstly a digital PWM signal is needed to be fed into the voltage-controlled oscillator (VCO). Before feeding into the VCO the signal is passed through a RC filter. As the output of the VCO is in high frequency range, a frequency divider is used to get the output in the range of the desired frequency. For the smart shoe guidance application that is in the kHz range. The amplitude of the signal becomes less and

to amplify it a voltage-controlled voltage source is used in the last part of the circuit. Fig. 16 outlines the overall analog and digital circuit system design as mentioned. A brief overview of each of the circuit systems is in the following discussion.

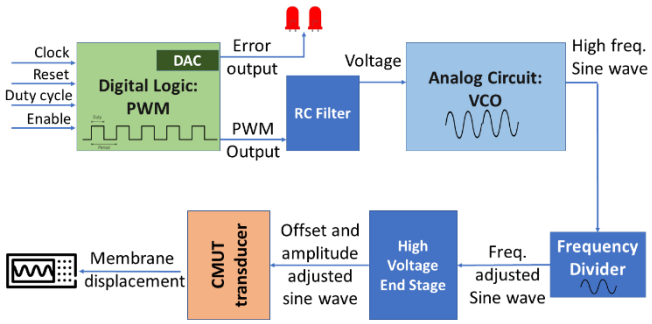

Fig. 16 Overall circuit configuration for analog and digital system

A voltage-controlled oscillator is an electronic oscillator designed for getting oscillations by controlling a voltage input. The frequency of oscillation can be varied by using the voltage control. VCO plays an important role in communication system, providing a periodic signal and frequency transmission needed for digital circuit system. If ideal VCO is considered, then its output frequency is linearly proportional of its control voltage. VCO also has low power consumption, operation in wide frequency range, phase stability less area, low cost, large gain factor and ease of highly integration ability. It uses amplification, feedback, and a resonator circuit to produce a replicating voltage waveform at a desired frequency. An applied voltage varies the frequency or the rate of repetition per unit time. VCOs are widely used in locked loops, clock recovery circuits, and frequency synthesizers [17].For this work a current starved VCO based on ring oscillator is used with extra transistors acting as a current source for the inverters.

The frequency divider is used here to decrease the magnitude of the high frequency output that comes from the VCO. It adjusted the frequency according to the desired range of application. After the signal is passed through the frequency divider the signal is amplified with a voltage-controlled voltage source (VCVS). The VCVS works as an amplifier to increase the amplitude of the signal.

Circuit design and simulation for the analog circuit was done in Cadence Virtuoso software tool. VCO was designed in transistor level. Cell view was used for the schematics design. Only the frequency divider is made using the Verilog-A for making the block and used in the cell view.

B. Comparison of Topologies

Ring oscillator can be made of odd number of inverters ("NOT" gates) [18]. The number of inverter stages (N) is inversely proportional with the oscillation frequency (f_{osc}). So, the minimum number of stages results in oscillation frequency in GHz range. For the MHz range frequencies more number of stages with bigger transistors are used, which causes more power consumption [19]. So, the number of stages creates a delicate tradeoff between oscillation frequency and power consumption. Table VII summarizes the tradeoffs respectively for less and a greater number of stages.

TABLE VII STAGE NO. TRADEOFFS BETWEEN THE DIFFERENT PARAMETERS OF RING OSCILLATORS

Parameters	Less stages	More stages
Frequency [19]	more	less
Power consumption [19]	less	more
Transistor size [19]	less	more
Jitter [20]	less	more
Phase noise [20]	less	more

There are different types of ring oscillators depending on the application for specific parameters as mentioned in Table VII. In the next part few of the ring oscillator topologies are discussed.

1) *LC VCO:*

The resonance frequency of the energy-storing components is what causes the LC oscillator, a resonator circuit, to oscillate. Usually, it is made up of a parallel pair of capacitors and inductors. A lossless LC circuit is the ideal case. The energy flows continuously between the inductor and capacitor in a perfect LC tank circuit because there is no damping. The Q of the tank circuit used in oscillators has a significant impact on phase noise. The tank circuit must thus be continuously monitored in order to minimize phase noise [21]. One type of LC VCO is the complementary cross-coupled LC VCO shown in Fig. 17. This form of VCO has both kinds of MOS transistors inside the core. Consequently, the voltage swing is increased and double transconductance is provided. According to the function, the complementary cross-coupled CMOS VCOs can run either with or without tail current. Complementary cross-coupled CMOS is used due to its symmetrical waveform and low phase noise [22]. Due to the symmetrical waveform of this design, the DC component of phase noise is eliminated, improving phase noise performance [23].

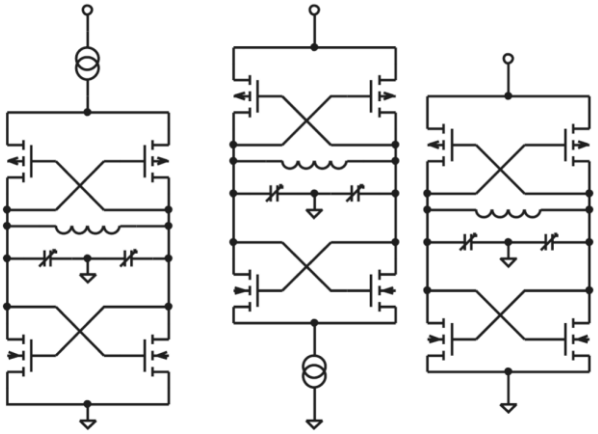

Fig. 17 Complementary cross-coupled LC VCO with a) PMOS tail current b) NMOS tail current c) No tail current [24]

2) *Currrent Starved Ring Oscillator:*

Fig. 18 shows the conventional CSRO architecture that includes a bias circuit a bias circuit (M1-M3), basic CMOS inverters (M4-M9), PMOS current sources (M10-M12), and NMOS current sinks (M13-M15). From Eq. (9) the bias current I_d and also the frequency is controlled by the external control voltage V_{ctrl}. The bias current must change linearly when the control voltage varies in order to maintain linearity across a broad frequency range. However, in a conventional design, given a specific range of control voltage, one of the

bias circuit's transistors (PMOS) runs in the saturation region while another (NMOS) operates in the linear region, leading to nonlinearity in the biasing current. The linearity of the VCO is also controlled by the current source/sink transistors' (CSTs) operating area. The CSTs function in the triode area when the control voltage is high, and their gate voltages have less of an impact on the bias current [25]. The result is a narrowing of the tuning range for frequencies. Additionally, the delay is prolonged because M13–M15's drain voltages converge with each stage's output voltage before the load capacitance is discharged. A similar approach is made for designing the intended circuit for our analysis that is discussed in the next section.

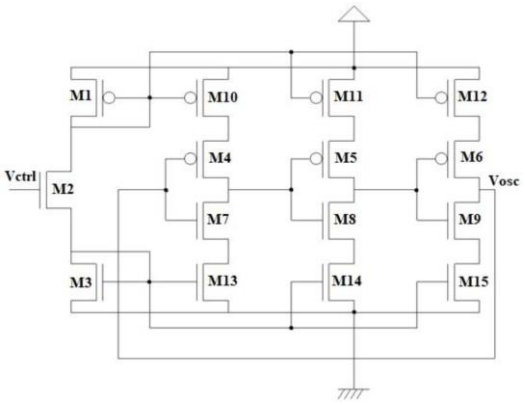

Fig. 18 Conventional Current Starved Ring Oscillator (CSRO) [26]

3) Current Starved Skewed Topology:

Fig. 19 depicts the schematic for the 7-stage current-starved negative skewed NMOS delay RO (NMOS skewed CS). This oscillator uses a combination of CS and NMOS skewed techniques to operate. To reduce the circuit's power consumption, CS lowers the reference bias current. However, the NMOS skewed approach can be used to make up for the frequency reduction that results from this.

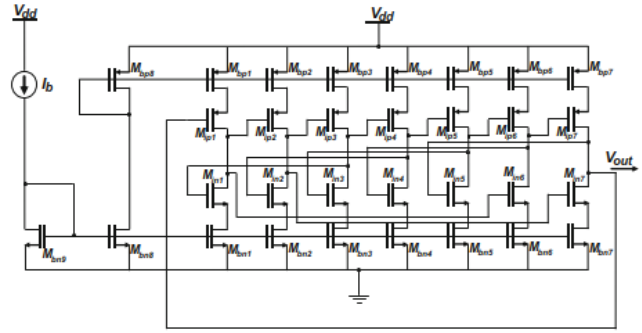

Fig. 19 Schematic of 7-stage NMOS skewed CS ring Oscillator [27]

When compared to an increase in frequency, this method's power gain is less. This is so that the tradeoff between frequency and power consumption can be compensated for in both the CS and NMOS biased approaches.

C. Description of Selected Topology

For our project we have utilized current starved ring oscillator with nine stage which includes extra transistors to mirror the same current to each stage also ring oscillator is being used in various technologies as a common topology. These extra transistors reduces the current which causes lower power consumption, but on the other hand reduced current affects the maximum frequency [26] There are many proposed current starved ring oscillator (CSRO) which utilize different biasing circuits. From Table VIII, the implemented parameters can be observed. The supply voltage, V_{dd} was chosen based on the design specification. The output frequency is maximum when $V_{ctrl} = V_{dd}$ [28]. As for this project, the control voltage ranges from 0.6-1.0V and for that purpose V_{dd} was set to 1.0V. As for the sizes of the transistor and some other parameters the minimum feature size was chosen. This is the minimum feature which is known as 0.35 μm technology for implementing or integrating in analog and mixed signal (AMS) [29].

TABLE VIII PARAMETERS FOR RING OSCILLATOR [28], [29]

Parameters	Value	Unit	Method
Supply Voltage, V_{dd}	1	V	Literature review [28]
Threshold Voltage, V_{th}	0.5	V	Simulation and datasheet
Switching point, V_{sp}	>= 0.5	V	Simulation
Trans-conductance, nMOS, K_n	170	μA/V^2	Datasheet [29]
Trans-conductance, pMOS, K_p	58	μA/V^2	Datasheet [29]
Oxide Thickness, T_{ox}	7.6	nm	Datasheet [29]
Oxide Capacitance, C_{ox}	4.54	fF	Calculated
Width of nMOS, W_n	10	μm	Minimum feature size
Width of pMOS, W_p	30	μm	Three size larger than W_n
Length of nMOS, L_n	0.35	μm	Minimum feature size
Length of pMOS, L_p	0.35	μm	Minimum feature size

D. Hand Calculations

This sub-section will discuss about the hand calculations that are done for the analog circuit part. Oscillation frequency is given by the following formula [19], [26]:

$$f_{osc} = \frac{1}{T} = \frac{1}{N\,(t_1 + t_2)} = \frac{I_d}{NC_{tot}V_{dd}} \qquad (9)$$

Here, T is period, N is number of inverter stages, t_1 and t_2 are delays to charge from 0 V to V_{SP} (switch point) and discharge from V_{dd} to V_{SP}, I_d is bias current, C_{tot} is the total capacitance, and V_{dd} is the supply voltage. In the hand calculations the oscillation frequencies are calculated corresponding to different values of the drain current.

Total capacitance on the drains of NMOS and PMOS transistors of a single inverter can be calculated as [19], [20]:

$$C_{tot} = C_{out} + C_{in} = \frac{5}{2} C_{ox}(W_p L_p + W_n L_n) \qquad (10)$$

Here C_{out} is the output capacitance, C_{in} is the input capacitance, C_{ox} is the oxide capacitance per unit area W_p, L_p and W_n, L_n are width and length of PMOS and NMOS respectively.

The time delays of the VCO is t_1 and t_2, which are the equations (9) can be expressed as [19]:

$$t_1 = C_{tot}\frac{V_{sp}}{I_d} \quad (11)$$

$$t_2 = C_{tot}\frac{V_{dd} - V_{sp}}{I_d} \quad (12)$$

The calculation of the charge and discharge time of the capacitor using these formulas mentioned above.
Oxide capacitance per unit area is calculated by the following formula [29]:

$$C_{ox} = \frac{\varepsilon_0 \varepsilon_r}{T_{ox}} \quad (13)$$

Here, ε_0 is permittivity of vacuum, ε_r is permittivity of silicon-oxide, and T_{ox} is the thickness of oxide layer at the transistor gate.

The bias current I_d is given by the following set of formulas [30]:

$$I_d = \frac{\mu C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_{Th})^2 \quad (14)$$

Here μ is the mobility of the charge carrier, V_{GS} is the gate-source voltage and V_{Th} is the threshold voltage. For simplicity, the values of width and length were kept fixed, so the drain current can only depend on the on-voltage (V_{GS}-V_{Th}).

Table IX contains the simulation results and hand calculation of oscillation frequencies at 10 different values of the control voltage. There is clear deviation between these values, and based on our observations, we have discovered 2 main reasons for it:

1) First of all, the formulas which are used for the hand calculation are only applicable for the operation of transistors in the strong inversion region, so it can be observed that below the threshold voltage (V_{th}= 0.5 V) simulated oscillation frequency and hand calculation results are in different orders. On the other hand, around the switching point voltage the deviation of frequency is considerably small. Table IX depicts the result of hand calculation and simulation only when the control voltage is above threshold as there is no bias current generation below the threshold voltage.
2) Secondly, the simulation values belong to a complete ring oscillator design which includes mirroring transistors, while on the other hand in hand calculations mirroring transistors are not considered.

TABLE IX COMPARISON BETWEEN SIMULATION VALUES AND HAND CALCULATION

Control Voltage (V_{ctrl})	Drain Current (I_d)	Simulated Oscillation frequency (f_{osc})	Calculated Oscillation frequency (f_{osc})
0.6 V	3.3 µA	7.04 MHz	2.3 MHz
0.7 V	6.8 µA	8.01 MHz	4.75 MHz
0.8 V	11.4 µA	9.21 MHz	8.0 MHz
0.9 V	16.3 µA	11.45 MHz	11.39 MHz
1.0 V	21.3 µA	12.57 MHz	14.88 MHz

E. Cadence Schematics

The design of the VCO along with other components are depicted in following figures.

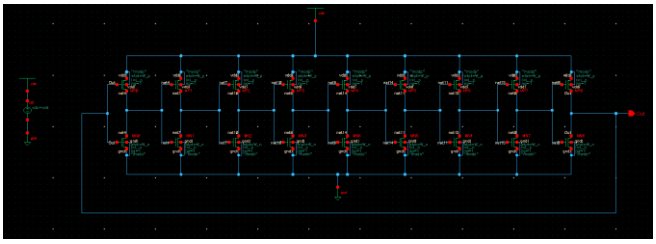

Fig. 20 Ring oscillator (9 stage)

Here the 9-stage ring oscillator (Fig. 20) is depicted without any control voltage. The following in Fig. 21 is the full circuit diagram illustrating the current starved variable ring oscillator with an input of a ramp signal.

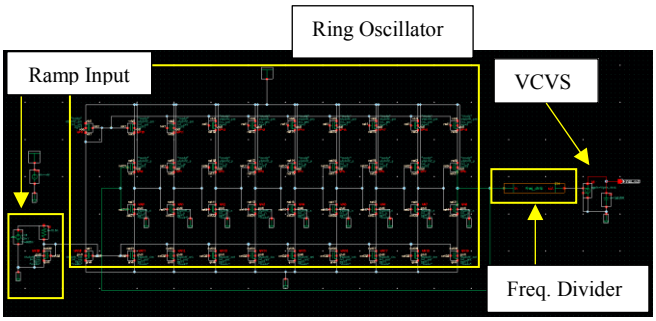

Fig. 21 Full topology of the design

As output of the design, it contains a frequency divider which scales down the frequency as mentioned earlier and through a VCVS amplifier we achieve our desired output. Here the capacitance at the output is our mems-capacitance of 0.15 pF. In following figures, the schematic of the individual parts is shown for better visual.

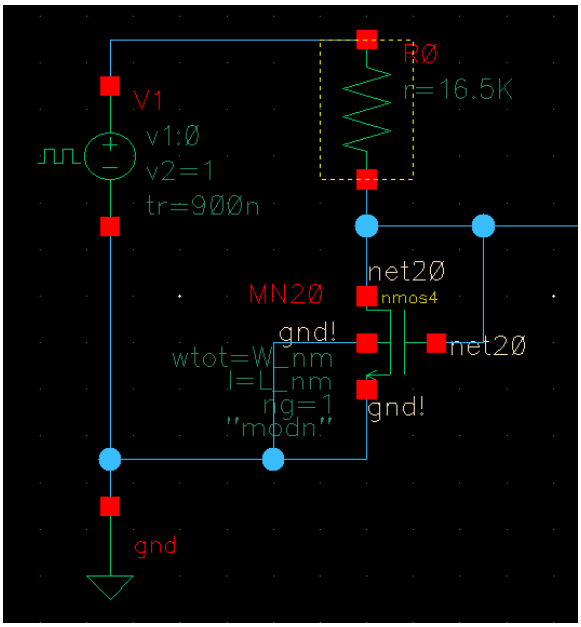

Fig. 22 Bias current generation for inverter stage (VCO)

The ramp signal (Fig. 22) with diode connected transistor for mirroring the input bias current.

Fig. 23 Frequency Divider component

Shown in Fig. 23, the frequency divider generated with analog-A with divide ratio of 38. In following figure includes the script of the frequency divider.

The code for the frequency divider is shown in Fig. 24. Here in the generic code, the ratio was set to 38 to convert generated 7-12MHz ring oscillator output to 106±3 kHz. The output voltage parameter here is a variable so it can be modified in simulation setup as well according to the requirement of the design. As for this project it was set to 0-1 V as low and high state respectively.

```
`include "disciplines.vams"
module divider1 (out, in);
output out; voltage out;
// output

input in; voltage in;
// input (edge triggered)

parameter real vh=+1;
// output voltage in high state

parameter real vl=-1;
// output voltage in low state

parameter real vth=(vh+vl)/2;
// threshold voltage at input

parameter integer ratio=38 from
[38:inf);
// divide ratio

parameter integer dir=1 from [-1:1]
exclude 0;
// dir=1 for positive edge trigger
// dir=-1 for negative edge trigger

parameter real tt=1n from (0:inf);

// transition time of output signal

parameter real td=0 from [0:inf);

// average delay from input to
output

integer count, n;

analog begin
    @(cross(V(in) - vth, dir))
begin
        count = count + 1;
// count input transitions

        if (count >= ratio)
            count = 0;
        n = (2*count >= ratio);
    end
    V(out) <+ transition(n ? vh :
vl, td, tt);
end
endmodule
```

Fig. 24 Verilog-a code for frequency divider, modified from [31]

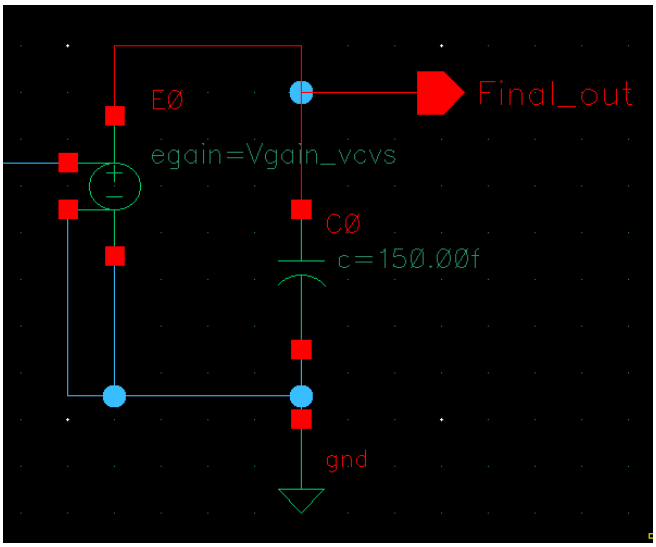

Fig. 25 VCVS for amplification (high voltage end stage)

VCVS shown in Fig. 25 used with high gain to amplify the voltage level of the output frequency to the desired value.

F. Result of analyses

1) Transient Analysis

For transient analysis following setup (Fig. 26) window is depicting the chosen parameters which are being mentioned earlier as well.

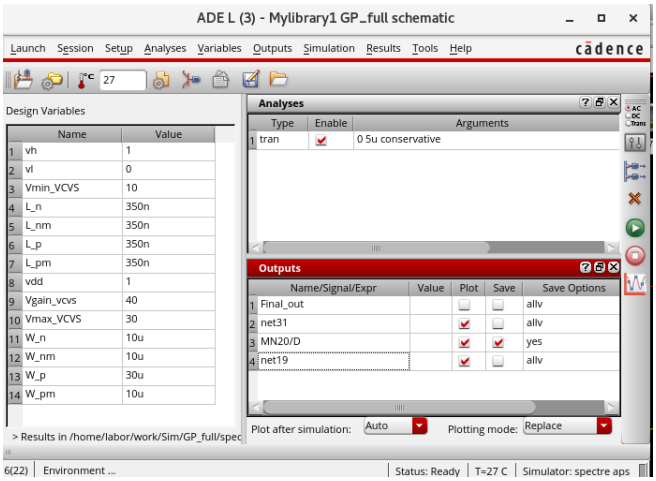

Fig. 26 Setup for transient analysis in simulator

The following figures depict the output of the ring oscillator and final output from the VCVS for a ramp input signal of 0-1 V along with the setup parameter shown in parameter window.

The following Fig. 27 depicts the biasing current with respect to the ramp signal in input. The triggering happens when the ramp signal reaches over 0.5 V as it is expected, and current is around 1.2 µA.

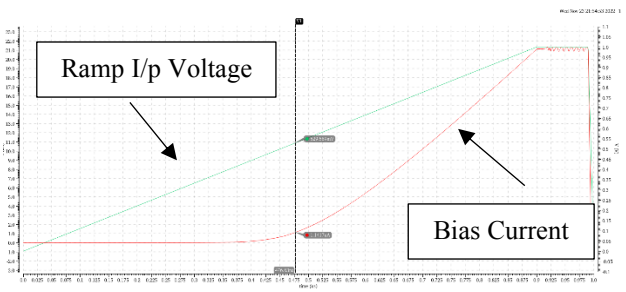

Fig. 27 Bias current with Ramp Input voltage

The frequency is being added with CALC function in Cadence which is shown in the following figure where we can see the frequency of ring oscillator. The changes in frequency are 7-12 MHz for ring oscillator output and the frequency of final stage is 106±3 kHz as shown in Fig. 28.

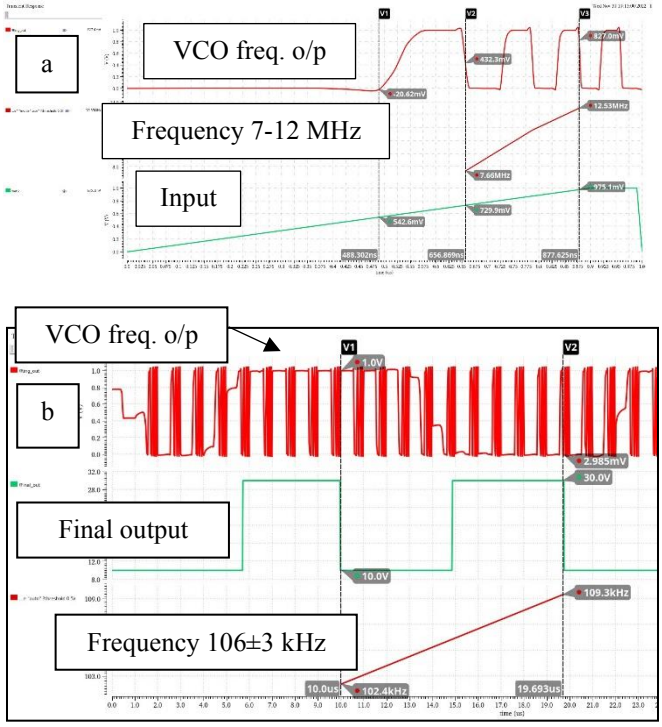

Fig. 28 Frequency analysis plot at b) Ring Oscillator and b) Final stage

From the Fig. 29 of transient analysis, we can see that the ring oscillator output is quite high in frequency range working for a ramp input and at the output as the frequency is around 106 kHz which is our resonance frequency of the designed transducer. The output characteristics are mentioned earlier in Table IX depicting the output of VCO ranging from 7 MHz to 12 MHz.

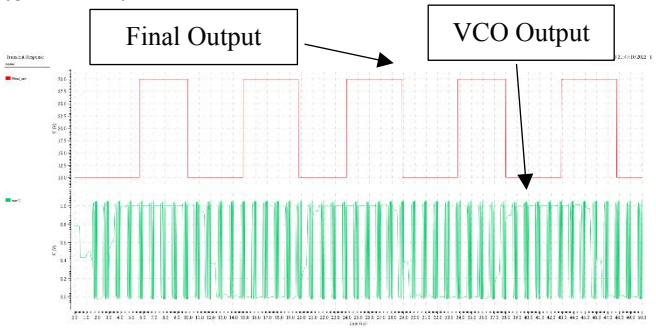

Fig. 29 Transient analysis plots

2) PVT Analysis

PVT analysis is the process, voltage, and temperature simulation used to evaluate the effectiveness of the model using the model's minimum and maximum values for different parameter. In this case the parameters were set by creating corners were for CMOS wp-worst power and ws-worst speed were chosen. In total 19 corners were created with the temperature set to -40, 27 and 85 degree Celsius and the voltages set to 0.8, 1.0 and 1.2 V to observe the variations in the circuit. During the simulation transient analysis were done for the ring oscillator.

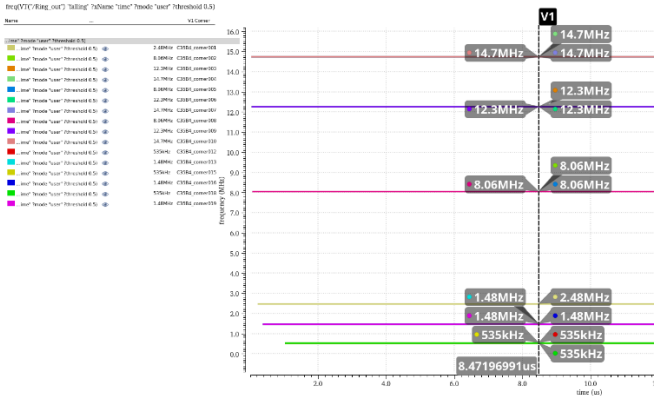

Fig. 30 PVT 1 Output Frequency at 0.6 V for all corners.

TABLE X PVT 1

Control Voltage, V_{ctrl} (V)	Corner No.	Supply Voltage, V_{dd} (V)	Temperature (°C)	Condition	Oscillation frequency, f_{osc} (MHz)
0.6	1	1.0	27	cmostm	2.479
	2	0.8	-40	cmoswp	8.058
	3	0.8	27	cmoswp	12.27
	4	0.8	85	cmoswp	14.75
	5	1.0	-40	cmoswp	8.058
	6	1.0	27	cmoswp	12.27
	7	1.0	85	cmoswp	14.75
	8	1.2	-40	cmoswp	8.058
	9	1.2	27	cmoswp	12.27
	10	1.2	85	cmoswp	14.75
	11	0.8	-40	cmosws	-
	12	0.8	27	cmosws	0.535
	13	0.8	85	cmosws	1.476
	14	1.0	-40	cmosws	-
	15	1.0	27	cmosws	0.535
	16	1.0	85	cmosws	1.476
	17	1.2	-40	cmosws	-
	18	1.2	27	cmosws	0.535
	19	1.2	85	cmosws	1.476

Here in Fig. 30 the output frequency of all the corners are shown and Table X it can be observed that the output is almost consistent in every case except for case 11, 14 and 17 where the corners were created for worse speed and the temperature is -40 °C. Regarding these cases, in low temperature the switching speed decreases as the mobility of electron or charge decreases.

Fig. 31 PVT 2 Output Frequency at 0.8V for all corners.

TABLE XI PVT 2

Control Voltage, V_{ctrl} (V)	Corner No.	Supply Voltage, V_{dd} (V)	Temperature (°C)	Condition	Oscillation frequency, f_{osc} (MHz)
0.8	1	1.0	27	cmostm	7.639
	2	0.8	-40	cmoswp	16.02
	3	0.8	27	cmoswp	21.47
	4	0.8	85	cmoswp	24.48
	5	1.0	-40	cmoswp	16.02
	6	1.0	27	cmoswp	21.47
	7	1.0	85	cmoswp	24.48
	8	1.2	-40	cmoswp	16.02
	9	1.2	27	cmoswp	21.47
	10	1.2	85	cmoswp	24.48
	11	0.8	-40	cmosws	1.693
	12	0.8	27	cmosws	3.628
	13	0.8	85	cmosws	5.359
	14	1.0	-40	cmosws	1.693
	15	1.0	27	cmosws	3.628
	16	1.0	85	cmosws	5.359
	17	1.2	-40	cmosws	1.693
	18	1.2	27	cmosws	3.628
	19	1.2	85	cmosws	5.359

As for other cases shown in Table XI, Table XII, Table XIII, Table XIV, Fig. 31, Fig. 32, Fig. 33, and Fig. 34. All the corners were solved. The only difference with the first analysis is that the control voltage is more. In first analysis it was 0.6 V and for later case it was 0.8 V, 1.0 V, 1.2 V and 1.4 V.

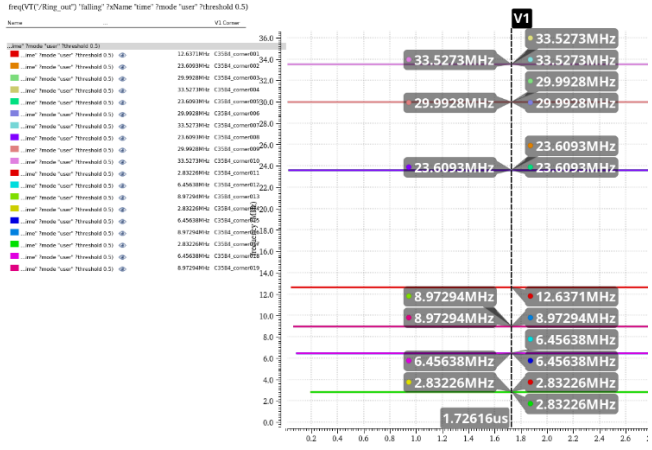

Fig. 32 PVT 3- Output Frequency at 1.0 V for all corners.

TABLE XII PVT 3

Control Voltage, V_{ctrl} (V)	Corner No.	Supply Voltage, V_{dd} (V)	Temperature (°C)	Condition	Oscillation frequency, f_{osc} (MHz)
1.0	1	1.0	27	cmostm	12.64
	2	0.8	-40	cmoswp	23.61
	3	0.8	27	cmoswp	29.99
	4	0.8	85	cmoswp	33.53
	5	1.0	-40	cmoswp	23.61
	6	1.0	27	cmoswp	29.99
	7	1.0	85	cmoswp	33.53
	8	1.2	-40	cmoswp	23.61
	9	1.2	27	cmoswp	29.99
	10	1.2	85	cmoswp	33.53
	11	0.8	-40	cmosws	2.832
	12	0.8	27	cmosws	6.456
	13	0.8	85	cmosws	8.973
	14	1.0	-40	cmosws	2.832
	15	1.0	27	cmosws	6.456
	16	1.0	85	cmosws	8.973
	17	1.2	-40	cmosws	2.832
	18	1.2	27	cmosws	6.456
	19	1.2	85	cmosws	8.973

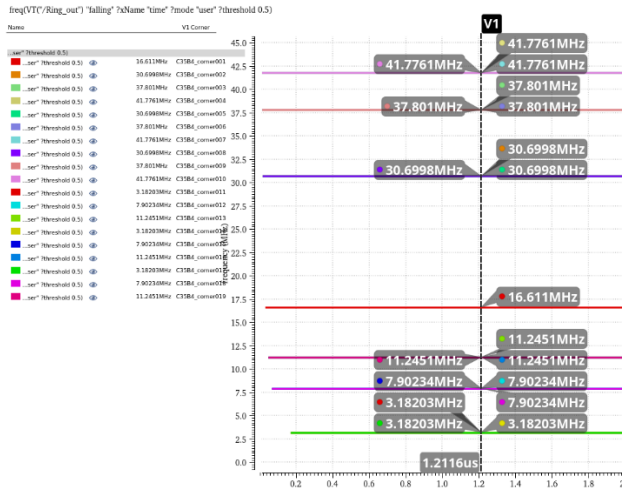

Fig. 33 PVT 4- Output Frequency at 1.2 V for all corners

TABLE XIII PVT 4

Control Voltage, V_{ctrl} (V)	Corner No.	Supply Voltage, V_{dd} (V)	Temperature (°C)	Condition	Oscillation frequency, f_{osc} (MHz)
1.2	1	1.0	27	cmostm	16.61
	2	0.8	-40	cmoswp	30.70
	3	0.8	27	cmoswp	37.80
	4	0.8	85	cmoswp	41.78
	5	1.0	-40	cmoswp	30.70
	6	1.0	27	cmoswp	37.80
	7	1.0	85	cmoswp	41.78
	8	1.2	-40	cmoswp	30.70
	9	1.2	27	cmoswp	37.80
	10	1.2	85	cmoswp	41.78
	11	0.8	-40	cmosws	3.182
	12	0.8	27	cmosws	7.902
	13	0.8	85	cmosws	11.25
	14	1.0	-40	cmosws	3.182
	15	1.0	27	cmosws	7.902
	16	1.0	85	cmosws	11.25
	17	1.2	-40	cmosws	3.182
	18	1.2	27	cmosws	7.902
	19	1.2	85	cmosws	11.25

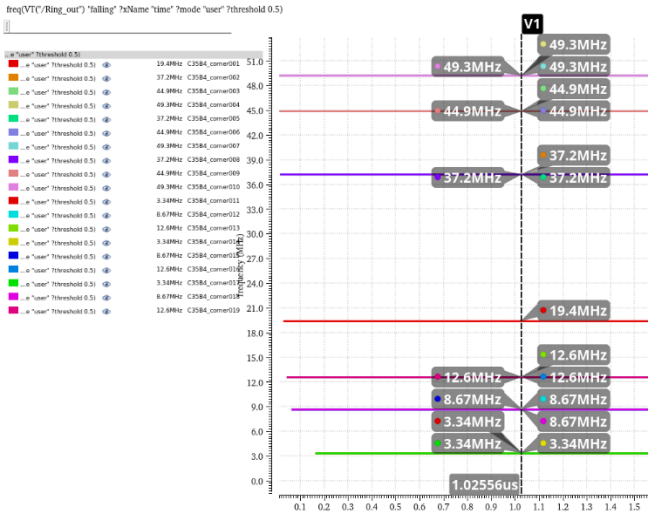

Fig. 34 PVT 5- Output Frequency at 1.4 V for all corners

TABLE XIV PVT 5

Control Voltage, V_{ctrl} (V)	Corner No.	Supply Voltage, V_{dd} (V)	Temperature (°C)	Condition	Oscillation frequency, f_{osc} (MHz)
1.4	1	1.0	27	cmostm	19.41
	2	0.8	-40	cmoswp	37.24
	3	0.8	27	cmoswp	44.93
	4	0.8	85	cmoswp	49.26
	5	1.0	-40	cmoswp	37.24
	6	1.0	27	cmoswp	44.93
	7	1.0	85	cmoswp	49.26
	8	1.2	-40	cmoswp	37.24
	9	1.2	27	cmoswp	44.93
	10	1.2	85	cmoswp	49.26

	11	0.8	-40	cmosws	3.338
	12	0.8	27	cmosws	8.669
	13	0.8	85	cmosws	12.57
	14	1.0	-40	cmosws	3.338
	15	1.0	27	cmosws	8.669
	16	1.0	85	cmosws	12.57
	17	1.2	-40	cmosws	3.338
	18	1.2	27	cmosws	8.669
	19	1.2	85	cmosws	12.57

With the PVT analysis, the noticeable thing is that in worst power and worst speed scenario the frequency is almost same in all analysis for their respective control voltage despite the change in supply voltage and temperature condition variation. The only change is that the frequency of output decreases when the condition is set for worst speed. However, the order (MHz) remains same for all cases except the first analysis where the control voltage is 0.6 V.

G. Creation of an Analog Cell of the Circuit

As the design have different parts for difference functions, a cell was generated of the VCO to be used as a block in the circuit simulation. Fig. 35 depicts the block of the VCO.

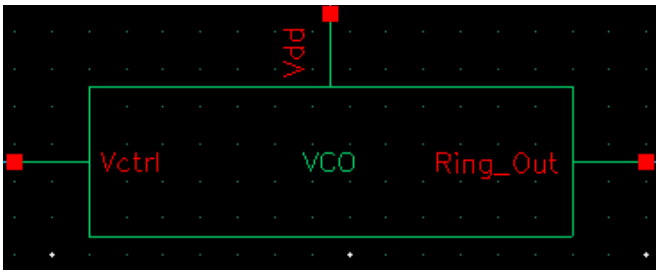

Fig. 35 Analog cell of VCO

Here the V_{ctrl} is the control voltage input in, V_{dd} is the supply and Ring out is the output pin of the VCO which is connected to the frequency divider in the full setup. This was also tested successfully and same output were obtained during the simulation.

H. Analog Circuit Conclusion

The final output was satisfactory regarding the requirements of the transducer. As, the analog design is implemented to get the input of the transducer and for that one VCO was required. For stable functioning ring oscillator performed as expected and usage of frequency divider and amplifier generated the final output which in consequently feed the transducer input signal to displace the membrane and create oscillation as described earlier.

IV. DIGITAL DESIGN

A. Digital Design Description

The CMUT transducer required a sinusoidal voltage around the resonance frequency of the device, as input, to produce the membrane displacements that will generate the ultrasound waves. To achieve this a combination of digital and analog logics were used as shown previously. The requirement for the digital logic was to generate a Pulse Width Modulated (PWM) voltage whose duty cycle would determine the voltage that is passed on to a voltage-controlled oscillator (VCO), through a RC (Resistor Capacitor) circuit. Hence the duty cycle had to be controllable, and it forms the main input for the digital logic. Such a system can be effectively realized by programming the logic using VHDL (Very High Speed Integrated Circuit Hardware Description Language) and implemented on FPGA (Field Programmable Gate Array) hardware by synthesizing the written code. This is highly advantageous as the interfaces and system components can be tailored to our requirement in comparison to using microcontrollers or other off-the-shelf boards. FPGA uses Configurable Logic Blocks to achieve the digital logic and hence introduce minimal delays. As VHDL enables top-down design approach where the system development can be made using Register Transfer Level (RTL) logic, the programming is easier to write and understand. The project also needed a subcircuit to convert the digital output signal to analog voltage. This meant the usage of mixed signals was necessary and it was best achieved using VHDL Analog and Mixed Signal (AMS) programming using ANSYS Twin Builder.

To perform the HDL programming, ModelSim HDL Simulator from Siemens was used. It is a multi-language environment that can perform simulation of hardware description languages like VHDL, Verilog and SystemC. The project did not involve implementing the design itself on an FPGA and using the hardware independently, but instead only a check was made to see if the code was synthesizable and to explore the resource usage when implemented on an FPGA. For this, a Programmable Logic Device (PLD) design software named Altera Quartus II (or Intel Quartus II) was used.

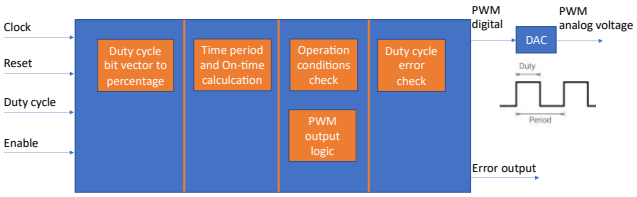

Fig. 36 Overall digital logic with independent subcircuits

The block diagram of the digital circuit is shown in Fig. 36. A synchronous digital system is designed for the project which requires a clock and reset signal. The clock signal is designed considering the Altera DE0 Cyclone III FPGA development board. Thus, the system clock frequency was defined as 50MHz corresponding to the frequency generated on the board. An enable signal was considered to activate the output logic. The data input which controls the pulse width of the PWM is the duty cycle, which is designed as an 8-bit vector. At the output, digital logic produces a continuous PWM analog voltage of defined duty cycle. The frequency of the PWM output is a design requirement and hence is considered as a fixed parameter within the design. The major subcircuits of the design are as follows:

- Duty cycle bit vector to percentage: This stage converts the 8-bit duty cycle input vector to a percentage value so that the PWM parameters can be effectively derived based on this
- Time-period and on-time calculation: Time period is calculated based on the clock frequency and required

PWM frequency. On-time is derived based on the duty cycle percentage which is set by the user.

- Operation conditions check: Checks if the control inputs such as reset and enable are as prescribed for system operation. The digital logic to generate the digital PWM output is activated only when the enable input is high.
- PWM output logic: Generates the digital PWM output based on the given duty cycle and calculated time-period.
- Duty cycle error check: A feature to limit the duty cycle values that may be selected for the PWM. The analog circuit requires voltage within the range of 0.5 V to 1 V. Since the duty cycle of the PWM decides the voltage generated at the output of RC circuit, this subcircuit limits the duty cycle input by producing an error if the value used will generate an out-of-range output voltage at RC stage (Resistor Capacitor circuit).
- Digital to Analog Converter (DAC): This subcircuit written in VHDL AMS converts the digital voltage that is generated by the PWM logic, to an analog voltage that can be supplied to the RC circuit.

Major part of the digital system implementation was performed in VHDL using behavioral logic. Conditional and relational operators for most of the decision subcircuits. Since the digital system forms the input stage of the overall architecture, a reliable signal generation is necessary. First, the decision circuits are synchronized by a reliable clock signal which is designed to match that generated by DE0 FPGA board and a reset signal is also considered. Additionally, an enable signal controls the overall activation of the output logic. When the buttons on the FPGA board are used to provide the bit values of duty cycle, a debounce logic can be employed to overcome the physical effects of the buttons. Also, to prevent the PWM output from behaving incorrectly, the on-time value is only read once in a time-period window, using a read lock signal. This preserves the timing characteristic of the signal in every time-period.

B. Digital Design Implementation

The PWM logic in VHDL is implemented as a single entity with input and output parameters. The major input parameters for the PWM circuit design are the time-period and duty cycle values. Time-period is not supplied directly but is calculated based on the input clock frequency and the required PWM output frequency. As discussed earlier, the input clock frequency is 50 MHz corresponding to the FPGA onboard clock. The output frequency needs to be high enough so that the voltage that will be generated at the output of the RC stage has less ripples. Considering this, a value of 500 kHz was fixed. The duty cycle is an input that is a bit vector so that it can be controlled using buttons on the FPGA board. The bit vector length is controllable and set to 8 for the simulation. An input of all 0s correspond to 0% duty cycle and all 1s correspond to 100%. The reset and enable are also inputs but have one-bit resolution. The output is also a single bit signal. All the input and output values are defined as *std_logic* or *std_logic_vector*.

Initially, time-period and on-time are calculated as an integer multiple of the input clock period. The decision circuit starts by checking for the clock rising edge and generates a positive output until the required on-time is reached, after which it forces the output to zero till the end of time-period, provided the enable signal is active. Once time-period is reached the count is reset. A flowchart that describes the main process flow of the digital system is shown in Fig. 37. Note that command processing in VHDL is concurrent except inside a process. Some information blocks such and gathering input, calculating values etc. are only represented with directional flow so that the logic can be comprehended easily. At start, the input parameters to the entity are gathered and other parameters necessary for processing further subcircuits are derived based on these inputs. At each rising edge of the input clock, the enable signal value is checked. If the enable is high, then a counter is incremented at rising edge of clock to count the clock cycles. Until the counter value is less than the calculated on-time, the PWM output is set to logic 1. Once the counter value crosses the on-time value, then the PWM output is forced to logic 0, till the counter value reaches the time-period value, at which the counter is reset to default value. Additionally, once the counter starts counting a read lock is activated, using which, further changes in on-time are ignored until the whole time-period has elapsed. The process runs continuously until stopped. Generated output is a digital signal and is converted to analog voltage using a DAC implemented in VHDL-AMS, before it is supplied to the RC stage.

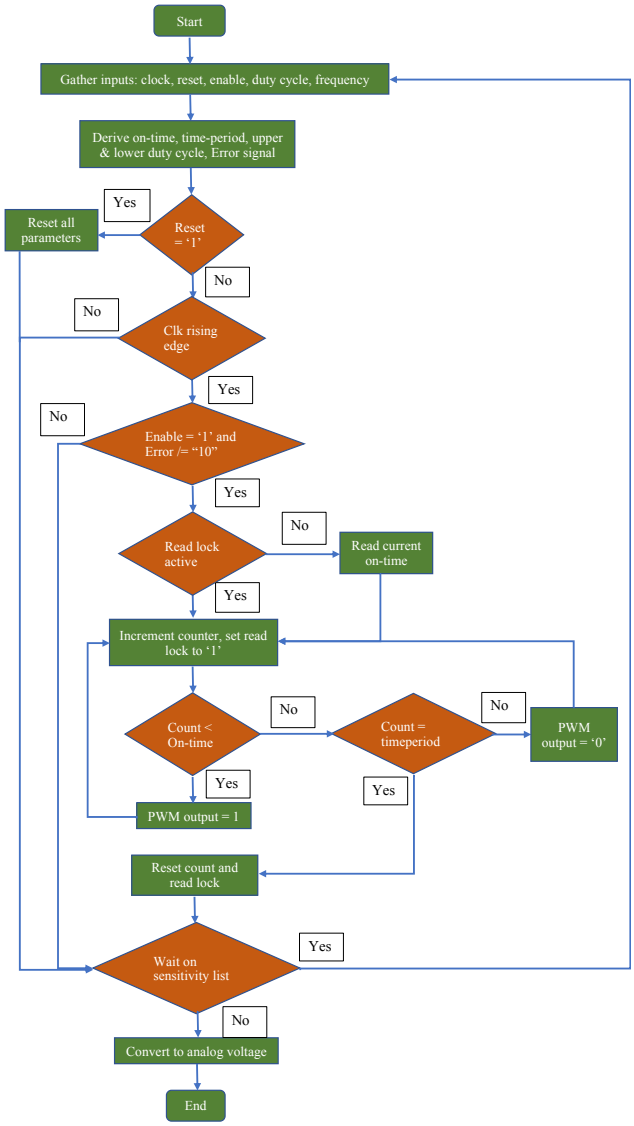

Fig. 37 Flowchart for the implemented digital logic

The implemented logic was verified using the Mentor Graphics Model Sim software where the selected signals can be simulated as waveforms for manual inspection. A testbench code was also created to pass the required inputs to the PWM component. Selected parameters are listed on the left side of the waveform chart and their corresponding state with respect to time (at the bottom) can be observed on right. The code was also complied in Altera Quartus II software and modifications were made to ensure that the code was synthesizable. For example, the input duty cycle change identification using 'event operator had to be replaced with a read lock logic as the mentioned operator's use on a bit vector is not synthesizable. Compilation details and the resource usage from Chip Planner software based on the Cycle III FPGA board are also presented for information in the annex.

C. *Simulation result*

The correctness of the digital logic was first verified through simulation, where each signal in the entire digital block, including the internal signals, were inspected with possible combinations of inputs to ensure its operation was as expected at a given instant of time.

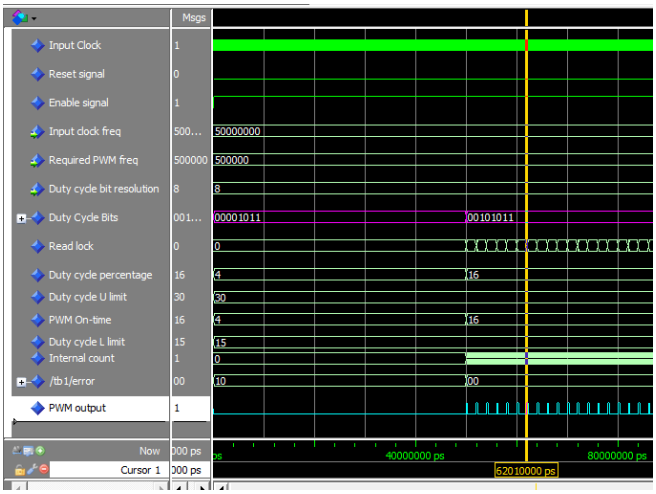

Fig. 38 Simulated output of digital system in Model Sim as waveform

All inputs to the system can be seen in the digital system block diagram. As the input clock frequency and the required PWM frequency are known, they were defined as generics in the VHDL code. They are shown in the Fig. 38. Also, the resolution of the input bit vector which determines the duty cycle was defined as a generic. For the implementation, it was defined as value 8, meaning the duty_cycle input was an 8-bit vector.

The time period for the PWM signal, meaning the sum of on-time and off-time, is calculated as the ratio of clock frequency to PWM frequency. So here the ratio would be 50MHz divided by 500 kHz meaning 100 which is 100 clocks as was observed in the simulated output. Various combinations of input bit vectors were fed to the system and the internal signal values and output was verified. Consider the initial input bit vector "00001011". The duty cycle percentage in the logic was calculated as the decimal value of the bit vector divided by 256 which is 11/256 here, which in turn is 4, as only integers are considered in VHDL. Thus, the on-time is 4% of the total time-period 100, which is value 4 as shown in the simulated result. This formed the first two subcircuits of the system and they provided expected results as the simulated and calculated results matched. As discussed previously, the upper limit and lower limit of the duty cycle are decided based on the voltage range for oscillator which are calculated as:

$$Duty\ cycle\ lower\ limit = \frac{(Min\ voltage\ *\ Timeperiod)}{PWM\ analog\ output\ voltage} \quad (15)$$

$$Duty\ cycle\ upper\ limit = \frac{(Max\ voltage\ *\ Timeperiod)}{PWM\ analog\ output\ voltage} \quad (16)$$

Min voltage and Max voltage are the required voltage limits for the analog system, which is 0.5 V and 1 V. The standard PWM analog voltage is 3.3 V. Hence, for a time-period of 100, the lower (Duty cycle L limit) and upper (Duty cycle U limit) limits to get a voltage range of 0.5 to 1 V calculates to 15 and 30 respectively, which are matched in the simulated results shown in Fig. 38. Since the current duty cycle input only corresponds to an on-time of 4, which is less than the minimum required on-time for the analog system, no output is expected to be generated. The simulated results also confirmed this behavior and shows the error signal vector (/tb1/error) as "10" indicating the error was detected. At time T= 50 µs a new duty cycle was produced which generated an on-time value of 16 which was within the required limits. Hence an output was expected, and again the simulation results indicated the same. The new error signal value is "00" confirming that the on-time was within required range for the given duty cycle input. A constant PWM signal was visible equivalent to width of 16 clock signals which confirmed the implemented logic. Thus, the remaining subcircuit functionalities were also confirmed with this. Additionally, the reliability additions such as enable signal change, read lock verification, counter logic, transition on rising edge of clock signal, and reset signal checks were also made and the simulated results matched the expected behavior. Simulations performed by varying all controllable parameters in the system always produced results that matched the output requirement and hence could produce a reliable PWM signal.

D. *Digital System Modelling*

System level modelling was also performed to check if the operation of the digital logic was as expected and the to ensure the integration with the Digital to Analog Converter would produce the required analog PWM voltage. The model was made in ANSYS Twin Builder. The PWM generation digital block named "my_pwm1" was implemented using the VHDL code that was verified in Model Sim. The clock signal ("clk") and the input bit vector ("duty_cycle_bit") were kept as input ports but the enable and reset signal was internally coded as generics, that could be controlled from the interactive GUI, for the simplicity of modelling. They were modified by clicking on the PWM block as needed. The DAC code was written in VHDL-AMS and was implemented as a separate block "dac1". A clock signal ("clk1") of 50 MHz was set up by

selecting a pre-existing signal generator block from Twin Builder. For the bit vector generation, a separate block named "create_bit_vector1" was created so that different input bit vectors could be supplied, and the changes could be observed. At the output of the DAC a Nature Transformation component was needed to be able to plot the signal arriving at the terminal. The output of the digital system was generated at port "pwm_out" and fed to the DAC through its input port "din". The analog PWM output signal was read out at C2NC terminal. The overall circuit is shown in Fig. 39.

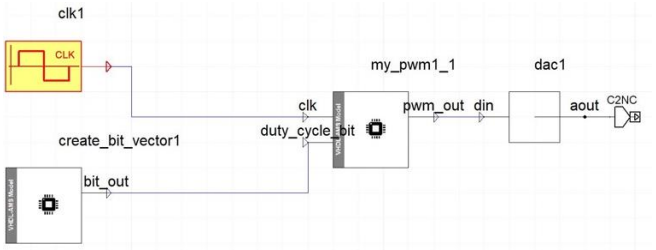

Fig. 39 Modelled digital system in ANSYS Twin Builder

Fig. 40 shows a rectangular plot (for better representation) of the generated analog PWM voltage at the output of the modelled system with respect to the clock signal and the digital PWM output. The y-axis represents the amplitude of the signal and corresponds to different value for each signal. For the clock (my_pwm1.clk), which is defined as BIT value in Twin Builder as it receives BIT values from the predefined clock-signal block, the amplitude changes between 0 and 1. For the PWM digital output (my_pwm1_1.pwm_out) which is defined as std_logic, it varies between 2 and 3 which corresponds to the position of logic 0 and logic 1 in the std_logic values. The analog PWM voltage (C2NC1.OUT) switches between 0 and 3.3 which is the standard voltage considered. Bit vector values like that used in Model Sim simulation were also provided in the Twin Builder Model.

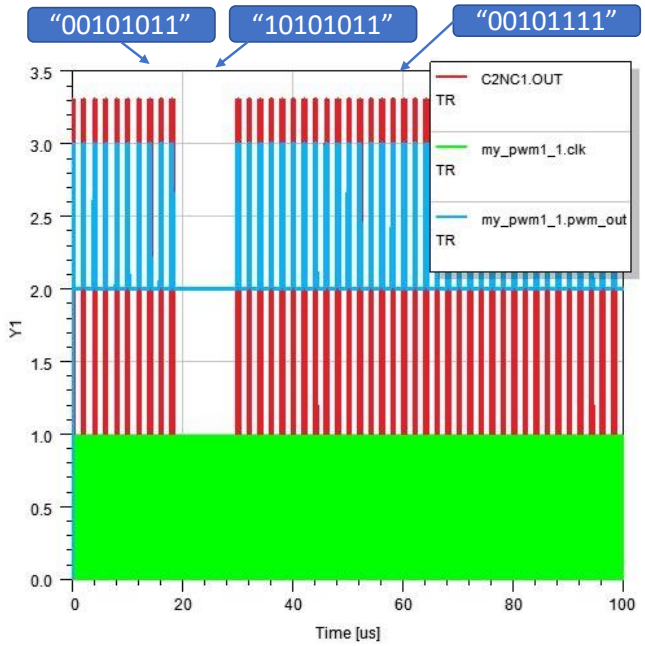

Fig. 40 Output of digital model for different duty cycle input bit vectors

A PWM output was generated when the on-time was within limits and no output was produced when it was outside limits as was the case with vector "10101011". The time-period of 2 µs as shown in the Fig. 41 for the PWM signal confirmed the frequency of 500 kHz and the on-time of 0.32 µs matches the duty cycle of 16% similar to what was discussed in the simulation part. Various combinations of the inputs also produced expected results thus confirming the system as reliable and its integration with the DAC as functional. The digital plot for the same system and the Twin Builder settings are presented in the annex.

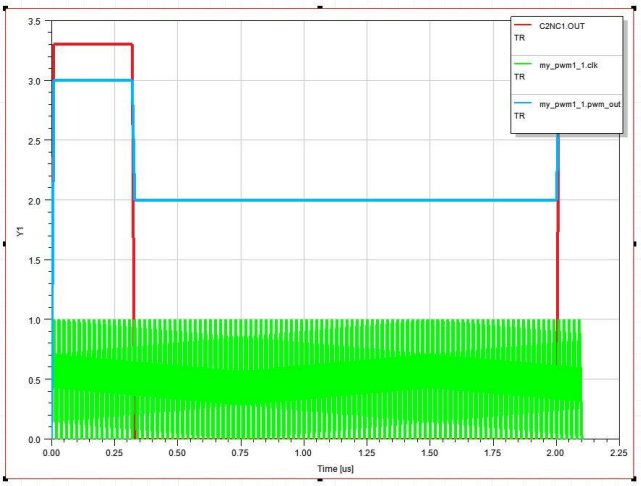

Fig. 41 Enlarged plot of digital model showing the on-time and time-period

E. Digital Design Conclusion

The digital logic was successfully designed and verified to function as the first stage for the overall CMUT transducer system. Programming using VHDL ensured that each input and interface signal could be defined as per requirement and the precision of the output could be verified using simulated timing diagrams. The challenging part was to implement a scalable design where each of the parameters could be updated without affecting the overall logic and to make the system reliable.

V. Conclusion (Whole Project)

A CMUT transducer system was completely designed from root level and successfully implemented over various stages in the project. The project involved the development of three main individual blocks: a digital, analog and micro-electromechanical component. The functioning of these blocks are as follows; digital block will generate a PWM wave which will be the input to the analog block. Later the analog block will generate the pulsating voltage depending on the digital input for implementing displacement of the membrane of the transducer. Finally, the transduces generates the output frequency for further functions. Regarding their implementation several tools were used and many design considerations were made as discussed in the report. Overall, the system was functional and expected results were achieved.

Acknowledgment

The authors would like to thank the faculty members- Ferenc Ender, Péter Pálovics, Gábor Takács and Ali Kareem, of BME Dept. of Electron Device for their constant support for this project.

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