# Design Rules Verification Report

Filename : C:\Github\RP2040_PCB\PCB\RP2040.PcbDoc

Warnings 0
Rule Violations 6

| Warnings | |
|---|---|
| Total | 0 |

| Rule Violations | |
|---|---|
| Clearance Constraint (Gap=0.229mm) (All),(All) | 0 |
| Short-Circuit Constraint (Allowed=No) (All),(All) | 0 |
| Un-Routed Net Constraint ( (All) ) | 0 |
| Modified Polygon (Allow modified: No), (Allow shelved: No) | 0 |
| Width Constraint (Min=0.025mm) (Max=2.54mm) (Preferred=0.254mm) (All) | 0 |
| Power Plane Connect Rule(Relief Connect )(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm) | 0 |
| Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All) | 0 |
| Hole To Hole Clearance (Gap=0.254mm) (All),(All) | 0 |
| Minimum Solder Mask Sliver (Gap=0.216mm) (All),(All) | 6 |
| Silk To Solder Mask (Clearance=0.178mm) (IsPad),(All) | 0 |
| Silk to Silk (Clearance=0.254mm) (All),(All) | 0 |
| Net Antennae (Tolerance=0mm) (All) | 0 |
| Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All) | 0 |
| Total | 6 |

| Minimum Solder Mask Sliver (Gap=0.216mm) (All),(All) |
|---|
| Minimum Solder Mask Sliver Constraint: (0.047mm < 0.216mm) Between Pad J2-1(25.954mm,45.814mm) on Top Layer And Pad |
| Minimum Solder Mask Sliver Constraint: (0.072mm < 0.216mm) Between Pad J2-1(25.954mm,45.814mm) on Top Layer And Pad |
| Minimum Solder Mask Sliver Constraint: (0.047mm < 0.216mm) Between Pad J2-2(25.304mm,45.814mm) on Top Layer And Pad |
| Minimum Solder Mask Sliver Constraint: (0.047mm < 0.216mm) Between Pad J2-3(24.654mm,45.814mm) on Top Layer And Pad |
| Minimum Solder Mask Sliver Constraint: (0.047mm < 0.216mm) Between Pad J2-4(24.004mm,45.814mm) on Top Layer And Pad |
| Minimum Solder Mask Sliver Constraint: (0.072mm < 0.216mm) Between Pad J2-5(23.354mm,45.814mm) on Top Layer And Pad |

Extra Room Definitions

| Schematic Object | PCB Object |
| --- | --- |
| [Room RP2040 (Scope=InComponentClass('RP2040')) TopLayer] | |