

DFM analysis report_JLCDFM

File name :

easygate-gerber

Report generated at :

2024-10-10 17:29:56

PCB layers :

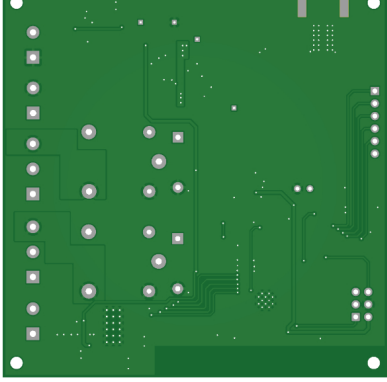
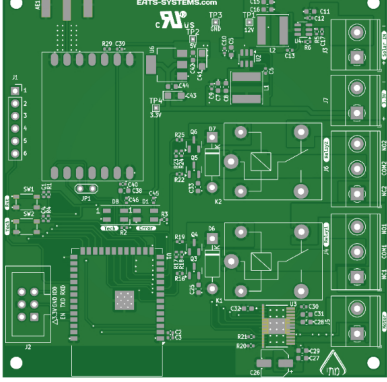
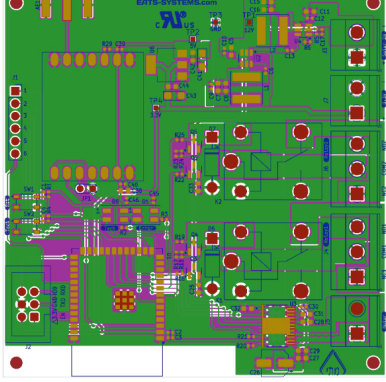
2

PCB size :

7.79x7.85cm

Analyze project :

☒PCB DFM ☐SMT DFM



PCB DFM>Routing layer analysis

Analyze project	Analysis results	PCB screenshot	Layer distribution	Statistics
Sharp trace corner (Check for sharp corners in traces)	No	No	No	Danger: 0 Warning: 0 Good: 0
BGA pad (Check BGA pads on the board)	No	No	No	Danger: 0 Warning: 0 Good: 0
Via placed within a pad (Check if there is a via placed within a pad)	No	No	No	Danger: 0 Warning: 0 Good: 0
Trace to board edge (Detect traces too close to the board edge)	No	No	No	Danger: 0 Warning: 0 Good: 0
Trace spacing (Measure spacing between adjacent parallel traces)	0.15mm Good		EasyGate-F_Cu.gbr	Danger: 0 Warning: 0 Good: 8
Unconnected trace end (Free-standing trace ends not connected to pads)	No	No	No	Danger: 0 Warning: 0 Good: 0
Trace width (Trace width information)	0.2mm Good		EasyGate-F_Cu.gbr EasyGate-B_Cu.gbr	Danger: 0 Warning: 0 Good: 100
Fiducial (Detect fiducial marks on the board)	No	No	No	Danger: 0 Warning: 0 Good: 0
Pad to board edge (Measure distance of pads from the board edge)	No	No	No	Danger: 0 Warning: 0 Good: 0
Pad spacing (Measure pad to pad spacing)	0.1mm Warning		EasyGate-F_Cu.gbr EasyGate-B_Cu.gbr	Danger: 0 Warning: 2 Good: 52
Plated through-hole to trace clearance (Measure clearance of plated through-holes to traces)	0.25mm Good		EasyGate-F_Cu.gbr EasyGate-B_Cu.gbr	Danger: 0 Warning: 0 Good: 18
Annular ring (Annular ring width of pads compared to holes)	0.15mm Warning		EasyGate-F_Cu.gbr EasyGate-B_Cu.gbr	Danger: 0 Warning: 100 Good: 0
tht to smd (Detect clearance of vias to pads)	1.1mm Danger		EasyGate-F_Cu.gbr	Danger: 16 Warning: 14 Good: 20
Via to pad (Detect clearance of vias to pads)	0mm Danger		EasyGate-F_Cu.gbr	Danger: 50 Warning: 0 Good: 0

PCB DFM>Soldermask layer analysis

Analyze project	Analysis results	PCB screenshot	Layer distribution	Statistics
Soldermask bridge (Detect distance between parallel soldermask opening edges)	No	No	No	Danger: 0 Warning: 0 Good: 0
Solder mask opening exposing trace (Detect clearance of solder mask openings to nearby traces)	0.03mm Danger		EasyGate-F_Mask.gbr EasyGate-B_Mask.gbr	Danger: 2 Warning: 12 Good: 3
Soldermask opening with multiple segments (Check if solder mask openings are constructed from multiple geometric shapes)	null Warning		EasyGate-F_Mask.gbr	Danger: 0 Warning: 8 Good: 0
Negative soldermask expansion (Detect solder mask openings smaller than their corresponding pads)	No	No	No	Danger: 0 Warning: 0 Good: 0

PCB DFM>Silkscreen layer analysis

Analyze project	Analysis results	PCB screenshot	Layer distribution	Statistics
Silkscreen to pad (Detect clearance of silkscreen to pads)	0.24mm Good		EasyGate-F_Silkscreen.gbr	Danger: 0 Warning: 0 Good: 25
Silkscreen to hole (Detect clearance of silkscreen to holes)	0mm Danger		EasyGate-F_Silkscreen.gbr	Danger: 50 Warning: 0 Good: 0
Silkscreen line width (Check silkscreen line width)	0.1mm Danger		EasyGate-F_Silkscreen.gbr	Danger: 4 Warning: 46 Good: 0

PCB DFM>Drill layer analysis

Analyze project	Analysis results	PCB screenshot	Layer distribution	Statistics
Missing plated through-hole (Detect top and bottom pads at the same location without plated through-holes)	null Warning		EasyGate-F_Cu.gbr	Danger: 0 Warning: 2 Good: 0
Plated through-hole spacing (Measure spacing between plated through-holes)	No	No	No	Danger: 0 Warning: 0 Good: 0
Short slot detection (Detect slots shorter than twice their width)	No	No	No	Danger: 0 Warning: 0 Good: 0
Slot width check (Measure slot width)	No	No	No	Danger: 0 Warning: 0 Good: 0
Via to PTH spacing (Measure spacing of vias to plated through-holes)	No	No	No	Danger: 0 Warning: 0 Good: 0
Unconnected via (Detect isolated unconnected vias)	null Warning		EasyGate-PTH.drl	Danger: 0 Warning: 50 Good: 0