VERIFICATION OF LOGIC GATES

AIM:

To verify the truth table of all logic gates using verilog HDL

APPARATUS REQUIRED:

- PC with windows
- Xilinx 14.7

PROCEDURE:

- Open New project and type the project name and check the top level source type as HDL
- Enter the device properties and click Next
- Click New Source And Select the Verilog Module and then give the file name
- Give the Input and Output port names and click finish
- Type the Verilog program and save it
- Double click the synthesize XST and check syntax for any errors.
- Once error is cleared, choose simulation and add verilog test fixture program.
- Alter the input values accordingly for different times and run the simulate behavioral model.

VERILOG PROGRAM USING GATE LEVEL MODLING:

```
module gates (…….);
input ……;
output ……..;
.
.
.
endmodule
```

VERILOG PROGRAM USING DATA FLOW MODLING:

```
module gates (…….);
input ……;
output ……..;
.
.
.
endmodule
```

VERILOG TEST FIXTURE:

```
initial begin
// Initialize Inputs
a = 0;
b = 0;
#100;
a = 0;
b = 1;
#100;
a = 1;
b = 0;
#100;
a = 1;
b = 1;
#100;
end
```

SIMULATION OF LOGIC GATES:

RESULT:

Thus the simulation of basic logic gates using verilog HDL has been done successfully.