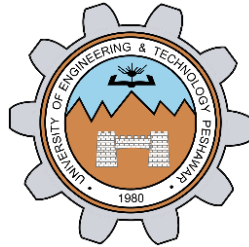


VERIFICATION OF KIRCHHOFF'S VOLTAGE LAW (KVL)
USING BREADBOARD

LAB # 05



Spring 2023 CSE103L Circuits & Systems-I Lab

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“On my honor, as student of University of Engineering and Technology, I have neither given nor received unauthorized assistance on this academic work.”

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KIRCHHOFF'S VOLTAGE LAW(KVL):

It is a fundamental law in electrical circuits that states that the sum of the voltage drops around any closed loop in a circuit must be equal to zero. This means that the voltage supplied by a battery or other voltage source must equal the voltage drops across all the circuit elements, such as resistors and capacitors, in the loop.

Explanation:

KVL is based on the principle of energy conservation. When a charged particle moves through a circuit element, such as a resistor, it loses energy in the form of heat, which is equivalent to a voltage drop across the element. Similarly, when a charged particle moves across a battery or other voltage source, it gains energy, which is equivalent to a voltage rise. KVL states that the total energy gained by a particle as it moves around a closed loop in the circuit must be equal to the total energy lost, so that the net energy change is zero.

Example:

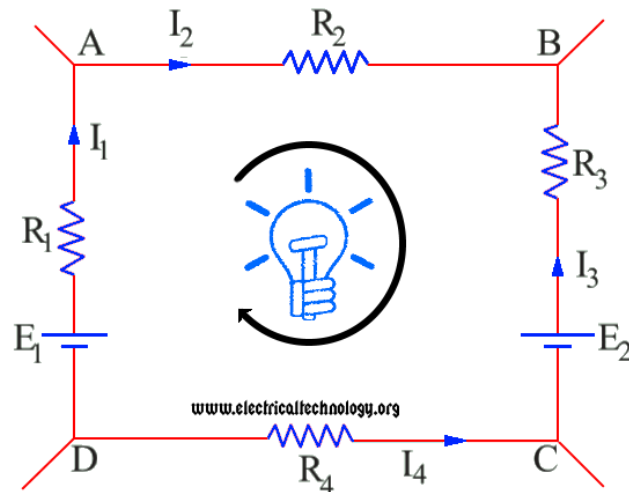
For example, consider a simple circuit consisting of a battery, a resistor, and a switch, connected in series. When the switch is closed, current flows through the circuit and the voltage drop across the resistor is equal to the voltage supplied by the battery. This follows from KVL, which states that the sum of the voltage drops around the loop must be equal to zero. If the battery supplies a voltage of 5 volts and the resistor has a resistance of 1 ohm, the current flowing through the circuit is 5 amps, and the voltage drop across the resistor is also 5 volts. Thus, KVL is satisfied: 5 volts - 5 volts = 0 volts.

OBJECTIVE:

Define Kirchhoff's Voltage Law.

1. Discuss how Kirchhoff's Voltage Law applies to Series and Parallel Circuits.
2. Analyze the circuit and circuit elements.
3. How to make a circuit diagram to verify Kirchhoff's voltage law.

CIRCUIT DIAGRAM:



$$E_1 - E_2 = I_1 R_1 + I_2 R_2 - I_3 R_3 - I_4 R_4$$

Kirchhoff's Voltage Law (KVL)

MATHEMATICAL EXPRESSION:

$$V_{AB} + V_{BC} + V_{CD} + V_{DA} = 0$$

APPARATUS:

- Breadboard
- Resistors of different values
- DC power supply
- Digital multimeter (DMM)
- Connecting wires

PROCEDURE:

- The procedure to verify KVL on a breadboard is as follows:
- Set up the breadboard with the resistors and connecting wires as per your circuit design.
- Connect the DC power supply to the breadboard.
- Use the DMM to measure the voltage across each resistor.
- Starting from any point in the circuit, follow the loop in the circuit and add the voltage drops across each resistor in the loop. The sum of the voltage drops should equal the applied voltage from the power supply.
- Repeat step 4 for all loops in the circuit.
- If the sum of the voltage drops in each loop equals the applied voltage from the power supply, then KVL is verified in the circuit.

Note: Make sure to set the DMM to the appropriate voltage range and connect it in parallel with the resistor to measure the voltage drop. Also, double-check all connections before applying power to the circuit

OBSERVATIONS AND CALCULATIONS:

USING TWO RESISTORS:

S. No	V	V _m	V ₁	V ₂	Error=V _m (V ₁ +V ₂)
1.	5V	5.61	2.75	2.73	0.13V
2.	10V	10.01	5.29	5.38	0.24V
3.	15V	16.53	8.14	8.06	0.33V

USING THREE RESISTORS:

S. No	V	V _m	V ₁	V ₂	V ₃	Error=V _m -(V ₁ +V ₂ +V ₃)
1.	5V	5.61	2.59	2.52	0.25	0.15
2.	10V	10.91	5.15	5.09	0.49	0.18
3.	15V	16.53	7.86	7.76	0.75	0.16

ANALYSIS:

Kirchhoff's Voltage Law (KVL) states that the sum of all voltages around a closed loop in a circuit must equal zero. This means that the voltage drops across all the circuit elements in the loop must add up to the voltage source(s) in the loop.

The aim of verifying KVL using a breadboard is to demonstrate the validity of this law in a practical circuit using simple electronic components. The breadboard is a tool used for prototyping and testing electronic circuits. It provides a platform for connecting components together without the need for soldering.

In conclusion, verifying Kirchhoff's Voltage Law using a breadboard is a simple and effective way to demonstrate the law in a practical circuit using simple electronic components. It provides a hands-on approach to learning and understanding the fundamental principles of circuit analysis.

LAB RUBRICS: (Circuits & Systems-I Lab)

Criteria & Point Assigned	Outstanding 4	Acceptable 3	Considerable 2	Below Expectations 1
Attendance and Attentiveness in Lab PLO10	Attended in proper Time and attentive in Lab	Attended in proper Time but not attentive in Lab	Attended late but attentive in Lab	Attended late not attentive in Lab
Equipment / Instruments Selection and Operation PLO1, PLO2, PLO3, PLO5,	Right selection and operation of appropriate equipment and instruments to perform experiment.	Right selection of appropriate equipment and instruments to perform experiment but with minor issues in operation	Needs guidance for right selection of appropriate equipment and instruments to perform experiment and to overcome errors in operation	Cannot appropriately select and operate equipment and instruments to perform experiment.
Result or Output/ Completion of target in Lab PLO9,	100% target has been completed and well formatted.	75% target has been completed and well formatted.	50% target has been completed but not well formatted.	None of the outputs are correct
Overall, Knowledge PLO10,	Demonstrates excellent knowledge of lab	Demonstrates good knowledge of lab	Has partial idea about the Lab and procedure followed	Has poor idea about the Lab and procedure followed
Attention to Lab Report PLO4,	Submission of Lab Report in Proper Time i.e. in next day of lab., with proper documentation.	Submission of Lab Report in proper time but not with proper documentation.	Late Submission with proper documentation.	Late Submission Very poor documentation

