TITLE: VERIFICATION OF NODEL ANALYSIS METHOD

LAB # 07

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CSE103L Circuits & Systems-I Lab

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"On my honor, as student of University of Engineering and Technology, I have neither given nor received unauthorized assistance on this academic work."

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Submitted to:

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OBJECTIVE

The objective of the "verification of node voltage method" is to validate the accuracy and correctness of the node voltage method as a technique for solving electrical circuits. The node voltage method, also known as the nodal analysis method, is a systematic approach used to analyze and solve electrical circuits by considering the voltages at various nodes in the circuit.

In detail, the verification of the node voltage method involves the following objectives:

Validation of Circuit Analysis: The primary goal is to verify that the node voltage method provides accurate and reliable results when applied to different types of electrical circuits. By comparing the results obtained using the node voltage method with other established methods or known solutions, the accuracy of the method can be assessed.

Assessment of Circuit Complexity: The verification process aims to determine the effectiveness of the node voltage method for circuits of varying complexity. This involves applying the method to circuits with different numbers of nodes, branches, and voltage/current sources to assess its scalability and efficiency in handling complex circuit configurations.

Comparison with Alternative Methods: Another objective is to compare the node voltage method with alternative circuit analysis techniques, such as mesh analysis or superposition, to evaluate its advantages and disadvantages. This allows for a comprehensive understanding of the strengths and limitations of the node voltage method in comparison to other methods.

Evaluation of Numerical Stability: The verification process also includes investigating the numerical stability of the node voltage method. This involves assessing the method's performance when dealing with circuits that may exhibit sensitivity to numerical errors, such as circuits with high gain or feedback.

Analysis of Convergence and Convergence Criteria: The node voltage method requires an iterative approach to solve circuits, and convergence of the iterative process is essential. The objective is to examine the convergence behavior of the method and establish appropriate convergence criteria to ensure accurate and efficient circuit analysis.

Identification of Limitations and Constraints: The verification process aims to identify any limitations or constraints associated with the node voltage method. This includes understanding situations where the method may not be applicable or may yield inaccurate results, such as circuits with nonlinear elements or circuits with significant mutual inductance.

By achieving these objectives, the verification of the node voltage method provides a thorough assessment of its reliability, accuracy, applicability, and limitations. It helps establish confidence in the method's usage and guides engineers and researchers in determining when and how to apply the node voltage method for solving electrical circuits.

Steps:

Step 1: Identify and label the nodes:

Identify the nodes in the circuit. Nodes are the points where three or more circuit elements are connected. Assign a label or a variable to each node. Typically, one node is chosen as the reference node (usually the one with the lowest number) and assigned a reference voltage of 0V.

Step 2: Write Kirchhoff's current law (KCL) equations:

At each non-reference node, write a KCL equation in terms of the currents flowing into or out of the node. KCL states that the sum of currents entering a node is equal to the sum of currents leaving the node. Express the currents in terms of the node voltages using Ohm's law (V = IR) and the given circuit elements.

Step 3: Solve the KCL equations:

Solve the system of KCL equations to obtain a set of simultaneous equations in terms of the node voltages. The number of equations will be equal to the number of non-reference nodes in the circuit.

Step 4: Express the equations in matrix form:

Write the set of simultaneous equations in matrix form. Create a coefficient matrix (A) by extracting the coefficients of the node voltages from the equations. Create a column matrix (V) containing the unknown node voltages. Create a column matrix (I) containing the current sources or current-dependent voltage sources in the circuit.

Step 5: Solve the matrix equation:

Solve the matrix equation A * V = I for the column matrix V. This can be done by inverting the coefficient matrix A and multiplying it by the column matrix I: V = A^(-1) * I.

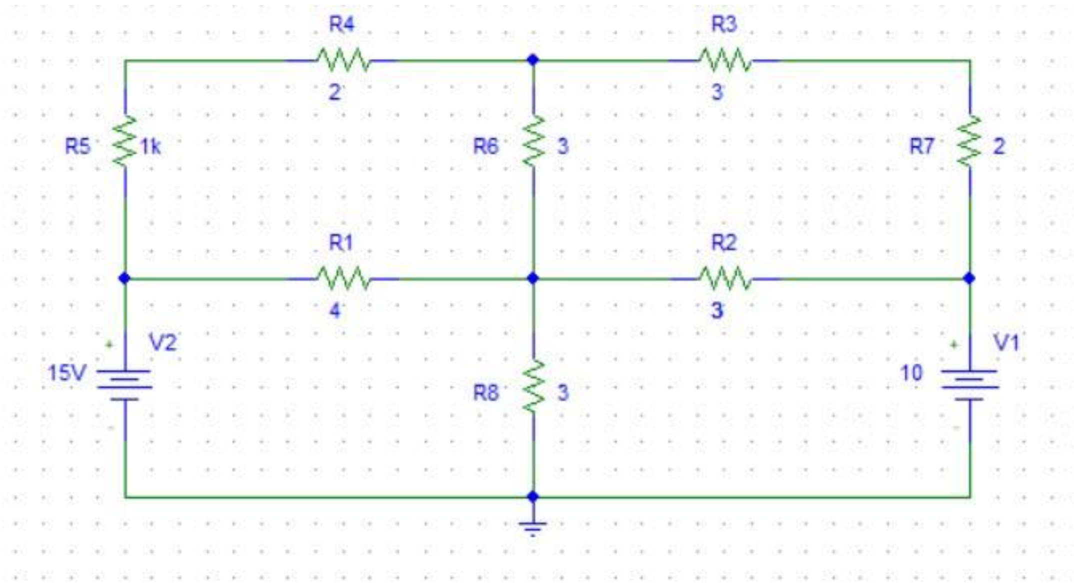
Step 6: Calculate the remaining currents or voltages:

Using the solved node voltages, calculate the currents or voltages of interest in the circuit. This can be done using Ohm's law and the known circuit elements.

Step 7: Verify the solution:

Check if the obtained node voltages satisfy the KCL equations. The sum of currents entering a node should be equal to the sum of currents leaving the node.

Circuit diagram:



Finding the Values Using Node Voltage Method:

We will use node voltage method to find the unknown values of the voltages in the circuit.

We have two equations:

$$\frac{Vb - 15}{3} + \frac{Vb - 10}{5} + \frac{Vb - Vd}{3} = 0 \text{ ---------------- } (1)$$

$$\frac{Vd - 15}{4} + \frac{Vd - 10}{3} + \frac{Vd - Vb}{3} = 0 \text{------------------ } (2)$$

Equation (1):

$5 \quad (Vb - 15) + 3\,(Vb - 10) + 5\,(Vb - Vd) = 0$

$5Vb - 75 + 3Vb - 30 + 5Vb - 5Vd = 0$

$13Vb - 5Vd - 105 = 0$ -------------- (3)

Equation (2):

$3\,(Vd - 15) + 4\,(Vd - 10) + 4Vd + 4\,(Vd - Vb) = 0$

$15Vd - 4Vb - 85 = 0$ --------------- (4)

Multiplying equation (3) with 3 and then adding with equation (4)

$\cancel{-15Vd} + 39Vb - 315 = 0$

$\underline{\cancel{-15Vd} - 4Vb - 85 = 0}$

$35Vb - 400 = 0$

$Vb = 11.42$

Put in equation (4)

$15Vd - 4\,(11.42) - 85 = 0$

$Vd = 8.712$

LAB RUBRICS: (Circuits & Systems-I Lab)

Criteria & Point Assigned	Outstanding 4	Acceptable 3	Considerable 2	Below Expectations 1
Attendance and Attentiveness in Lab PLO10	Attended in proper Time and attentive in Lab	Attended in proper Time but not attentive in Lab	Attended late but attentive in Lab	Attended late not attentive in Lab
Equipment / Instruments Selection and Operation PLO1, PLO2, PLO3, PLO5,	Right selection and operation of appropriate equipment and instruments to perform experiment.	Right selection of appropriate equipment and instruments to perform experiment but with minor issues in operation	Needs guidance for right selection of appropriate equipment and instruments to perform experiment and to overcome errors in operation	Cannot appropriately select and operate equipment and instruments to perform experiment.
Result or Output/ Completion of target in Lab PLO9,	100% target has been completed and well formatted.	75% target has been completed and well formatted.	50% target has been completed but not well formatted.	None of the outputs are correct
Overall, Knowledge PLO10,	Demonstrates excellent knowledge of lab	Demonstrates good knowledge of lab	Has partial idea about the Lab and procedure followed	Has poor idea about the Lab and procedure followed
Attention to Lab Report PLO4,	Submission of Lab Report in Proper Time i.e. in next day of lab., with proper documentation.	Submission of Lab Report in proper time but not with proper documentation.	Late Submission with proper documentation.	Late Submission Very poor documentation