DESIGNING OF SR FLIP-FLOP USING SKY130 Technology

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30th Jan, 2022

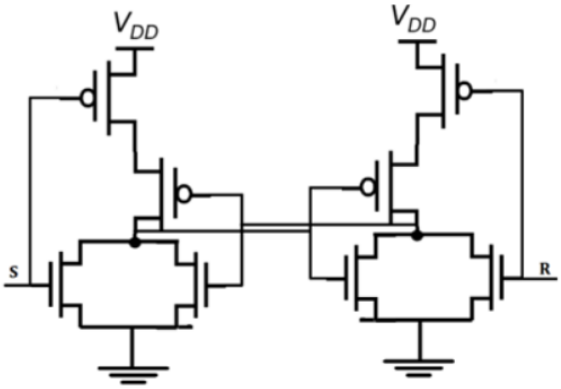
Abstract

In VLSI, digital circuit with low power design is the widely used. The expected circuit diagram and waveform of low power and high speed SR flip flop using CMOS technology is shown. Flip-flop is the primary place of memory elements to use on any portable device, a wide attention to reduce energy consumption flip-flop will help reducing energy consumption in a large IC. In this paper, we will be designing a flip-flop with CMOS logic; It consumes less energy than conventional gates designed. Switching transistors occurs when applied input clock is applied. The proposed SR flip flop will be designed in Esim and implemented using 130 nm in SkyWater Technology.

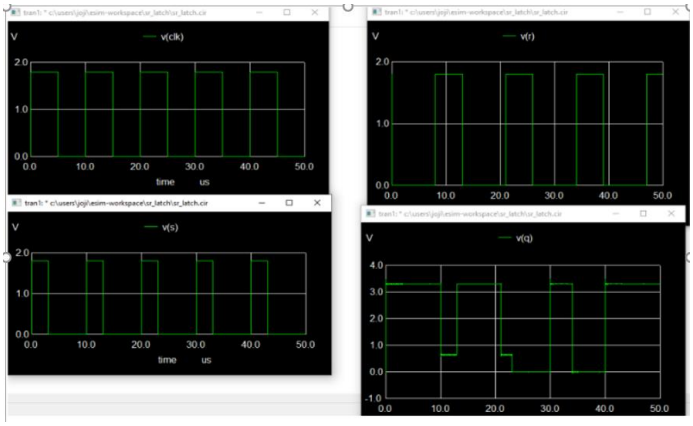
Circuit Details

The SR flip-flop is the most basic sequential logic circuit known as SR Latch. The term “Flip-flop” relates to the actual operation of the device, as it can be “flipped” into one logic Set state or “flopped” back into the opposing logic Reset state. The SR flip flop has 2 inputs (Set and Reset). The output Q is high when the set input is high and reset is low. The converse is also true. Q=0 for S=0 & R=1; and the flip-flop is in reset state. If S=R=0; there is no change in the state of the flip-flop. S=R=1 is invalid condition.

If the S is equal to V_{OH} and the R is equal to V_{OL}, both of the parallel-connected transistors M1 and M2 will be ON. The voltage on node $Q^{----}Q^{-}$ will assume a logic-low level of V_{OL} = 0. At the same time, both M3 and M4 are turned off, which results in a logic-high voltage V_{OH} at node Q. If the R is equal to V_{OH} and the S is equal to V_{OL}, M1 and M2 turned off and M3 and M4 turned on.



Expected Circuit Diagram [1]



Expected Waveform [2]

References

[1]VLSI Design - Sequential MOS Logic Circuits (tutorialspoint.com)
[2]https://esim.fossee.in/hackathon/completed-circuits (Joji Jose, Government Engineering College, Idukki)