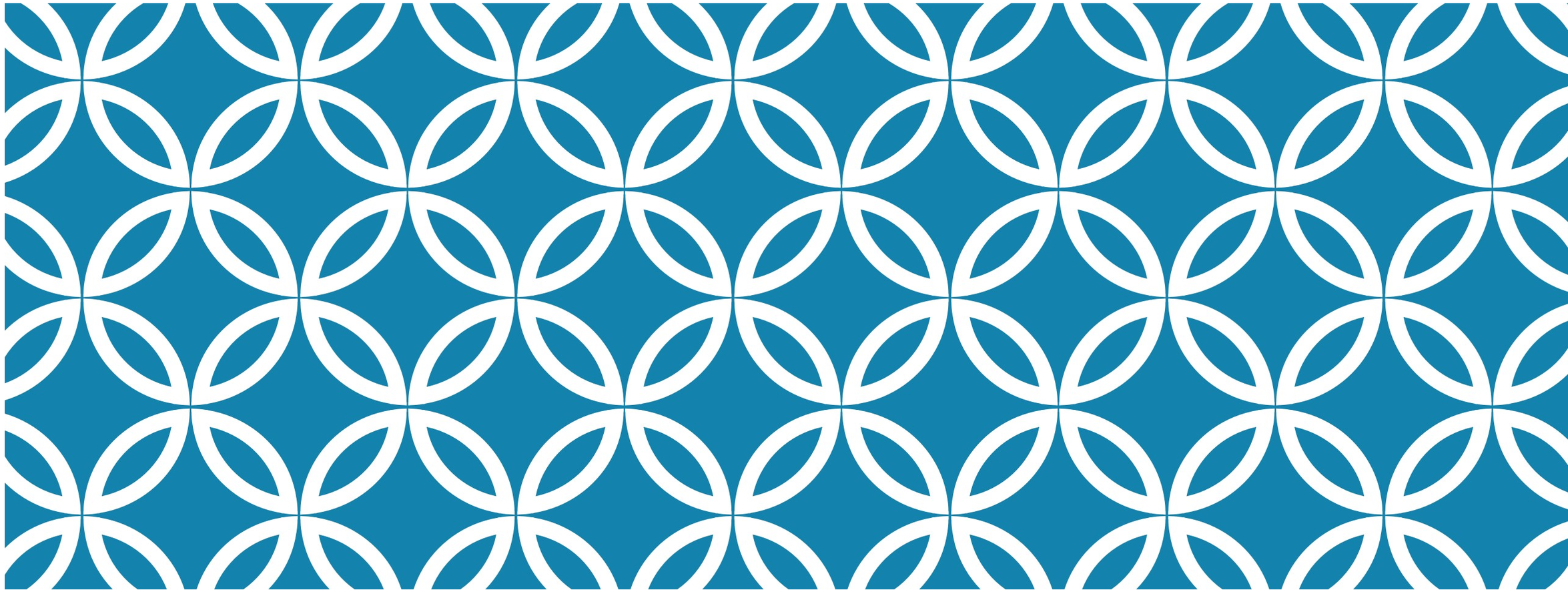

LOGICAL INSTRUCTIONS

15ECE304 Micro Processor & Micro Controller

This group of instructions performs logical operations on data in registers and memory. All status flags are affected by these instructions with some exceptions.

ANA r -- AND the contents of accumulator with that of specified register.

Mnemonic	Operands	Description
ANA	r	• Performs A = A AND r • CY is RESET & AC is SET and all other flags are modified as per standard

EXAMPLE ANA B A = 87h B = 12h

		8	7	6	5	4	3	2	1	0	Status Flags				
A	87 H		1	0	0	0	0	1	1	1					
B	12 H		0	0	0	1	0	0	1	0					
CY											Z	S	P	CY	AC
AND	**02 H**		**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**1**

ANI 8 Bit Data -- AND Immediate 8 bit data with accumulator

Mnemonic	Operands	Description
ANI	Data	• A = A AND Data • CY is RESET & AC is SET and all other flags are modified as per standard

EXAMPLE ANI 46 h A = 87h Data = 46 h

		8	7	6	5	4	3	2	1	0	Status Flags				
A	87 H		1	0	0	0	0	1	1	1					
Data	46 H		0	1	0	0	0	1	1	0					
CY											Z	S	P	CY	AC
AND	**06 H**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**0**	**0**	**0**	**1**	**0**	**1**

XRA r -- XOR contents of A with r

Mnemonic	Operands	Description
XRA	r	• A = A XOR r • CY & AC are cleared to '0' & remaining flags are modified as per standard

EXAMPLE XRA B A = 87h B = 12 h

		8	7	6	5	4	3	2	1	0	Status Flags				
A	87 H		1	0	0	0	0	1	1	1					
B	12 H		0	0	0	1	0	0	1	0					
CY											Z	S	P	CY	AC
XOR	**95 H**		**1**	**0**	**0**	**1**	**0**	**1**	**0**	1	**0**	**1**	**1**	**0**	**0**

XRI 8 Bit Data -- XOR Immediate 8-bit data with accumulator

Mnemonic	Operands	Description
XRI	Data	• A = A XOR Data • CY & AC are cleared to '0' & remaining flags are modified as per standard

EXAMPLE XRI 46 h A = 87h Data = 46 h

		8	7	6	5	4	3	2	1	0	Status Flags				
A	87 H		1	0	0	0	0	1	1	1					
Data	46 H		0	1	0	0	0	1	1	0					
CY											Z	S	P	CY	AC
XOR	**C1 H**	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**1**	**0**	**0**	**0**

ORA r -- OR the contents of accumulator with that of register.

Mnemonic	Operands	Description
ORA	r	• A = A OR r • CY & AC are cleared to '0' & remaining flags are modified as per standard

EXAMPLE ORA B A = 87h B = 12h

		8	7	6	5	4	3	2	1	0	Status Flags				
A	87 H		1	0	0	0	0	1	1	1					
B	12 H		0	0	0	1	0	0	1	0					
CY											Z	S	P	CY	AC
OR	**97 H**		**1**	**0**	**0**	**1**	**0**	**1**	**1**	**1**	**0**	**1**	**0**	**0**	**0**

ORI 8 Bit Data -- OR Immediate 8-bit data with accumulator

Mnemonic	Operands	Description
ORI	Data	• A = A OR Data • CY & AC are cleared to '0' & remaining flags are modified as per standard

EXAMPLE ORI 46 h A = 87h Data = 46 h

		8	7	6	5	4	3	2	1	0	Status Flags				
A	87 H		1	0	0	0	0	1	1	1					
Data	46 H		0	1	0	0	0	1	1	0					
CY											Z	S	P	CY	AC
OR	**C7 H**	**0**	**1**	**1**	**0**	**0**	**0**	**1**	**1**	**1**	**0**	**1**	**0**	**0**	**0**

CMP r -- Compare the contents of accumulator with r

Mnemonic	Operands	Description
CMP	r	• A + 2's Comp r • Result is not stored anywhere • if (A) < (r/mem): carry flag is set • if (A) = (r/mem): zero flag is set • if (A) > (r/mem): carry and zero flags are reset

EXAMPLE CMP B A = 44 h B = 13 h 2's Comp B = ED h

		8	7	6	5	4	3	2	1	0	Status Flags				
A	44 H		0	1	0	0	0	1	0	0					
B	ED H		1	1	1	0	1	1	0	1					
CY											Z	S	P	CY	AC
ADD	**A > B**	1	0	0	1	1	0	0	0	1	**0**	**0**	**0**	**0**	**1**

CPI 8 Bit Data -- Compare Immediate 8-bit data with accumulator

Mnemonic	Operands	Description
CPI	Data	• A + 2's Comp Data • Result is not stored anywhere • if (A) < (Data): carry flag is set • if (A) = (Data): zero flag is set • if (A) > (Data): carry and zero flags are reset

EXAMPLE CPI 13h A = 44 h Data = 13 h 2's Comp Data = ED h

		8	7	6	5	4	3	2	1	0	Status Flags				
A	44 H		0	1	0	0	0	1	0	0					
B	ED H		1	1	1	0	1	1	0	1					
CY											Z	S	P	CY	AC
ADD	**A > B**	1	0	0	1	1	0	0	0	1	**0**	**0**	**0**	**0**	**1**

RLC -- Rotate Left Circular Accumulator

Mnemonic	Operands	Description
RLC		• A = A << 1 • 7th bit is copied to both CY & 0th bit • Only CY is affected.

EXAMPLE RLC A = 87h

		8	7	6	5	4	3	2	1	0	Status Flags				
A	87 H		1	0	0	0	0	1	1	1					
											Z	S	P	CY	AC
Rotate	**0F H**		**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**NA**	**NA**	**NA**	**1**	**NA**

RAL -- Rotate Accumulator left through carry

Mnemonic	Operands	Description
RAL		• A = A << 1 • 7th bit is copied to CY • CY is copied to 0th bit. • Only CY is affected.

EXAMPLE RAL A = 87h CY = 0

		8	7	6	5	4	3	2	1	0	Status Flags				
A	87 H		1	0	0	0	0	1	1	1					
CY											Z	S	P	CY	AC
Rotate	**0E H**		**0**	**0**	**0**	**0**	**1**	**1**	**1**	**0**	**NA**	**NA**	**NA**	**1**	**NA**

RRC -- Rotate Accumulator right circular

Mnemonic	Operands	Description
RRC		• A = A >> 1 • 0^{th} bit is copied to both CY & 7th bit • Only CY is affected

EXAMPLE RRC B A = 87h

		8	7	6	5	4	3	2	1	0	Status Flags				
A	87 H		1	0	0	0	0	1	1	1					
CY											Z	S	P	CY	AC
Rotate	**C3 H**		**1**	**1**	**0**	**0**	**0**	**0**	**1**	**1**	**NA**	**NA**	**NA**	**1**	**NA**

RAR -- Rotate Accumulator Right through Carry

Mnemonic	Operands	Description
RAR		• A = A >> 1 • 0^{th} bit is copied to CY • CY is copied to 7^{th} bit. Only CY is affected

EXAMPLE RAR A = 87h CY = 0

		8	7	6	5	4	3	2	1	0	Status Flags				
A	87 H		1	0	0	0	0	1	1	1					
CY											Z	S	P	CY	AC
Rotate	**43 H**		**0**	**1**	**0**	**0**	**0**	**0**	**1**	**1**	**NC**	**NC**	**NC**	1	**NC**

CMA -- Complement Accumulator

Mnemonic	Operands	Description
CMA		• A = Not A • None of flags are affected

EXAMPLE CMA A = 87 h

		8	7	6	5	4	3	2	1	0	Status Flags				
A	87 H		1	0	0	0	0	1	1	1					
CY											Z	S	P	CY	AC
NOT	**78 H**		**0**	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**NC**	**NC**	**NC**	NC	**NC**

STC -- Set Carry Flag

Mnemonic	Operands	Description
STC		• CY = 1 • None of flags are affected

EXAMPLE STC CY = X

		8	7	6	5	4	3	2	1	0	Status Flags				
CY	X										Z	S	P	CY	AC
NOT											**NC**	**NC**	**NC**	1	**NC**

CMC -- Complement Carry Flag

Mnemonic	Operands	Description
CMC		• CY = Not CY • None of flags are affected

EXAMPLE CMC CY = 1

		8	7	6	5	4	3	2	1	0	Status Flags				
CY	1										Z	S	P	CY	AC
NOT											**NC**	**NC**	**NC**	0	**NC**