Low power 4-Bit Flash ADC with Two Stage Comparator and ROM Based Encoder

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***Abstract*— In this paper, a 4-bit Flash Analog to Digital Converter (ADC) is designed for low power applications. There are two stages in this design which includes the low power comparator stage which gives the thermometer code and the encoder stage to convert the thermometer code to BCD. This design incorporates 15 current mirror based comparators with each consuming 26 µW and a proposed ROM based encoder implemented with least transistor count and also the best power optimization is achieved. The proposed ADC design has a total power consumption of 341.193µW operating at 1V power supply. This design has been simulated in Cadence Virtuoso with 90nm technology node library. Besides this, the paper also gives a brief comparison of the proposed design with the existing FAT Tree based ADC and multiplexer (MUX) based ADC.**

Keywords—Comparator, MUX, FAT Tree, thermometer code, encoder, ROM, Flash ADC, BCD, low power, NMOS, PMOS

I. Introduction

Generally, the flash ADCs are incorporated in applications requiring large bandwidth but they consume more power compared to other ADC architectures. Hence, power optimization is very much necessary for these applications. The flash ADC comprises of two sections (figure1), the first section is a set of comparator arrays and the second being the encoder. The input signal is compared directly includes a series of reference voltages, which are typically produced by a resistor ladder. If the level of the input signal is less (greater) than a reference voltage, the logical zero (one) occurs at the proper reference voltage. The thermometer code is created at the output of the comparator array. A thermometer-to-binary encoder is the ADC's second component.

Now, coming to the first part of the ADC, ie; the comparator array, 2^N-1 comparators are required for an N-bit flash ADC. As a result, the designer must figure out how to enhance comparator speed while without raising power dissipation too much. Another problem is that the resolvable minimum differential input should not be too large to allow for the construction of a flash ADC with acceptable resolution. In order to minimize the minimum input, the input referred offset must be reduced as well. Figure 1 depicts the general circuit diagram of a CMOS flash ADC. Because of its parallel construction, it uses 2^N resistors and 2^N-1 comparators to convert analogue signals to N bits of digital data. The Vin is supplied to one of each comparator's input terminals, and this input voltage is compared to another reference voltage created by the resistor ladder, as illustrated in figure 1. The number of comparators and resistors in the circuit may be raised and lowered to improve or decrease the resolution. Figure 2 is a symbolic diagram of a comparator

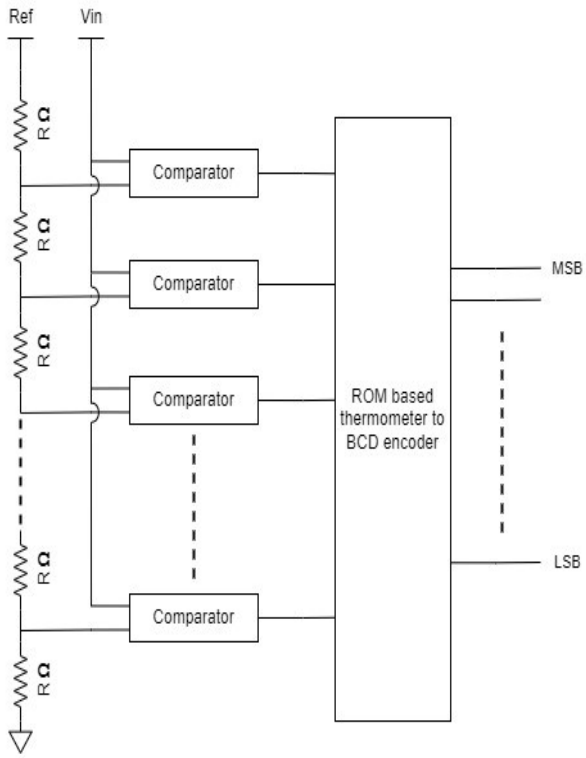

Fig. 1 Block diagram of N-bit flash ADC

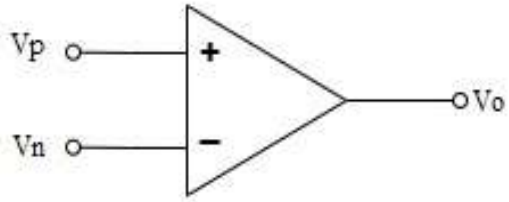

Fig. 2 Symbol of Comparator

TABLE I. TRUTH TABLE OF THERMOMETER CODE TO BCD ENCODER

Thermometer Code															BCD Output			
x15	x14	x13	x12	x11	x10	x9	x8	x7	x6	x5	x4	x3	x2	x1	y3	y2	y1	y0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0
0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	1	1
0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1	0	0
0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	1
0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	1	0
0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	1	1	1
0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	1
0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	1	0
0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

II. EXISTING COMPARATORS

A. *Pre-amplifier and latch based comparator*

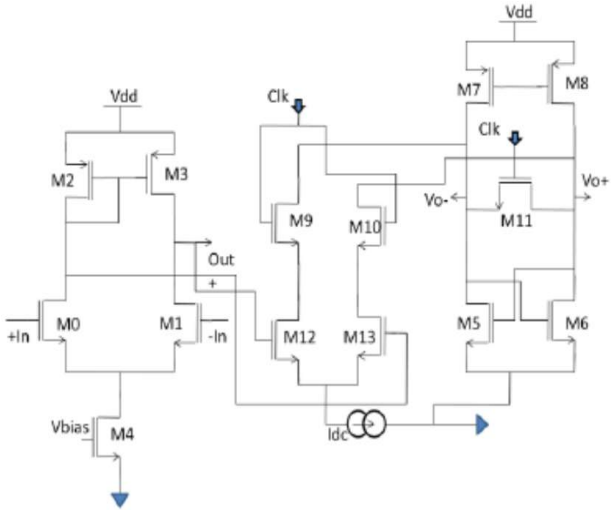

Fig. 3 Pre-amplifier and latch based comparator [2]

The comparator as shown in figure 3 is a pre-amplifier and latch based two stage comparator. Input differential pairs with NMOS transistors and PMOS loads are used to get sufficient gain in the pre-amplifier stage. Two inverters are connected back to back and an NMOS transistor is connected to the differential ends of the latch stage. The pre-amplifier stage is used to improve the sensitivity of the comparator and helps in isolating the input from switching noise of the positive feedback stage implemented in the comparator. The pre-amplifier stage is used to amplify the difference between signal and reference voltage. This comparator design uses 14 transistors.

B. *Dynamic Comparator*

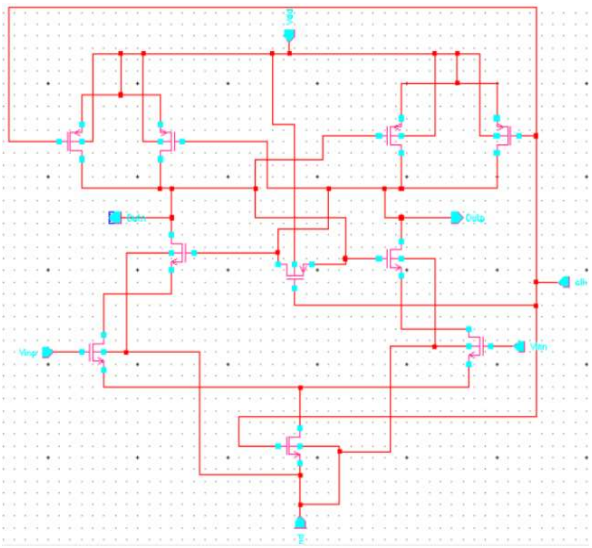

Fig. 4 Dynamic comparator [3]

The dynamic comparator compares the voltages only when the clock goes high, All MOSFETs used are biased in the saturation region so the currents in the branches are the same. As the sizing of all the transistors are the same, the current flowing into the MOSFETs remains identical. When clock input is made low, all the inside nodes are reset to Vdd. Only when inside nodes become Vdd the dynamic comparator goes into comparison mode and compares the input voltage with the given reference signal. The output from the comparator array will be in thermometer code and an encoder is used to convert it to BCD format. This comparator design used 10 transistors.

III. PROPOSED COMPARATOR

Comparators compare one analogue signal (V_P) to another reference signal (V_N) and provide a digital output waveform as a result of the comparison. It is commonly used in ADC conversion.

Vp < Vn Then Vo = Vss = logic 0

Vp > Vn Then Vo = Vdd = logic 1

The interior construction of the comparator (figure 2) is seen in figure 5. This is referred to as a CMOS two-stage comparator. It operates in open loop mode, which eliminates the need for comparator correction. In this case, a bigger bandwidth is achieved, resulting in a faster response. The comparator circuit has two stages: the first is a differential stage, and the second is the output stage. The benefit of this style of design is that it requires fewer transistors and smaller circuitry.

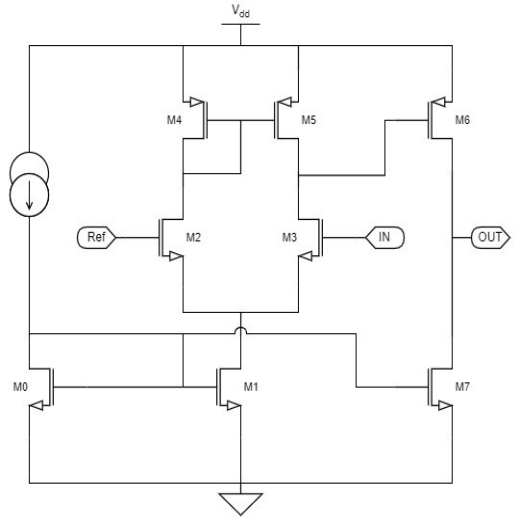

Fig. 5 Schematic of proposed comparator

The comparator used here consists of two stages, the first stage is a differential stage which is followed by a common source stage. The differential stage compares the input analog signal with the applied reference voltage from the series resistor branch. The second stage will make the output swing to full voltage range from Vdd to ground. M3 and M4 form the differential pair branch with M4 and M5 as active PMOS current mirror loads. M0 and M1 MOSFETs give the bias tail current for the differential pair MOSFETs M3 and M4. The same current is mirrored in the second stage through M7. To reduce the power consumption, the entire ADC along with the comparator array operate at a voltage supply of 1V. The transistor sizing is done in the comparator to have minimum power and less rise and fall times.

IV. EXISTING ENCODERS

The main encoder types are MUX based encoders and fat-tree based encoders.

A. MUX Based Encoder

The MUX based encoder used in this design uses transmission gate topology to convert thermometer code to binary code. A 4-bit encoder requires 11 numbers of 2:1 MUXs connected in a tree like structure. A total of 132 transistors are needed to construct a MUX based 4-bit encoder. Multiplexer based encoder is simple in architecture to build but yet power consuming compared to the proposed ROM based encoded design.

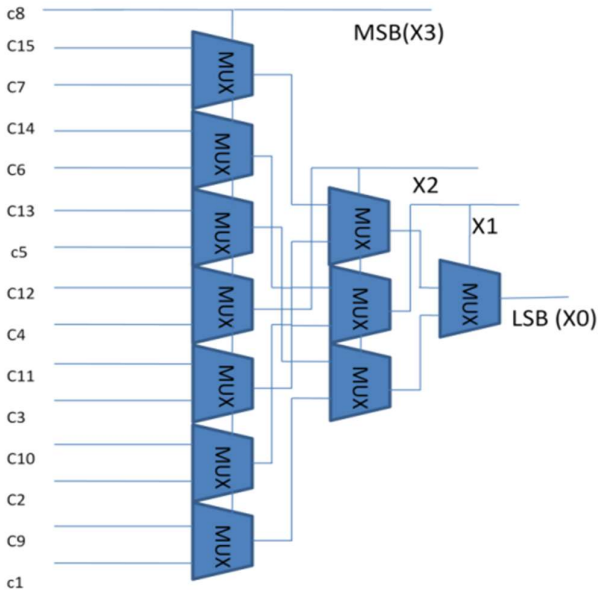

Fig. 6 Schematic of 4-bit Flash ADC using MUX based encoder [2]

B. FAT Tree based Encoder

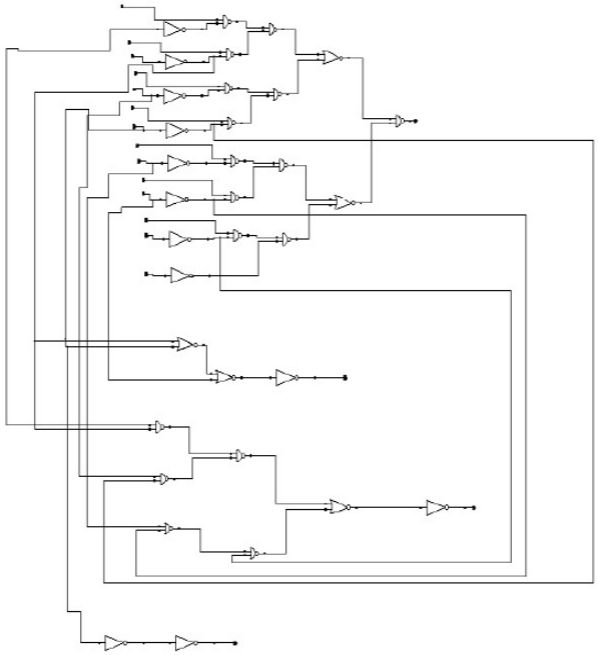

Fig. 7 Schematic of 4-bit Flash ADC using FAT Tree based Encoder [3]

The fat tree based encoder uses CMOS topology to perform thermometer code to binary code encoding. In a fat tree encoder this code conversion happens in two stages. First the thermometer code is converted to one hot code in the first stage and then the one hot code is converted to BCD in the

second stage of the encoder. This encoder design consists of NAND and NOR gates to perform the fat tree conversion. The transistor count for this encoder is 112 for 4-bit encoding. Our proposed ROM based encoder design requires almost half the number of transistors as needed by the fat tree encoder, thus reducing power and area.

V. PROPOSED ROM BASED ENCODER

The MUX based encoder and the Fat tree based encoders have more number of inverters stages in their designs. The inverter's parasitic capacitance at the input is larger than the parasitic capacitance at the input of other inverters. This fact restricts the performance of an encoder circuit. The problem solution is provided in the proposed encoder circuit (Figure 10). To construct the least significant bits y0 and y1, a tree consisting of two stages based on CMOS transistors is required, identical to the circuit that creates the input signal for the inverter in y2.

In this design intermediate control signals are generated in order to minimize the parasitic capacitance at the inverter inputs in the least significant bits. Hence, a circuit is designed to implement a logical function $a.\bar{b}$ which is the intermediate control signal and it is the 1st stage of the encoder block as shown in figure 8. Figure 9 resembles the symbol of the logical element which in incorporated in the Cadence virtuoso design as shown in figure 10.

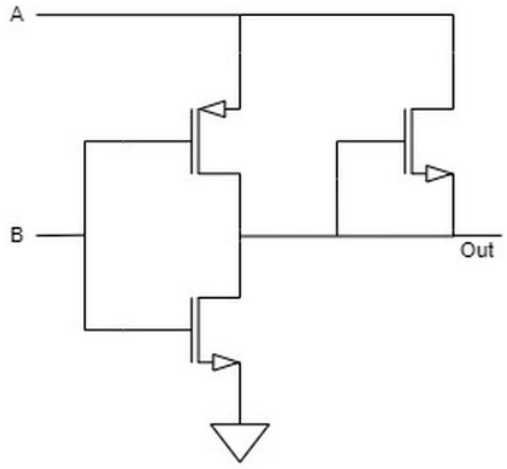

Fig. 8 Schematic of logical element $a.\bar{b}$ [4]

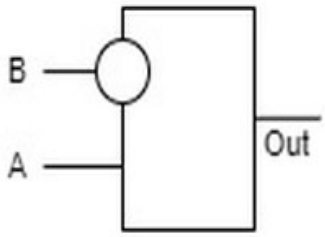

Fig. 9 Symbol of logical element $a.\bar{b}$ [4]

A. Boolean Expressions for Logical element $a.\bar{b}$

$$z_1 = x_1.\overline{x_2}$$
$$z_2 = x_2.\overline{x_4}$$
$$z_3 = x_3.\overline{x_4}$$
$$z_4 = x_4.\overline{x_8}$$
$$z_5 = x_5.\overline{x_6}$$
$$z_6 = x_6.\overline{x_8}$$
$$z_7 = x_7.\overline{x_8}$$
$$z_9 = x_9.\overline{x_{10}}$$
$$z_{10} = x_{10}.\overline{x_{12}}$$
$$z_{11} = x_{11}.\overline{x_{12}}$$
$$z_{13} = x_{13}.\overline{x_{14}}$$

B. Boolean Expressions for the ROM based Encoder

$$y_3 = x_8$$
$$y_2 = z_4 + x_{12}$$
$$y_1 = \overline{\overline{z_2 + z_6}\ .\overline{z_{10} + x_{14}}}$$
$$y_0 = \overline{\overline{z_1 + z_3 + z_5 + z_7}\ .\overline{z_9 + z_{11} + z_{13} + x_{15}}}$$

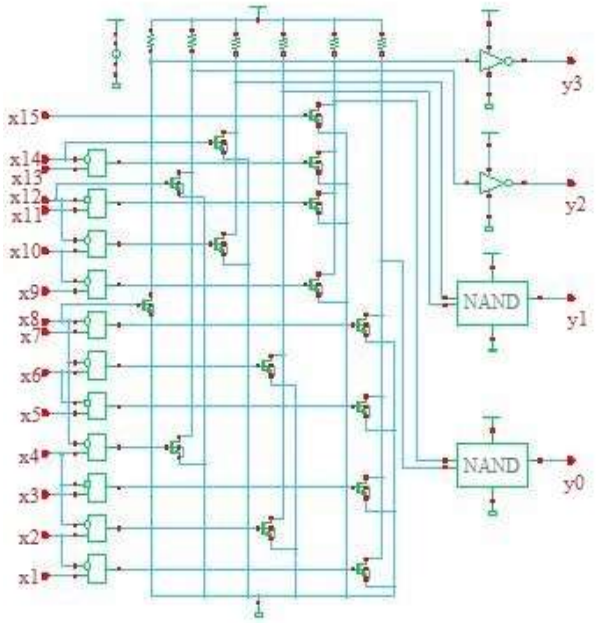

Fig. 10 Proposed ROM-based encoder based on $a.\bar{b}$ logical element and NAND in the least significant bits y0 and y1

The transistor array columns, which represents the least significant bits y0 and y1, are realized by two columns for each, the signals of which are sent to NAND inputs. The suggested circuit using NAND is solely utilized for creating the output with higher encoder resolution.

VI. COMPARISON OF PROPOSED ADC WITH MUX AND FAT TREE BASED ADCs

The ADC with the ROM based encoder has been simulated using Cadence Virtuoso on the 90 nm technology, operated at a supply voltage of 1V, for resolution of four bits. And so, it can represent 2^4 values. Thus, for each 0.0625 V we get a toggling of values. The simulation and compared results have been presented.

ADC USING PROPOSED ROM BASED ENCODER

This design includes 15 proposed comparators (figure 5) which are used to convert the analog signals to thermometer code. The thermometer code is fed to the proposed ROM based encoder in order to encode to the BCD form. This design has less number of transistors compared to the other designs which in turn leads to less power consumption, less parasitic capacitances and also less device area. Also, the transistor sizing has been done as shown in table II in order to achieve these optimizations.

TABLE II. TRANSISTOR SIZES USED FOR VARIOUS LOGIC ELEMENTS IN THE PROPOSED DESIGN

Transistor Sizes (Width)		
Inverter	PMOS	300nm
	NMOS	120nm
NAND	PMOS	300nm
	NMOS	240nm
$a.\bar{b}$	PMOS	300nm
	NMOS	120nm
Encoder	NMOS	240nm

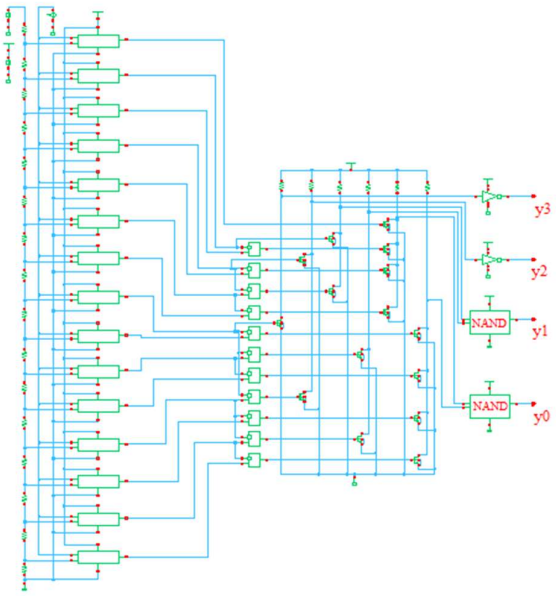

Fig. 11 Schematic of 4-bit Flash ADC using proposed ROM based encoder using $a.\bar{b}$ logic element

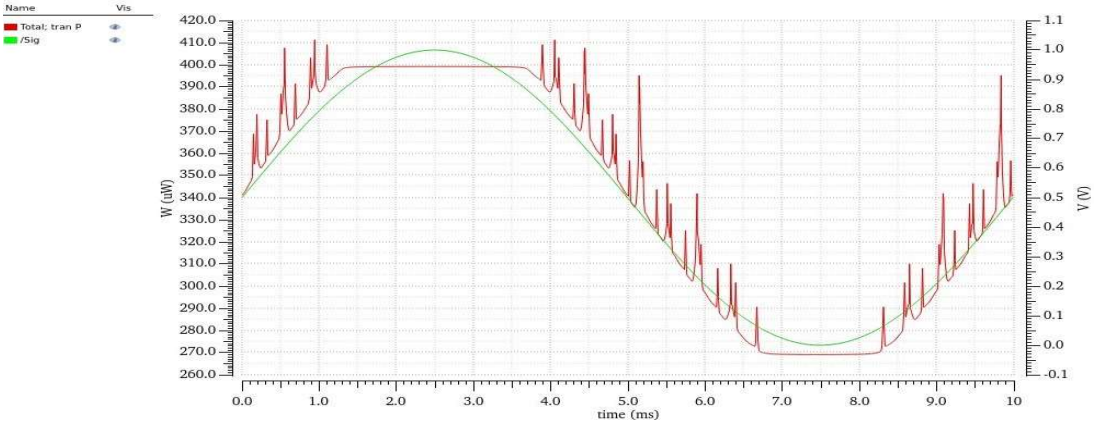

Fig. 12 Power consumption of the proposed circuit

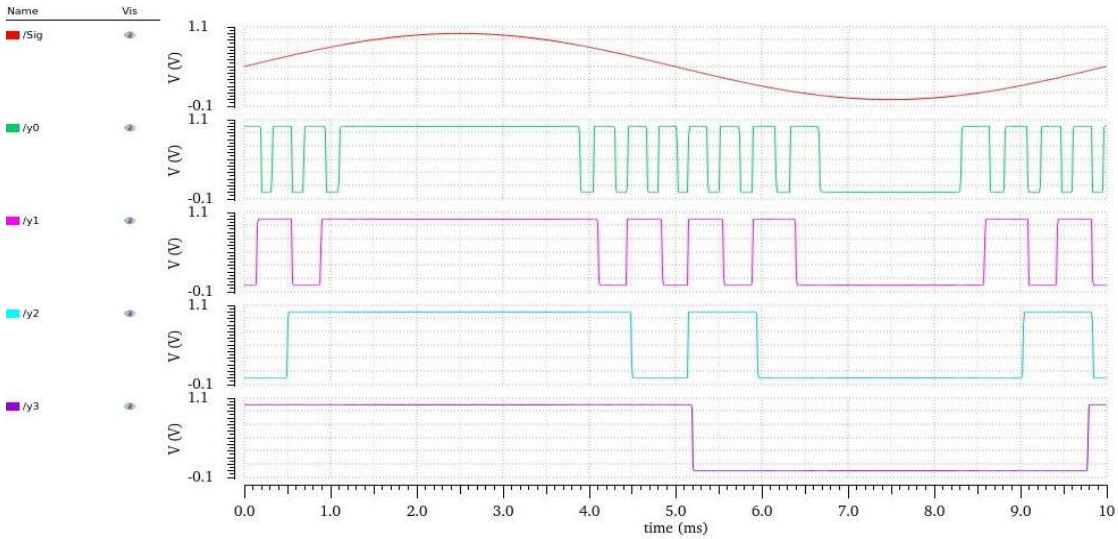

Fig. 13 Final output of the 4-bit ADC based on proposed ROM based encoder

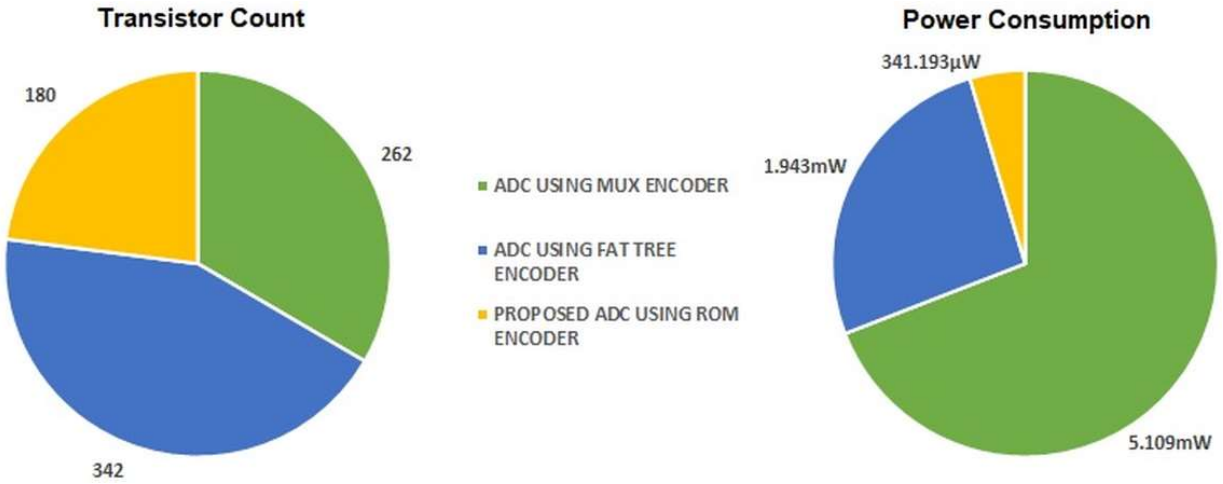

Fig. 14 Comparison Transistor Count and Power consumption for various ADCs

TABLE III. COMPARISON OF ALL THE THREE TYPES OF ADC DESIGNS

	Design1 [3]	**Design2 [4]**	**Proposed design**
Encoder type	Fat tree	Mux based	ROM based
Encoder transistor count	112	132	60
Comparator transistor count	150	210	120
Total transistor count	262	342	180
Total power consumption	5.109mW	1.943mW	341.193µW
Comparator power consumption	329.332µW	-	26µW
Operating voltage	1V	1.5V	1V

VII. CONCLUSION

The simulation results of the 4-bit Flash ADC using proposed ROM based encoder clearly shows the reduction in power consumption. As we use the current mirror based comparator the number of transistors for the comparator design is reduced to 8. Similarly, the power has been optimized in the encoder stage by reducing the transistor count to 60. The MUX encoder based ADC consumes 1.943mW of average power and fat tree encoder based ADC consumes 5.109mW of average power. Whereas, the ADC with proposed ROM based encoder consumes only 341.193µW of average power compared to the ADCs with MUX based and FAT Tree based encoder. Hence, the reduction in average power has a great advantage in the usage of this flash ADC in low power applications and also the reduced transistor count in turn will occupy less area.

VIII. REFERENCES

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