

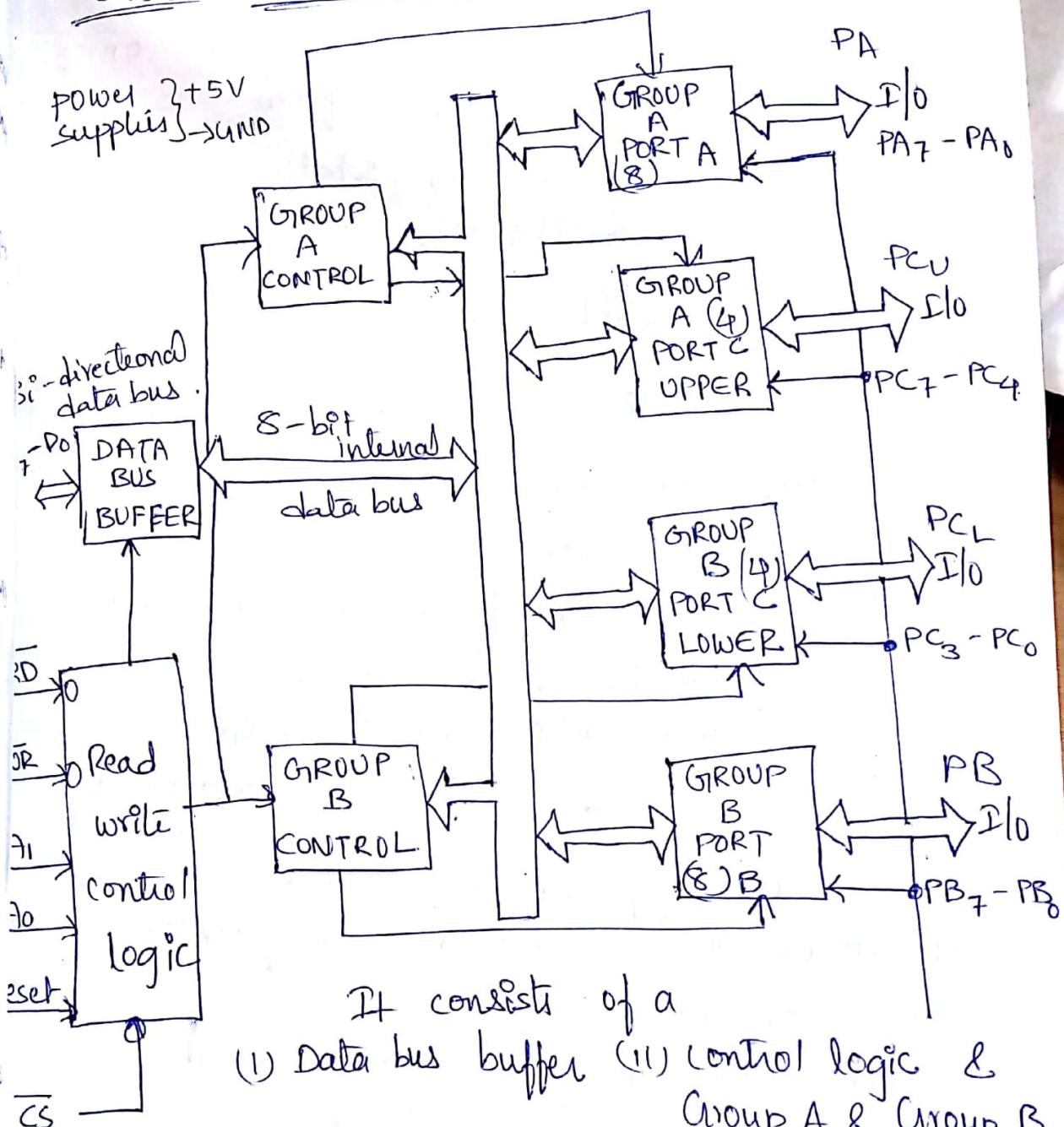
8255 → programmable peripheral Interface

- 8255 is a programmable peripheral Interface (PPI) device for use in INTEL micro computer systems. It is completely compatible with TTL.
- It is used as general purpose I/O component to interface peripheral equipment to the micro computer system bus.
- It can be programmed to transfer data under various conditions, from simple I/O to interrupt I/O.
- It can be used with almost any CPU.
- It has 24 input/o/p lines which may be individually programmed in two groups of twelve lines each (or) three groups of eight lines.
- The two groups of I/O pins are named as Group A & Group B.
- Each of these two groups contain subgroup of eight I/O lines called as 8-bit port & another subgroup of 4 I/O lines or a 4-bit port.

- Thus group A contains an 8-bit port A along with 4-bit port C upper.
- The port A lines are identified by symbols $PA_0 - PA_7$ while the port C lines are identified as $PC_4 - PC_7$.
- Similarly Group B contains an 8-bit port B, containing lines $PB_0 - PB_7$ & a 4-bit port C with lower bits $PC_0 - PC_3$.
- The port C upper & port C lower can be used in combination as an 8-bit port C.
- ~~All~~ All of these ports can function independently either as i/p or as o/p ports. This can be achieved by programming the bits of an internal register of 8255 called as control word register (CWR).
- ~~Each~~ Each port has an unique address & data can be read from or written to a port. In addition to the address assigned to the three ports, another address is assigned to the control register in to which control words are written for programming the 8255 to operate in various modes.

8255

Architecture



It consists of a

- (1) Data bus buffer
- (2) Control logic & Group A & Group B control.

Data bus buffer

→ It is a tri-state bi-directional 8-bit buffer which is used to interface the internal bus of 8255 to the system data bus.

→ Data is transmitted (or) Received by the buffer i.e. Read data from or write data in to the buffer as per the instructions by the CPU.

- Three ports of 8255 are divided into 2 groups
- Group A :- It includes port A & port C upper
- Group B :- " " " port B & port C lower
- The functions of 8255 A is classified into two modes .
i.e Bit set / Reset (BSR) mode & I/O mode .
- The bit set / reset mode allows setting & resetting of individual bits of Port C .
- The I/O mode is further divided in to three modes : i.e
- 1) Mode 0 . :- simple I/P / O/P
 - 2) Mode 1 . :- I/P / O/P with handshake
 - 3) Mode 2 → bi-directional I/O data transfer

Mode 0 :-

port A and Port B can be configured as simple 8-bit I/P or O/P ports without handshaking .

The two halves of port C can be programmed separately as 4-bit I/P or O/P ports .

Mode 1 :-

two groups each of 12 pins are formed .

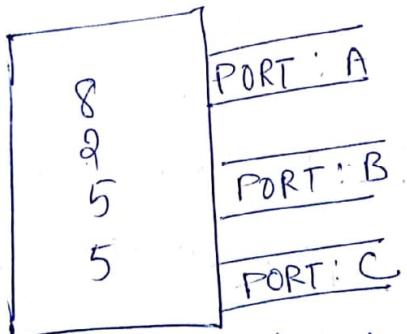
Group A consists of port A and the upper of port C while Group B consists of port B & the lower half of port C . port A and B can be programmed as 8-bit I/P or O/P ports with three lines of port C in each

group used for handshaking

Handshaking signals which are used to transfer data between devices whose transfer speeds are not same.

Mode 2 → port A can be used as a bidirectional port. only port A can be provided on. The handshaking signals are provided on five lines of port C ($PC_3 - PC_7$). Port B can be used in mode 0 or in mode 1.

→ All I/O pins of 8255 have 2.5 mA DC driving capability (ie. source current of 2.5 mA)



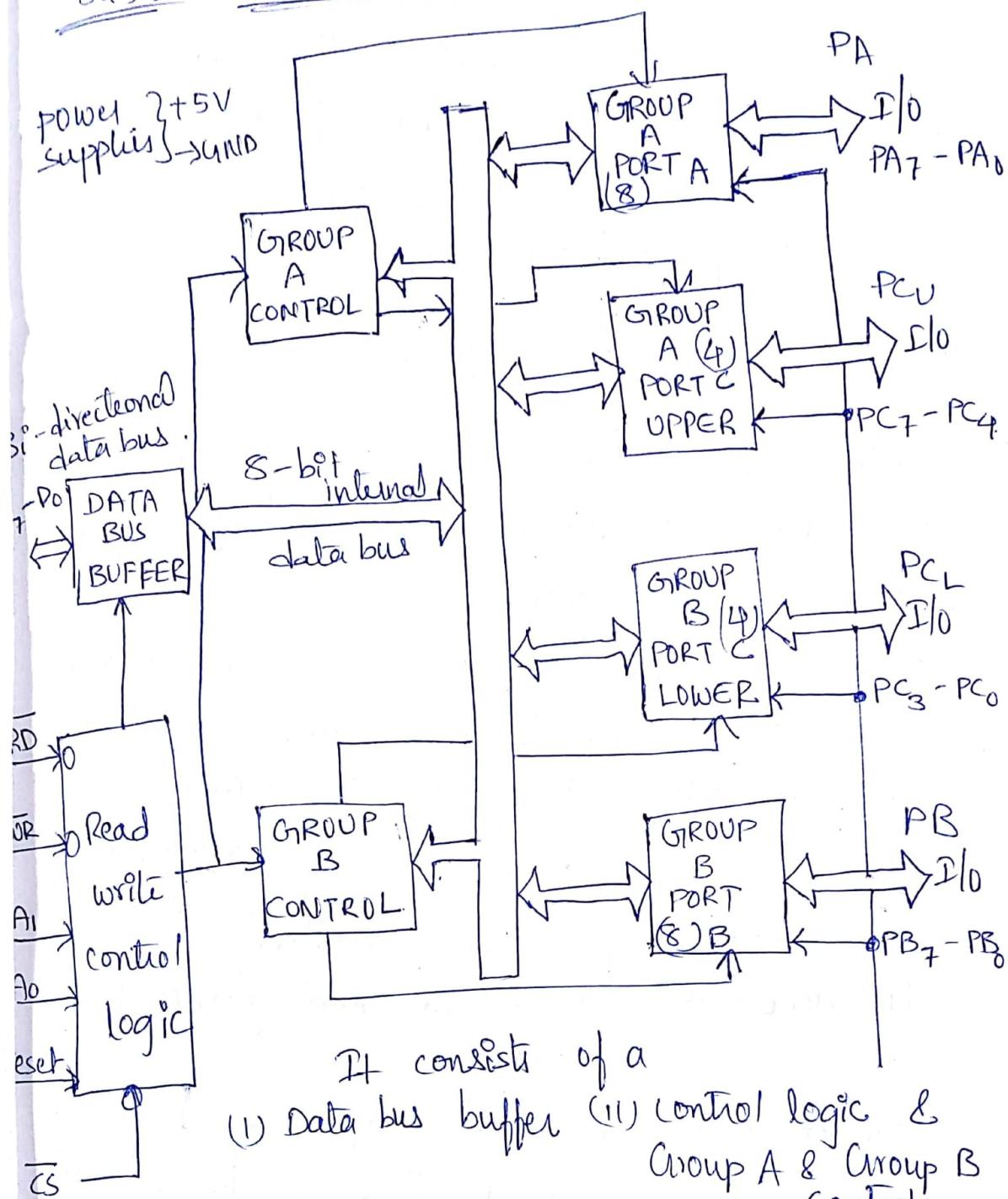
mode 0 — each port can be programmed in either I/P mode or O/P mode. where I/P's are not latched. O/P's are latched.

mode 1 — I/P's & O/P's are latched.

mode 2 — port A is used as bi-directional port. & port B either in mode 0 or mode 1. port A uses 5 signals from port C as handshaking signals for data transfer. the remaining 3 signals from port C can be either as simple I/O or as handshaking for port-B.

8255

Architecture



It consists of a

- (i) Data bus buffer
- (ii) Control logic & Group A & Group B control.

Data bus buffer

- It is a tri-state bi-directional 8-bit buffer, which is used to interface the internal data bus of 8255 to the system data bus.
- Data is transmitted (or) Received by the buffer i.e. Read data from or write data in to the buffer as per the instructions by the CPU.

- control words & status information is also transferred using the bus.
- O/p data from the CPU to the ports or control register, & O/p data ~~from~~ to the CPU from the port or status registers are all passed through the buffer.

Read / write Control logic

- This block is responsible for controlling the internal or external transfer of data/ control / status word.
- It accepts the I/p from the CPU address & control busses & it issues command to both the control groups. (Group A & Group B control)
- It issues appropriate enabling signals to access the required data / control words or status word.

Group A and Group B controls

- Each of the Group A & Group B control blocks receives control words from the CPU & issues appropriate commands to the ports associated with it.
- The Group A control block controls Port A and $PC_7 - PC_4$ while Group B control block controls Port B and $PC_3 - PC_0$.

Port A! This has an 8-bit latched & buffered o/p & an 8-bit I/P latch. It can be programmed in three modes mode 0, mode 1, mode 2.

Port B!- This has an 8-bit data I/O latch/buffer and an 8-bit data I/P buffer. It can be programmed in mode 0 & mode 1.

Port C! This has one 8-bit unlatched i/p buffer & an 8-bit o/p latch/buffer. Port C can be separated into two parts & each can be used as control signals for port A & B in the hand shake mode. It can be programmed bit set/reset operation.

Pin diagram of 8255	
PA ₃	1
PA ₂	2
PA ₁	3
PA ₀	4
RD	5
CS	6
CND	7
A ₁	8
AO	9
PC ₇	10
PC ₆	11
PC ₅	12
PC ₄	13
PC ₀	14
PC ₁	15
PC ₂	16
PC ₃	17
PB ₀	18
PB ₁	19
PB ₂	20
PA ₄	40
PA ₅	39
PA ₆	38
PA ₇	37
WR	36
RESET	35
D ₀	34
D ₁	33
D ₂	32
D ₃	31
D ₄	30
D ₅	29
D ₆	28
D ₇	27
V _{CC} (5V)	26
PB ₇	25
PB ₆	24
PB ₅	23
PB ₄	22
PB ₃	21

D₀-D₇ :- (Data bus)

These bi-directional tri-state data bus lines are connected to the system data bus. They are used to transfer data & control word from up to 8255 or to receive data or status word from 8255 to up.

PA₀-PA₇ :- (Port A)

These 8-bit bi-directional I/O pins are used to send data to o/p device & to receive data from i/p device. It functions as an 8-bit data o/p latch / buffer, when used in o/p mode & 8-bit data i/p buffer when used in i/p mode.

PB₀-PB₇ :- (port B)

These 8-bit bi-directional I/O pins are used to send data to o/p device & to receive data from i/p device. It functions as an 8-bit data , o/p latch / buffer when used in op mode & 8-bit data i/p buffer when used in i/p mode .

PC₀-PC₇ :-

These 8-bit bi-directional I/O pins are divided in to two groups PC_L (PC₃-PC₀) & PC_U (PC₇-PC₄). These groups individually can transfer data in or out when programmed for simple I/O, & used as hand shake signals when programmed for handshake or bi-directional modes.

RD → (Read).

This signal enables read operation when the signal is low, the CPU can read the data from selected I/O port or the Status word, through the data buffer.

WR → (Write)

This control signal enables write operation. When this signal goes low, CPU writes into a selected I/O port or control register, through the data bus buffer.

CS :-(chip select.)

This is an active low output which can be enabled for data transfer operation between the CPU & the 8255.

It connects to the decoded address & A₀ & A₁ are connected to the CPU address lines.

Their result depends on following operating conditions.

CS	A ₁	A ₀	Result
0	0	0	Port - A
0	0	1	Port - B
0	1	0	Port - C
0	1	1	control registers
1	X	X	No selection

Reset L

This is an active high signal used to Reset 8255. When this sig is high the control register is cleared & all the ports are set to the I/P mode. usually RESET OUT signal from 8085 is used to reset 8255

A₀ & A₁ -

These I/P signals work with RD & WR. They control the selection of the I/P's or control the selection of the control / status register or one of the three ports.

A ₁	A ₀	RD	WR	CS	Result
0	0	0	1	0	I/P operation PORT A → data bus
0	1	0	1	0	PORT B → data bus
1	0	0	1	0	PORT C → data bus
1	1	0	1	0	control word → data bus
0	0	1	0	0	<u>I/P operation</u> Data bus - PORT A
0	1	1	0	0	Data bus - PORT B
1	0	1	0	0	Data bus - PORT C
1	1	1	0	0	Data bus → Control Reg (port-n)

operation modes:-

(1) BSR mode (Bit set - Reset mode).

The individual bits of port C can be set or reset by sending out a single OUT instruction to the control reg. When Port C is used for control / status operation, this feature can be used to set or Reset individual bits.

(2) I/O modes

(i) mode 0: Simple I/P / O/P.

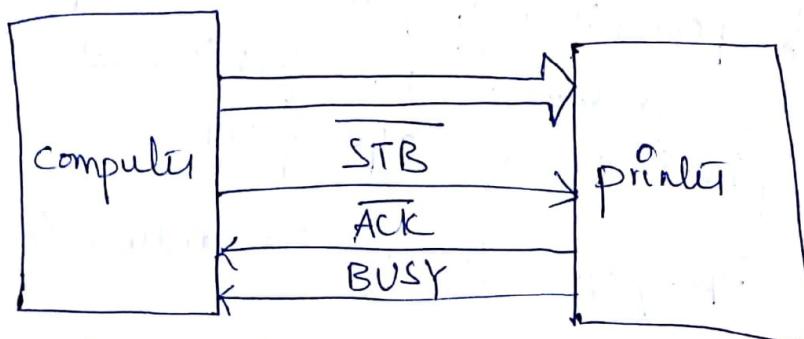
- In this mode, Port A and Port B are used as two simple 8-bit I/O ports & Port C as two 4-bit ports.
- Each port (or half-port, in case of C) can be programmed to function as simply an I/P port or an O/P port.
- The I/P / O/P feature in mode 0 are as follows:

(1) O/P's are latched (2) I/P's are buffered, not latched

(3) ports do not have handshake or interrupt capability.

Mode 1:- I/p / O/p with handshake.

- In this mode, I/p or O/p data transfer is controlled by handshaking signals.
- Handshaking signals are ~~not~~ used to transfer data between devices whose data transfer speeds are not same.
- Ex:- Computer can send data to the printer & accept with large speed but printer can't accept data & print data with this rate. So computer has to send data with the speed with which printer can accept. This type of data transfer is achieved by using handshaking signals along with data signals.



- It shows data transfer between computer & printer using handshaking signals. These handshaking signals are used to tell computer whether printer is ready to accept the data or not. If printer is ready to accept the data then after sending data on data bus

computer uses another handshaking signal (\overline{STB}) to tell printer that valid data is available on the data bus.

→ The 8255 mode 1 which supports handshaking has following features

(1) Two ports (A & B) function as 8-bit I/O ports. They can be configured either as I/P or O/P ports.

(2) Each port uses three lines from port C as handshake signals. The remaining two lines of port C can be used for simple I/O functions.

(3) I/P & O/P data are latched.

(4) Interrupt logic is supported.

Mode 2: Bi-directional I/O data transfer.

→ This mode allows bi-directional data transfer (transmission & reception) over a single 8-bit data bus using handshaking signals. This feature is available only in Group A with port A as the only bi-directional data bus; and PC₃ - PC₇ are used for handshaking purpose.

→ In this mode, both I/P's & O/P's are latched.

→ Due to use of a single 8-bit data bus for bi-directional data transfer the data sent out by the CPU is

To the peripheral only when the peripheral requests it.

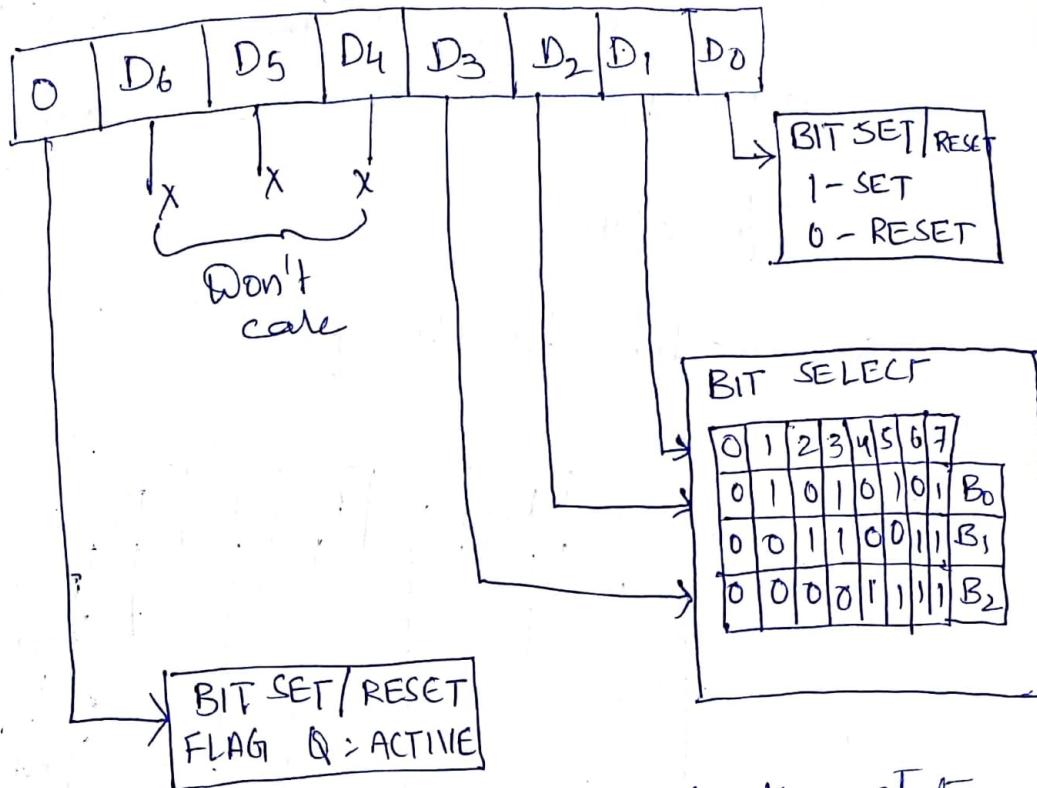
- The remaining lines of port C i.e. PC₀-PC₂ can be used for simple I/O functions.
- The port B can be programmed in mode 0 or in mode 1. When port B is programmed in mode 1, PC₀-PC₂ lines of port C are used as handshaking signals.

Control word Formats

- A high on the RESET pin causes all 24 lines of the three 8-bit ports to be in the I/O mode. All flip-flops are cleared and the interrupt are reset. This condition is maintained even after the RESET goes low.
- The ports of the 8255 can then be programmed for any other mode by writing a single control word into the control register, when required.

→ for Bit Set / Reset Mode :-

for bit set / reset control word format.

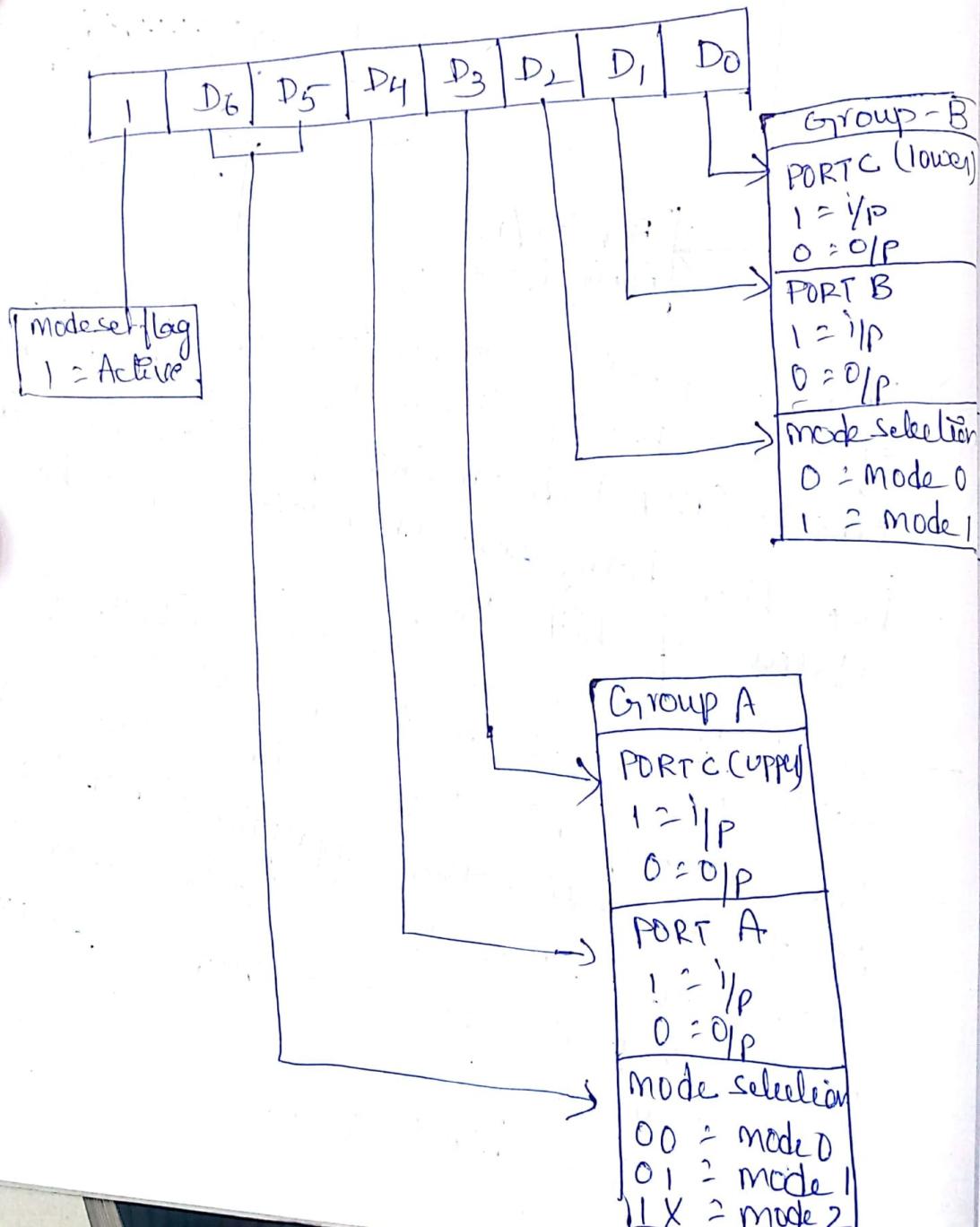


- The 8 possible combinations of the states of bits D₃-D₁ (B₂ B₁ B₀) in the Bit-set format (BSR) determine particular bit in PC₀-PC₇ being set or reset as per the status of bit D₀.
- A BSR word is to be written for each bit that is to be set or reset.
- For ex., if bit PC₃ is to be set & PC₄ is to be reset, the appropriate BSR words that will have to be loaded into the control reg will be, 0xXX0111 & 0xXX1000 respectively.
- X - don't care

→ The BSR word can be used for enabling or disabling interrupt by port C, when the IED for mode 1 or 2 is done by setting or resetting the associated bits of the interrupt.

For I/O mode

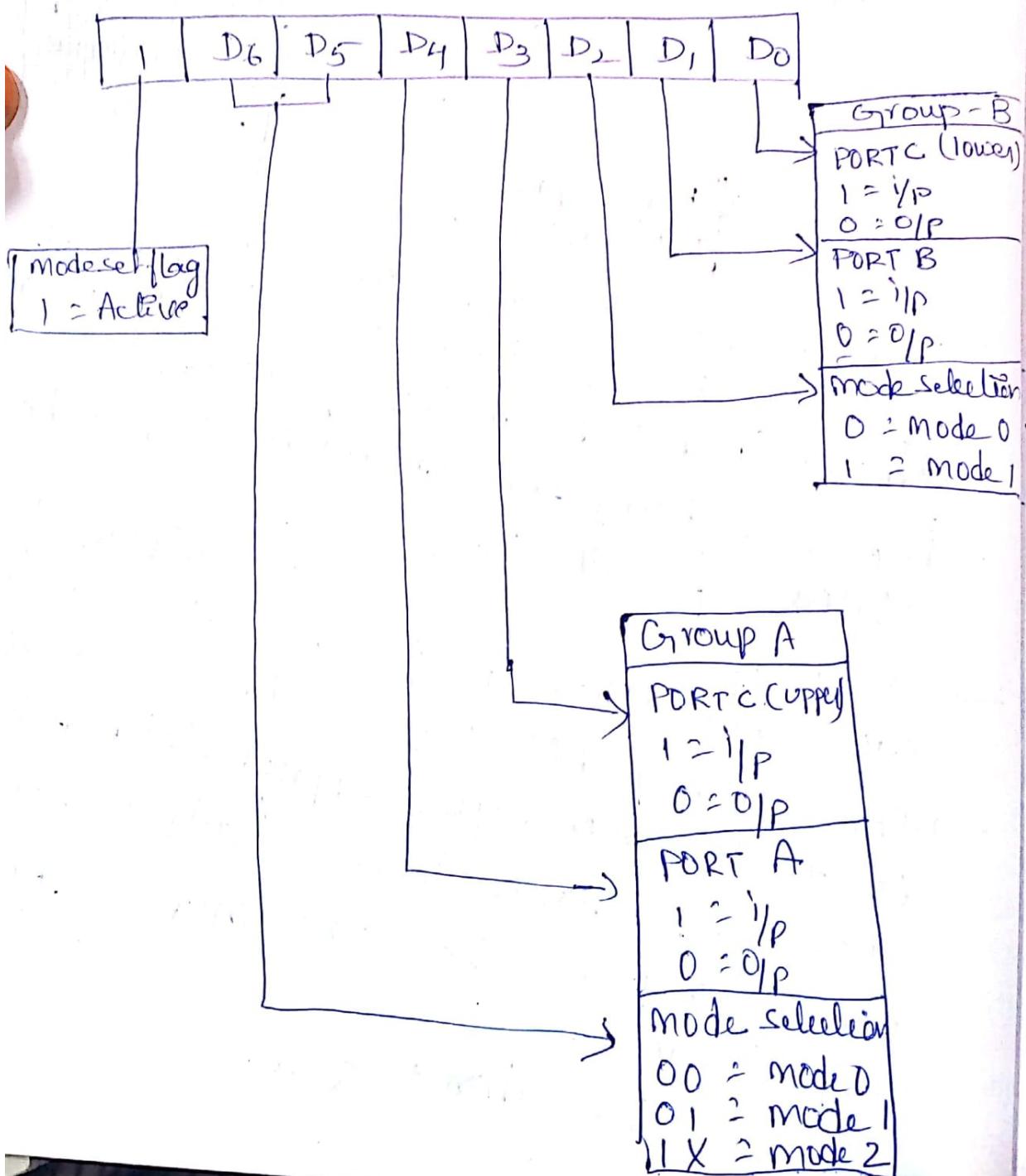
→ The mode format for I/O is



→ The BSR word can be used for enabling or disabling interrupt signals generated by port C. When the 8255 IC programmed for mode 1 or 2 operation. This is done by setting or resetting the associated bits of the interrupt.

For I/O mode

→ The mode format for I/O is



→ The control words for both mode definition & bit-set-reset are loaded into the same control register, with bit D₇ used for specifying whether the word loaded into the control register is a mode definition word or bit-set-reset word.

→ If D₇ is high, the word is taken as a mode definition word, & if it is low, it is taken as bit-set-reset word.

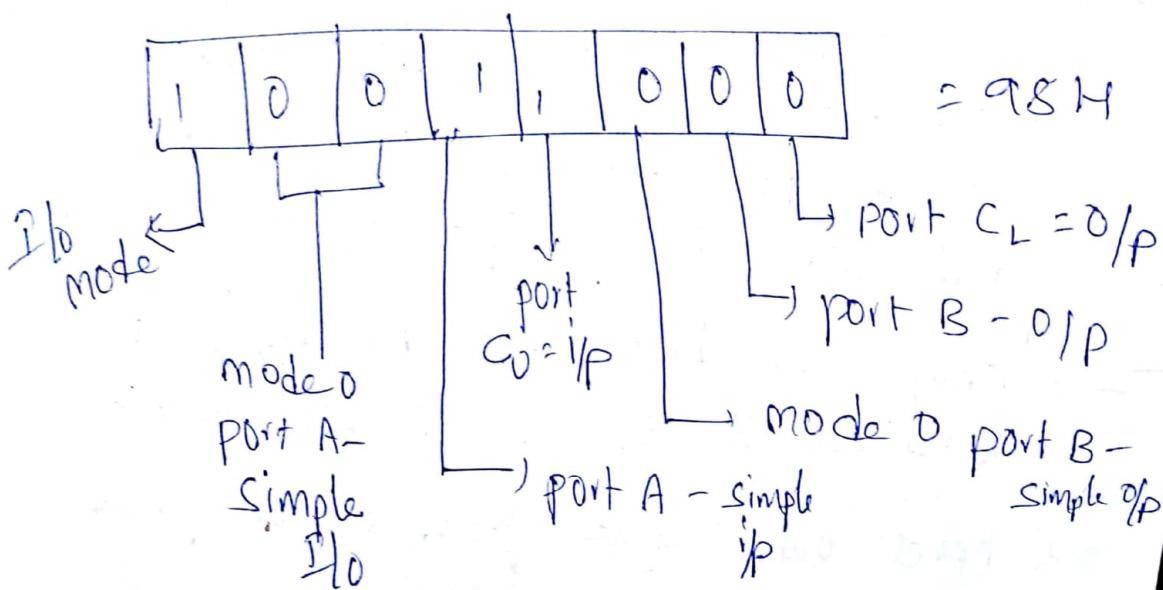
→ The appropriate bits are set or reset depending on the type of operation desired, & loaded into the control register.

Ex port A : Simple I/P

port B : Simple O/P

Port C_L = O/P

Port C_H = I/P

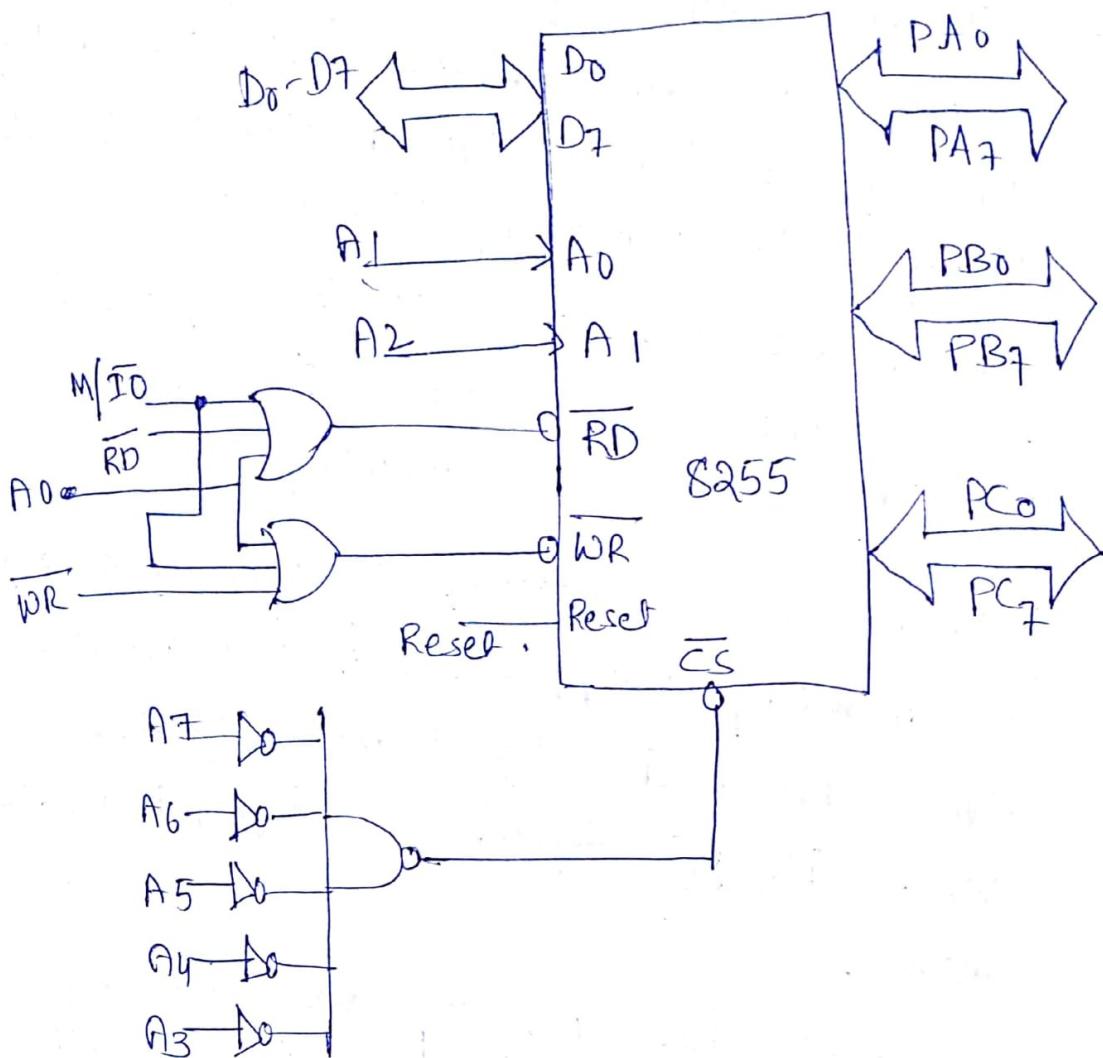


Qn port A = o/p with handshake
 Port B : i/p " "
 Port C₂ = o/p
 Port C₀ = i/p.
 Ans : AE

Interfacing of 8255 with 8086

- The 8086 has special instructions IN, OUT to transfer data through the input / output ports in I/O mapped I/O system.
- M/I_O signal is always low when 8086 is executing these instructions.
- only 256 (2^8) I/O addresses can be generated when direct addressing method is used. By using indirect address method their range can be extended up to 65536 (2^{16}) addresses.
- The fig shows the interfacing of 8255 with 8086 in I/O mapped I/O technique.
- Here RD and WR signals are activated when M/I_O signal is low.
- only lower data bus ($D_0 - D_7$) is used as 8255 is 8-bit device.
- Reset out signal from clock generator is connected to the Reset signal of the 8255.

Interfacing of 8255 with 8086

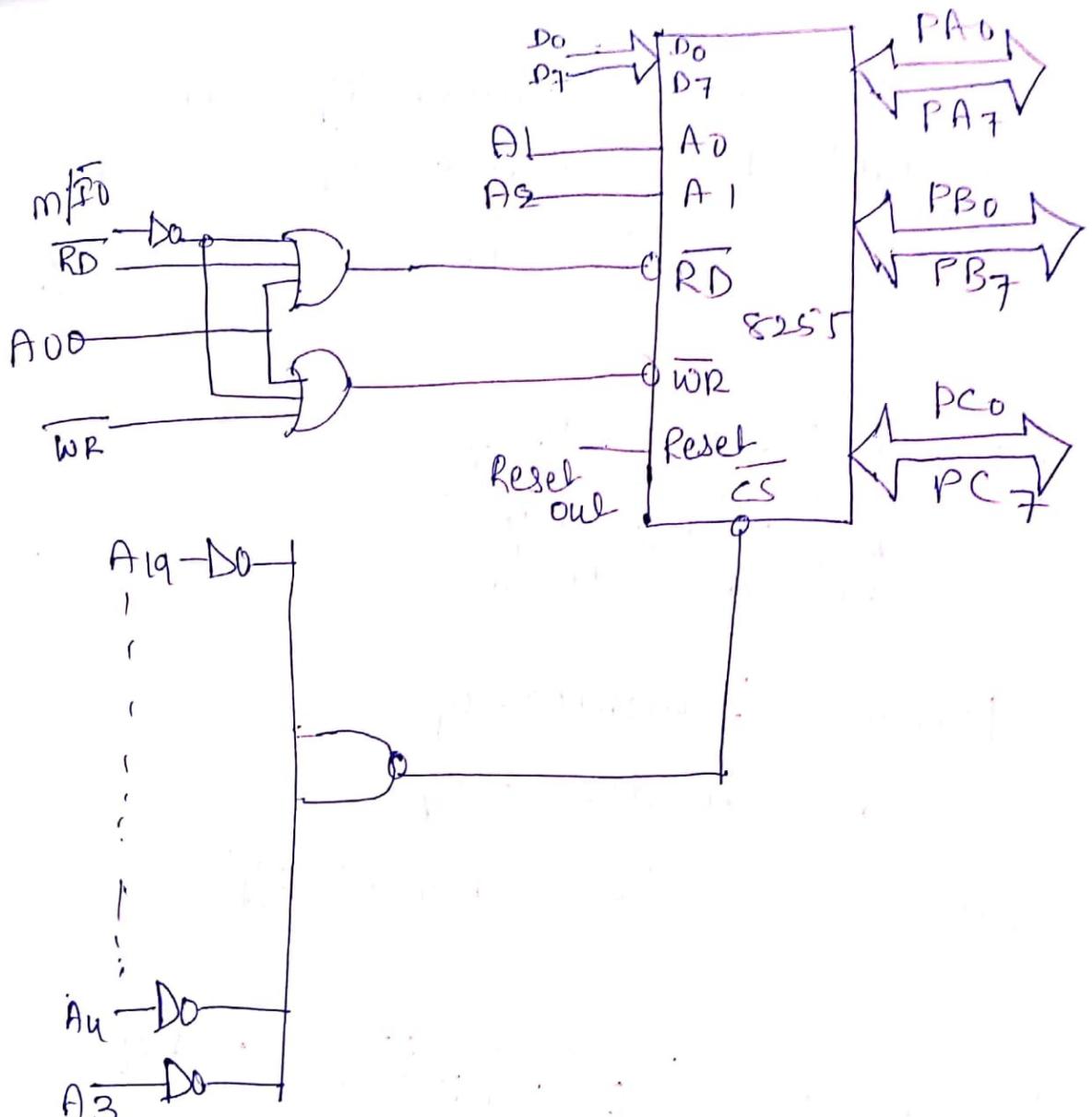


I/O map: (Direct addressing is used)

port / control Registry	Address lines	Address
	A ₇ A ₆ A ₅ A ₄ A ₃ A ₂ A ₁ A ₀	
PORT A	0 0 0 0 0 0 0 0	00 H
PORT B	0 0 0 0 0 0 1 0	02 H
PORT C	0 0 0 0 0 1 0 0	04 H
control register	0 0 0 0 0 1 1 0	06 H

Interfacing 8255 with 8086 (Indirect)

- In this type of I/O interfacing the 8086 uses 20 address lines to identify an I/O device & I/O device is connected as if it is a memory register.
- The 8086 uses same control signals & instructions & instructions to access I/O as those of memory.
- fig shows the interfacing of 8255 with 8086 in memory mapped I/O technique.
- Here RD & WR signals are activated when M/R signal is high, indicating Mem.
- Address lines A₀-A₂ are used by 8255 for internal decoding. To get absolute address, all remaining address lines (A₃-A₁₉) are used to decode the address for 8255.
- Other Signal connections are same as in I/O mapped I/O.



I/O map:

Registers	A ₁₉	A ₁₈	A ₁₇	A ₁₆	A ₁₅	A ₁₄	A ₁₃	A ₁₂	A ₁₁	-	A ₃	A ₂	A ₁	A ₀	address
PORTR	0	0	0	.	-	-	-	-	-	.	0	0	0	0	00001
PORTB	0	0	-	-	-	-	-	-	-	-	0	0	1	0	0002
PORTC	0	0	-	-	-	-	-	-	-	-	0	1	0	0	0004
control Reg	0	0	-	-	-	-	-	-	-	-	0	1	1	0	00061

(v) prepare a control word to initialize 8255

as

- (i) port A handshake O/P Ans : B4
(ii) port B handshake O/P. 101 B5
(iii) port C bits PC₆ & PC₇ as O/P.

1	0	1	1	1	0	1	1	0	X
PA	Mode	PA	PC ₆	PC ₇	Mode	PA	PC ₆	PC ₇	O/P

(i) Port A - handshake I/P

Port B - handshake O/P

Port C - bits PC₆ & PC₇ as O/P's

1	0	1	1	1	0	1	1	0	X
I/O	Mod	PA	PC	M1	PB	PC			B4