



Certificate no: UC-970cb576-e016-4d6e-b0e8-15d14e995c59
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Reference Number: 0004

CERTIFICATE OF COMPLETION

Verilog for an FPGA Engineer with Xilinx Vivado Design Suite

Instructors **Kumar Khandagle**

Naveen Badiger

Date **Dec. 14, 2022**

Length **16.5 total hours**