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https://github.com/Naveenub/resume/blob/main/Resume.pdf
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NAVEEN U BADIGER

OBJECTIVE

To pursue a challenging career in your organization which would be mutually beneficial in terms of learning experience and contribution to Organizational growth.

PROFILE SUMMARY

Proficient in designing from scratch, testing FPGA based digital systems and embedded systems with SOC, Verilog design sources, Verilog test bench sources. Possess excellent communication skills and ready to work in a challenging environment.

SKILLS & ABILITIES

KNOWLEDGE OF SEMICONDUCTOR/VLSI DESIGN

Fundamentals Of Digital And Analog Circuits, Design Methodologies, Design Flow, Hardware Description Languages, Etc.

INDUSTRY KNOWLEDGE

Analog Circuit Design, Digital Electronics, Microprocessors, Network Theory, Control System, Process Control Etc.

PROGRAMMING LANGUAGES

C; Verilog, Python, Matlab, Assembly Language, Embedded C

IDEs

Xilinx Vivado, NI Multisim, Octave, Cadence Virtuoso, KeilUvision, LabVIEW

INTERPERSONAL SKILLS

Communication, Empathy, Flexibility, Leadership, Patience, Self-learning

PROBLEM-SOLVING SKILLS

Attention To Detail, Collaboration, Patience, Research

COMMUNICATION SKILLS

Active Listing, Interpersonal Communication, Verbal/Nonverbal Communication, Written Communication

PRODUCT SKILLS

Jira Management, Linux, Xshell.

EDUCATION	**DIPLOMA** INSTITUTE NAME:- K H Kabbur Institute Of Technology, Vidyagiri, Dharwad FIELD OF STUDY:- Electronics And Communication PERIOD OF STUDY:- July 2015 to Dec 2018 PERCENTAGE SECURED:- 63.52% **BACHELOR'S OF ENGINEERING** INSTITUTE NAME:- Kls's Vishwanath Rao Deshpande Institute Of Technology, Haliyal FIELD OF STUDY: - Electronics And Communication PERIOD OF STUDY: - July 2019 to July 2022 PERCENTAGE SECURED: - 69.2% & CGPA SCORED: - 7.27/10
INTERNSHIP	INSTITUTE NAME:- Haegl Technologies Pvt Ltd, Dharwad AREA:- Artificial Intelligence And Internet Of Things TIME PERIOD:- 01st September 2021 To 30th September 2021
WORK HISTORY	Position:- Technical Associate Trainee, ZKTeco International Technical Support Center, Bangalore, Karnataka Period:- Oct 2022 – Present
ACADEMIC CERTIFICATES	Design of VLSI System and Verification of Digital Circuits using Simulation Tool
UDEMY CERTIFICATES	1. Verilog for an FPGA Engineer with Xilinx Vivado Design Suite 2. Verilog HDL VLSI Hardware Design Comprehensive Masterclass.pdf 3. FPGA Turbo Series-Communication Protocol
PROJECTS	**1. Blinking LED using 555 timers** **2. A stable Multivibrator (Mini-Project @ Diploma)** **3. Smart Train System (Final Year Project @ Diploma)** **4. Heart Beat Sensor using Arduino (Mini-Project @ Engineering)** **5. IOT based Industry Security Automation using Raspberry Pi** **(Final year Project @ Engineering)**
COMMUNICATION	Excellent written and verbal communication skills, Confident and professional speaking abilities, Empathic listener and persuasive speaker.
LEADERSHIP	Collaborating effectively, cultivating team orientation among staff/Colleagues, Decision-Making, Drawing consensus on group goals, Strategic planning.