Naveen Umesh Badiger

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https://github.com/Naveenub/resume/blob/main/Resume.pdf

Profile Summary	I am a skilled Electronics and Communication Engineer with hands-on experience in various circuit designs of small projects and mini-projects using Verilog code in Xilinx Vivado Design suite. I have also worked with various boards like Zynq-7000, Spartan 7, and others. My industrial knowledge includes Analog Electronics, Digital Electronics, Microprocessor, Network Theory, Control System, Integrated Circuits, FPGA, etc. I am well-versed in various IDEs like Xilinx Vivado, NI Multisim, Octave, Cadence Virtuoso, KeilUVision, LabView, etc. I have knowledge of Xilinx Vivado Debug and Verification, Simulation Process, and programming languages like C, Verilog, Python, Matlab, Assembly Language, Embedded C. I have experience working with OS like Linux, Unix, and Windows.
Education	DIPLOMA Institute Name:- K H Kabbur Institute Of Technology, Vidyagiri, Dharwad Field Of Study:- Electronics And Communication Period of study:- July 2015 to Dec 2018 PERCENTAGE SECURED:- 73.52% BACHELOR'S OF ENGINEERING Institute Name:- Kls's VishwanathRao Deshpande Institute Of Technology, Haliyal Field Of Study: - Electronics And Communication period of study: - July 2019 to July 2022 Percentage Secured: - 71.2% & CGPA Scored: - 7.52/10
Internship	Haegl Technologies Pvt Ltd, Dharwad Specialization:- Artificial Intelligence And Internet Of Things TIME PERIOD:- 01st September 2021 To 30th September 2021
Work History	ZKTeco International Technical Support Center, Bangalore, Karnataka Technical Associate Engineer Time Period:- Oct 2022 – Present

SKILLS & ABILITIES	Fundamentals Of Digital And Analog Circuits, Design Methodologies, Design Flow, Analog Circuit Design, Digital Electronics, Microprocessors, Network Theory, Control System, Process Control. C, Verilog, Python, Matlab, Assembly Language, Embedded C, Hardware Description Languages Xilinx Vivado, NI Multisim, Octave, Cadence Virtuoso, KeilUvision, LabVIEW Jira Management, Linux, Xshell.
Academic CERTIFICATES	Design of VLSI System and Verification of Digital Circuits using Cadence Virtuoso Simulation Tool
CERTIFICATES	Udemy Certifications 1. Verilog for An FPGA Engineer With Xilinx Vivado Design Suite 2. Verilog HDL VLSI Hardware Design Comprehensive Masterclass 3. FPGA Turbo Series-Communication Protocol Coursera Certifications 1. Introduction To Internet Of Things 2. Digital Electronics Circuits 3. VLSI Physical Design With Timing Analysis (Ongoing) 4. CMOS Digital VLSI Design (Ongoing)
PROJECTS	1. Blinking LED using 555 timers 2. A stable Multivibrator (Mini-Project @ Diploma) 3. Smart Train System (Final Year Project @ Diploma) 4. Heart Beat Sensor using Arduino (Mini-Project @ Engineering) 5. IOT based Industry Security Automation using Raspberry Pi (Final year Project @ Engineering)