Kerilee Bookleiner HW 5

1.

Event	P1	P2	P3	Bus Operations
Initial State	Invalid	Invalid	Invalid	
P1 writes A = 4	A = 4(modified)	Invalid	Invalid	RtW(A)
P3 writes B = 2	A = 4(modified)	Invalid	B = 2(modified)	RtW(B)
P2 reads A	A = 4(shared)	A = 4(shared)	B = 2(modified)	R(A), WB(A)
P3 reads A	A = 4(shared)	A = 4(shared)	A = 4(shared)	WB(B), R(A)
P3 writes A = 12	Invalid	Invalid	A = 12(modified)	RtW(A)
P2 reads A	Invalid	A = 12(shared)	A = 12(shared)	R(A), WB(A)
P1 reads B	B = 2(shared)	A = 12(shared)	A = 12(shared)	R(B)
P1 writes B = 10	B = 10(modified)	A = 12(shared)	A = 12(shared)	RtW(B)

2. A. Processor R issues a “write” into block a

- R sends a request to P to have block a as “exclusive”
- P sets the state of block a to “exclusive”
- P sends block a to R
- P informs R of block a’s other sharers (Q)
- R sets block a’s state to “exclusive”
- R sends invalidating messages to each sharer (Q)
- Q sets block a to invalid

B. Processor R issues a “read” into block b

- R sends read request of block b to P
- P informs R that block b is “exclusive” in Q
- R sends read request of block b to Q
- Q sends block b to R
- R stores block b where block c was previously stored
- Q and R set block b to “shared”
- Q informs P that it should change the state of block b to “shared”