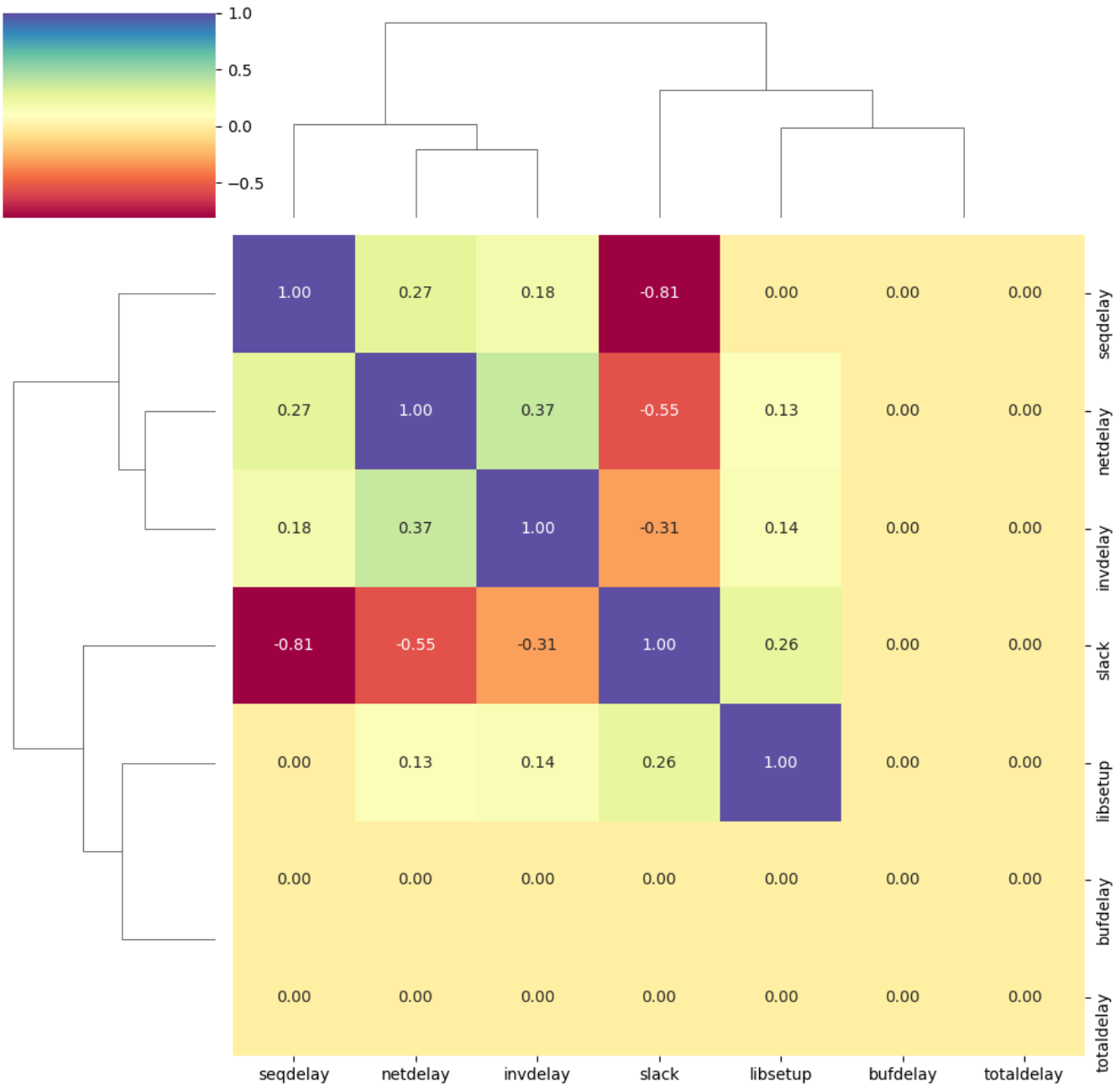
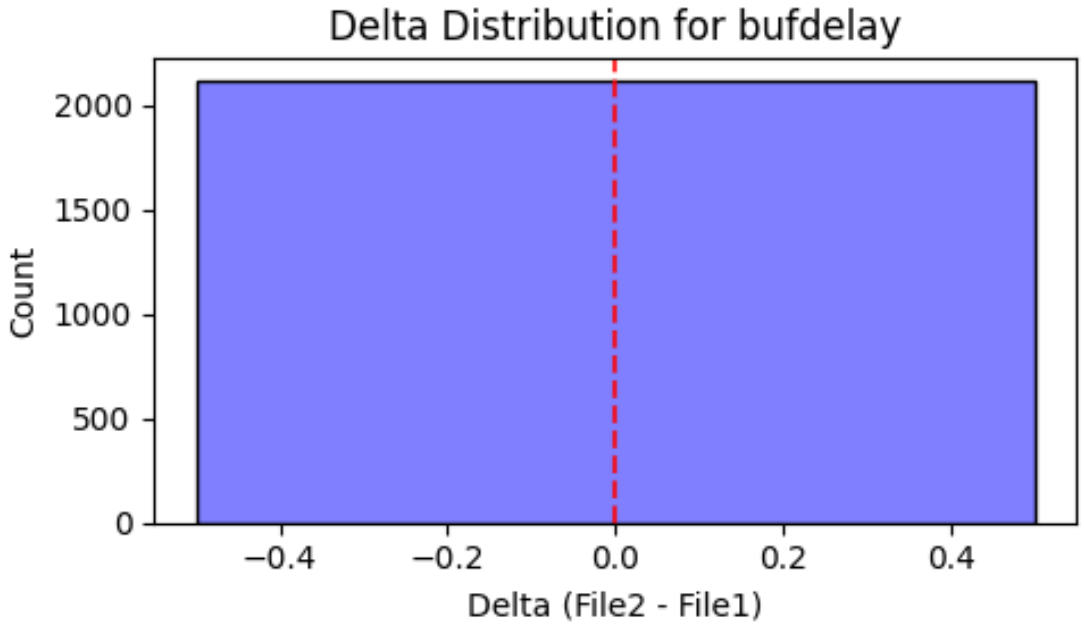
# Root Cause Analysis Report: fp_timing_f vs cts_timing_f



Above is a clustered correlation map for the computed delta data (fp_timing_f - cts_timing_f).

**Column: bufdelay (Delta)**




Key Delta Statistics:

Mean: 0.0000

Std: 0.0000

Min: 0.0000

25%: 0.0000

50%: 0.0000

75%: 0.0000

Max: 0.0000

Root Cause Analysis:

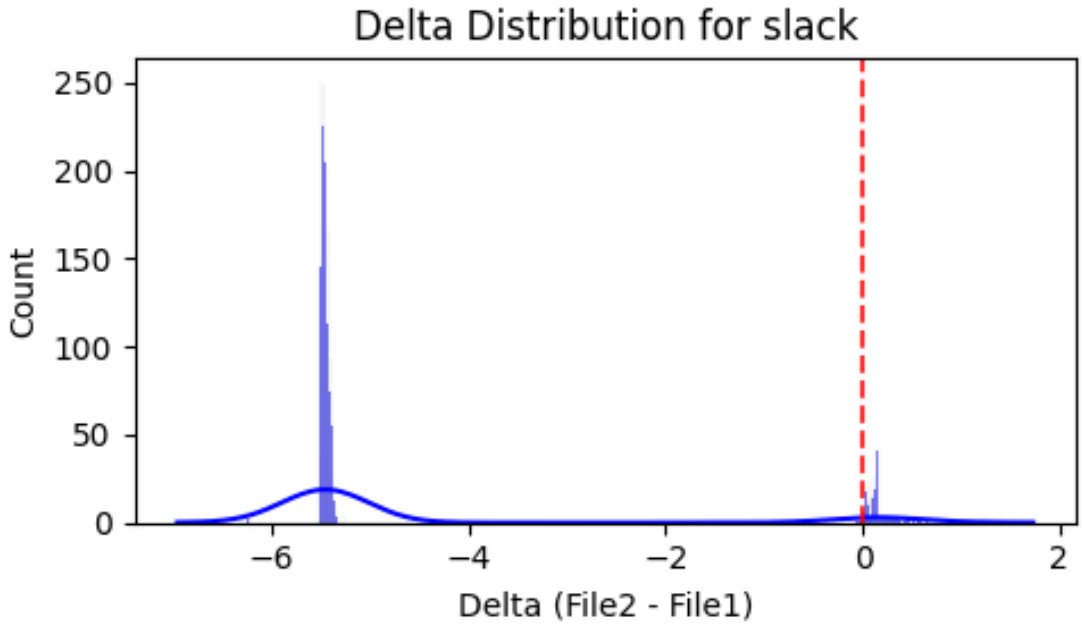
- Problem: No significant timing issue detected. The buffer delays are consistent across both files.

- Cause: The mean, standard deviation, minimum, maximum, and percentiles of the buffer delay values are all zero, indicating that there is no variation or shift in the delays between the two files.

- Solution: Since there is no issue detected, no action is required at this time.

- Prevention: Ensure proper design methodologies and verification processes are followed to maintain consistency in designs and avoid any potential timing issues. Regularly review and update design rules and constraints to account for process, voltage, and temperature (PVT) variations.

**Column: slack (Delta)**




Key Delta Statistics:

Mean: -4.6110

Std: 2.0327

Min: -6.9530

25%: -5.4760

50%: -5.4500

75%: -5.4010

Max: 1.7330

Root Cause Analysis:

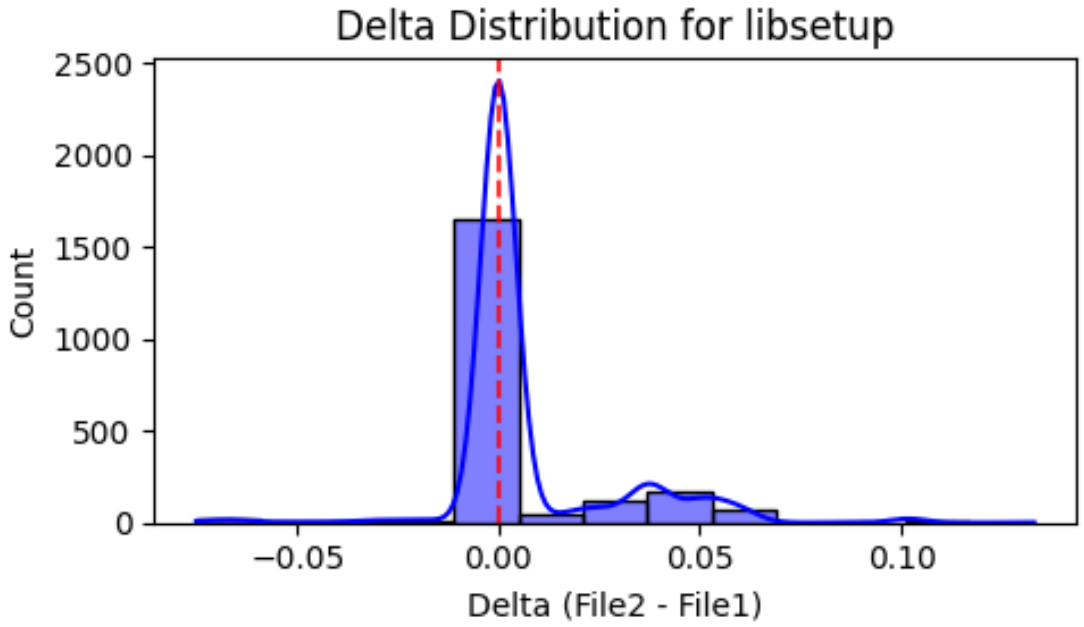
- Problem: Timing Slack Deficit

- Cause: The mean slack value has decreased significantly (from File1 to File2), indicating that the timing of the circuit has worsened. This could be due to changes in logic, clock frequency, or routing delays.

- Solution: Review the design for any logic changes that may have increased path delays, adjust clock frequency if possible, and optimize routing to minimize interconnect delays.

- Prevention: Implement timing-driven design methodologies, perform regular timing analysis throughout the design process, and consider using design techniques such as buffering, clock gating, or delay tuning to maintain sufficient timing slack.

**Column: libsetup (Delta)**




Key Delta Statistics:

Mean: 0.0075

Std: 0.0202

Min: -0.0750

25%: 0.0000

50%: 0.0000

75%: 0.0000

Max: 0.1330

Root Cause Analysis:

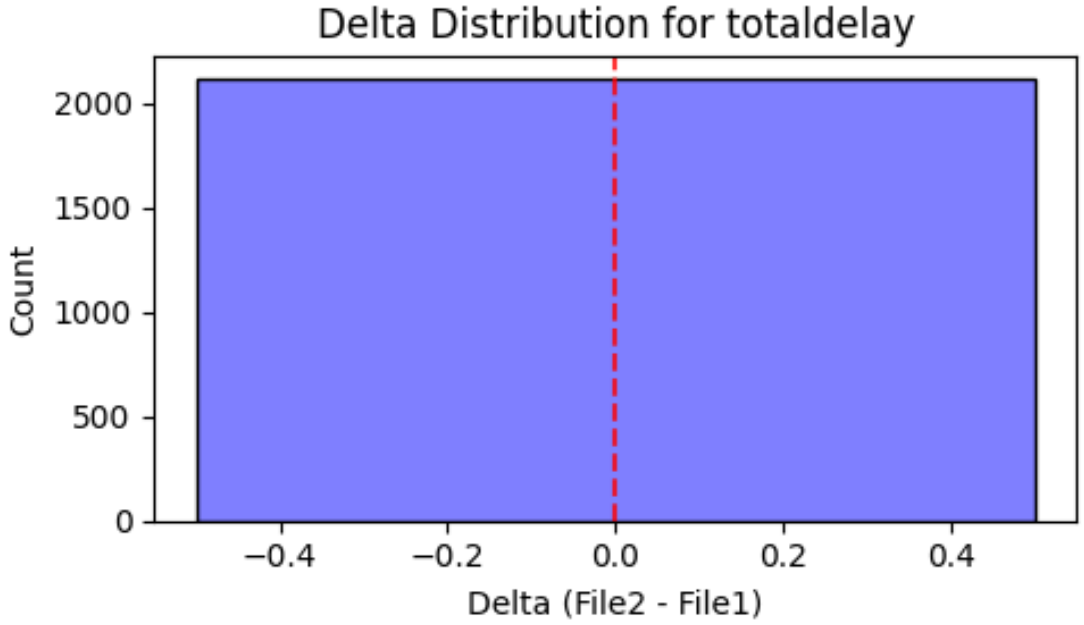
- Problem: Significant timing variation between the two files (File2 and File1)

- Cause: The large standard deviation (Std: 0.020) and maximum value (Max: 0.133) suggest that there might be differences in the design, routing, or process variations between the two files.

- Solution: Analyze the designs of both files to identify any discrepancies in logic, clock tree, or power/ground distribution. Perform detailed routing checks and ensure that the design rules are being followed consistently.

- Prevention: Implement design for timing (DFT) methodologies early in the design process to minimize timing variations. Use consistent design styles across the project and perform thorough design rule checking (DRC). Optimize clock trees and power/ground distribution networks to reduce timing skew and delay variation.

**Column: totaldelay (Delta)**




Key Delta Statistics:

Mean: 0.0000

Std: 0.0000

Min: 0.0000

25%: 0.0000

50%: 0.0000

75%: 0.0000

Max: 0.0000

Root Cause Analysis:

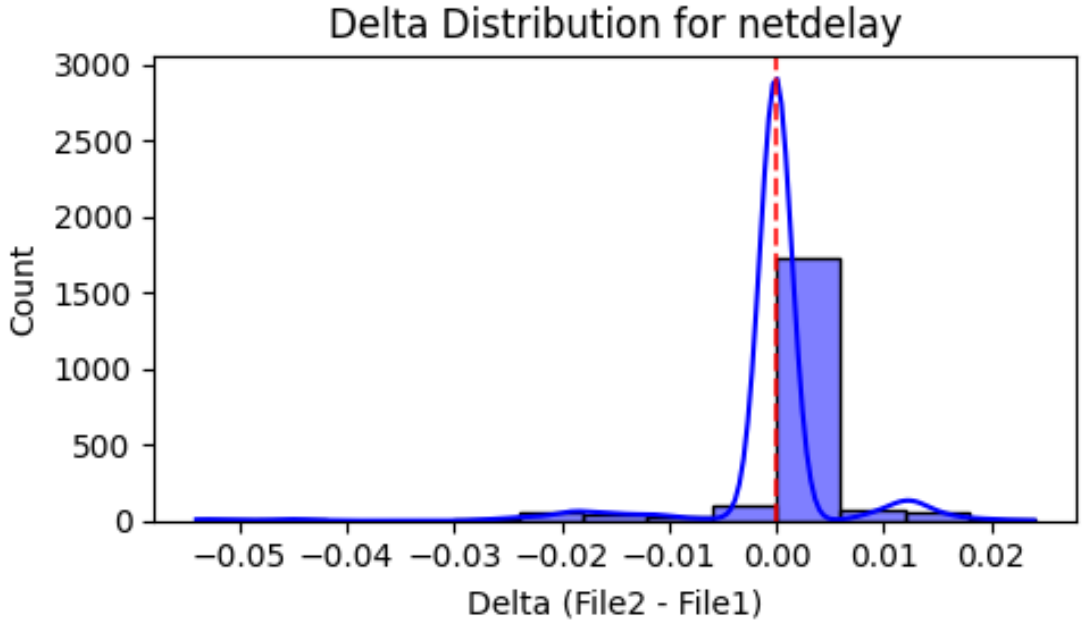
- Problem: No significant timing issue detected.

- Cause: The delta analysis shows no meaningful difference between the two files, indicating that there are no major design changes or timing shifts.

- Solution: Since there is no issue, no action is required at this moment. Continue with the current design flow.

- Prevention: Ensure thorough design reviews and verification checks to catch any potential issues early in the design cycle. Regularly compare designs using delta analysis to identify any changes that might affect timing.

**Column: netdelay (Delta)**




Key Delta Statistics:

Mean: -0.0005

Std: 0.0068

Min: -0.0540

25%: 0.0000

50%: 0.0000

75%: 0.0000

Max: 0.0240

Root Cause Analysis:

- Problem: Negative mean net delay and large negative delta values indicate potential timing

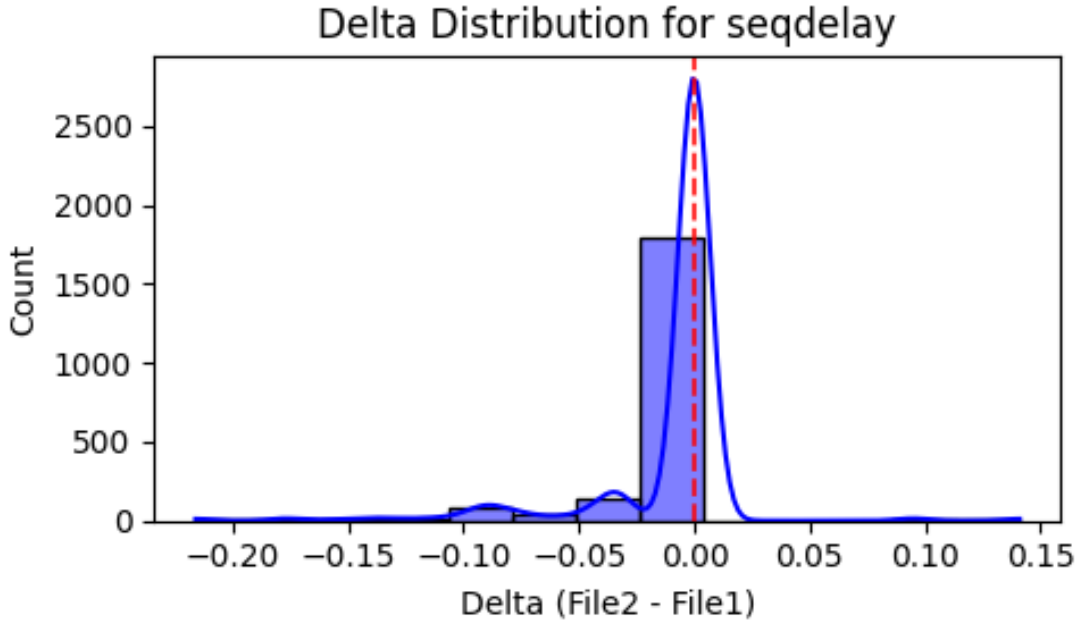
issues.

- Cause: The cause could be a design issue such as insufficient buffer insertion, long critical paths, or improperly sized clock trees. It may also be due to process, voltage, or temperature (PVT) variations that have shifted the timing.

- Solution: Review the design for appropriate buffer placement, optimize the routing and clock tree, and consider using timing-driven placement and routing tools. Adjust the design to meet the specified timing constraints.

- Prevention: Implement timing-aware design methodologies from the start of the design flow. Use statistical timing analysis to account for PVT variations. Regularly monitor and adjust the design during the development process to maintain timing closure.

**Column: seqdelay (Delta)**




Key Delta Statistics:

Mean: -0.0096

Std: 0.0322

Min: -0.2160

25%: 0.0000

50%: 0.0000

75%: 0.0000

Max: 0.1410

Root Cause Analysis:

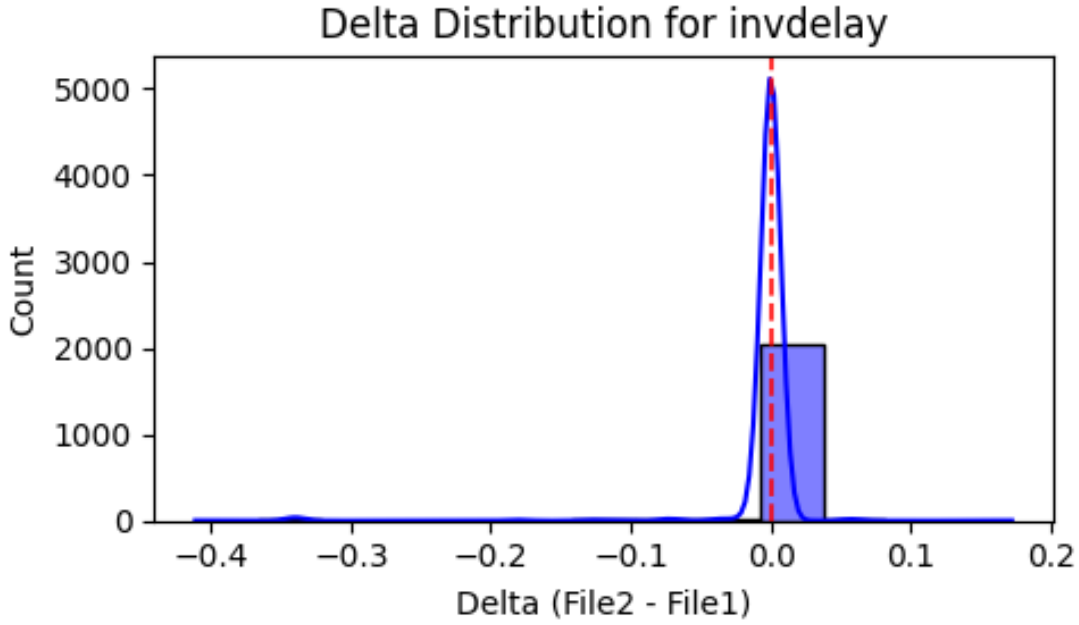
- Problem: Sequential delay is negative, indicating a potential timing violation.

- Cause: This could be due to slowing down of the sequential path (flip-flop) or an increase in load capacitance, or both. It might also be caused by improperly sized clock trees, incorrect clock skew compensation, or routing congestion affecting signal integrity.

- Solution: Optimize the design for speed by reducing the load on the flip-flops (e.g., minimizing fanout, optimizing logic depth), improving clock tree synthesis and routing, and ensuring proper clock skew compensation.

- Prevention: Perform thorough timing analysis during the design stage to identify potential bottlenecks and address them proactively. Use design for testability (DFT) techniques to monitor and control the timing of critical paths. Implement guard bands in the timing budget to account for process, voltage, and temperature variations.

**Column: invdelay (Delta)**




Key Delta Statistics:

Mean: -0.0037

Std: 0.0328

Min: -0.4110

25%: 0.0000

50%: 0.0000

75%: 0.0000

Max: 0.1720

Root Cause Analysis:

- Problem: Negative mean delay and skewed distribution towards negative values, indicating

potential timing issues.

- Cause: The design may have critical paths with insufficient drive strength, long wirelengths, or high capacitive loads that result in delays exceeding the specified clock period. Additionally, there might be process, voltage, or temperature variations causing timing shifts.

- Solution: Optimize the design by reducing wirelengths, increasing drive strengths, and minimizing capacitive loads where possible. Consider using timing-optimized standard cells, buffering critical paths, and adding guard rings to reduce coupling effects. Perform clock tree synthesis for better clock distribution.

- Prevention: During the design phase, perform thorough timing analysis early and iteratively throughout the design flow. Use timing-aware placement and routing tools to optimize for timing and minimize delays. Ensure that the design meets the specified timing requirements before proceeding to the next stage of development. Additionally, consider using design methodologies such as power-optimized or area-optimized styles based on the specific application's requirements.

**Thank you for using the Timing Data Delta Analysis!**