Biyani's Think Tank

Concept based notes

Advanced Computer Architecture

(BCA-III Year)

Nitika Newar, MCA
Revised By: Namarta
Dept. of Information Technology
Biyani Girls College, Jaipur

Published by :

Think Tanks

Biyani Group of Colleges

Sector-3, Vidhyadhar Nagar,

Jaipur-302 023 (Rajasthan)

Ph : 0141-2338371, 2338591-95 • Fax : 0141-2338007

E-mail : acad@biyanicolleges.org

Website :www.gurukpo.com; www.biyanicolleges.org

Edition : 2011

Price :

Leaser Type Setted by :

Biyani College Printing Department

Preface

I am glad to present this book, especially designed to serve the needs of the students. The book has been written keeping in mind the general weakness in understanding the fundamental concepts of the topics. The book is self-explanatory and adopts the "Teach Yourself" style. It is based on question-answer pattern. The language of book is quite easy and understandable based on scientific approach.

Any further improvement in the contents of the book by making corrections, omission and inclusion is keen to be achieved based on suggestions from the readers for which the author shall be obliged.

I acknowledge special thanks to Mr. Rajeev Biyani, *Chairman* & Dr. Sanjay Biyani, *Director* (*Acad.*) Biyani Group of Colleges, who are the backbones and main concept provider and also have been constant source of motivation throughout this Endeavour. They played an active role in coordinating the various stages of this Endeavour and spearheaded the publishing work.

I look forward to receiving valuable suggestions from professors of various educational institutions, other faculty members and students for improvement of the quality of the book. The reader may feel free to send in their comments and suggestions to the under mentioned address.

Author

Syllabus

B.C.A. Part-III

Advanced Computer Architecture

Parallel Computer Models : The state of computing, multiprocessors and multicomputer, multivector and SIMD computers, architectural development tracks.

Program and Network Properties : Conditions of parallelism, program partitioning and scheduling, program flow mechanisms.

System Interconnect Architectures : Network properties and routing, Static interconnection network and dynamic intercommection networks.

Processors and Memory Hierachy : Advanced processor technology—CISC, RISC, Superscalar, Vector VLIW and symbolic processors, memory technology.

Bus, Cache and Shared Memory.

Linear Pipeline Processors, Nonlinear Pipeline, processors Instruction pipeline Design Multiprocessors System Interconnects Vector Processing Principles, Multivector Multiprocessors.

Content

Chapter 1
Parallel Computer Models

Q.1. What is multiprocessors? What are the types of multi-processors?

Ans. A multiprocessor structure is an interconnection of two or more than two CPUs with memory as input-output apparatus. Multiprocessors are grouped as multiple instruction stream, multiple data stream (MIMD) systems.

some similarities are found between multiprocessor & multicomputer organization since both support simultaneous operations. However there is an important peculiarity between a system with multiple computers & a system with multiple processors. Computers are interconnected with each other with communication lines to make a computer network. The network comprise of numerous autonomous computers that may or may not converse with each other. A multiprocessor system is governed by one operating system that present inter-connection between processors & all the units of the system assist in the solution of a problem very large scale integrated circuit technology has abridged the cost of computer to such a low level that the concept of applying multiple processors to meet system performance needs has turn out to be an smart design prospect.
Multiprocessing develop the trustworthiness of system so that a failure or error in one part has narrowed impact on rest of system. If a fault roots one processor to fail, a second processor can be allocated to complete the functions of disabled processor. The entire system can keep on functioning suitably with possibly some loss in efficiency. The benefits resulting from a multiprocessor organisation is better system performance. The system derives its high performance from the fact that manipulation can advance in parallel in one of two ways:

1. Multiple independent tasks can be completed to work in parallel.

2. A single task can be divided into multiple parallel tasks.

Example 1. a computer system where are processor performs the computations for an industrial process control while others monitors control various parameter such as temperature and flow rate.

Example 2. a computer where are processor performs high speed floating point mathematical computations and another take care of routine data processing tasks.

Multiprocessing can improve performance by decomposing a program into parallel executable tasks. This can be achieved in one of two methods:

The user can explicitly declare that certain tasks of the program be executed in parallel. This must be done prior to load the program by specifying the parallel executable segments. Most multiprocessor constructs give an operating system with programming language construct appropriate for identifying parallel processing.

The other, more efficient way is to provide a compiler with multiprocessor software that can automatically detect parallelism in a users's program. The compiler checks for data dependency in the program. If a program depends on data generated in another part, the part yielding the needed data must be executed first. However two parts of a program that do not use data generated by each can run concurrently. The parallelizing compiler checks the complete program to detect any possible data dependence. These that have no data dependency are then measured for concurrent scheduling on different processors.

Multiprocessors are grouped according to their memory is organized. A multiprocessor system with common shared memory is grouped as shared memory (tightly coupled) multiprocessor. This does not prohibit each processor from having its own local memory. In fact, most commercial tightly coupled multiprocessor offer a cache memory with each CPU. In addition there is a global general memory that all CPUs can access. Information can thus be shared amid the CPU by placing it in the general global memory.

An alternative model of microprocessor is the distributed memory or loosely coupled system. Each processor element in a loosely coupled system has its own private local memory. The processors are tied together by a switching scheme designed to route information from one processor to another through a message passing scheme. The processors relay program is data to other processors in packets. A packet consists of an address, the data content and some error detection code. The packets are addressed to a specific processor or taken by first available processor, depending on the communication system used. Loosely coupled systems are most efficient when the interaction between tasks is minimal, whereas tightly coupled systems can tolerate a higher degree of interaction between tasks.

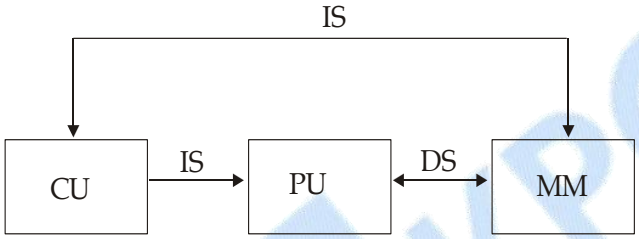
Q.2. What is parallel processing?

Ans. Parallel processing refer to a huge class of method that are used to offer simultaneous data processing jobs for increasing the computational speed of system. as an alternative of processing each instruction sequentially as in conventional computer, a parallel processing system is able to carry out concurrent data processing to attain faster execution time. The idea of parallel

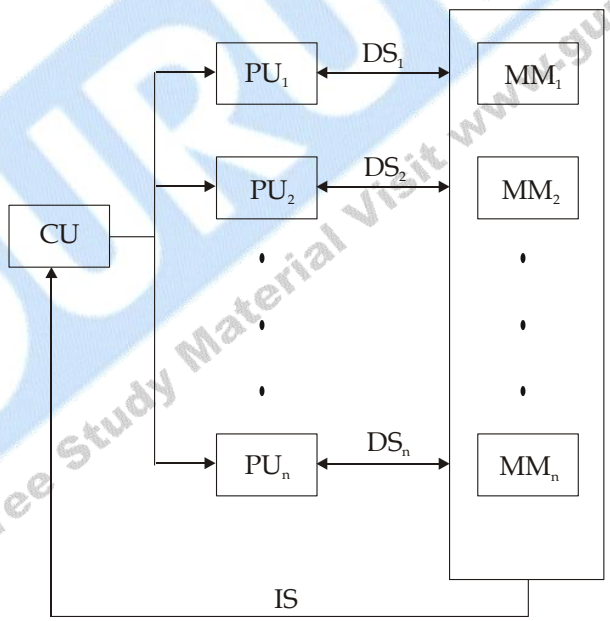
processing is to speed up the computer processing capability also increase its throughput, i.e., the amount of processing that can be done during an interval of time. Parallel processing at higher level of complexity can be realized by including multiplicity of functional units that do identical or different operations concurrently. Parallel processing is recognized by giving out the data among the multiple functional units. For example the arithmetic logic and shift operations

can be alienated into three units and the operands diverted to each unit under the supervision of control unit.

Singe Instruction stream – Single Data Stream (SISD)



Single Instruction Multiple Data Stream (SIMD)



CU: Control Unit

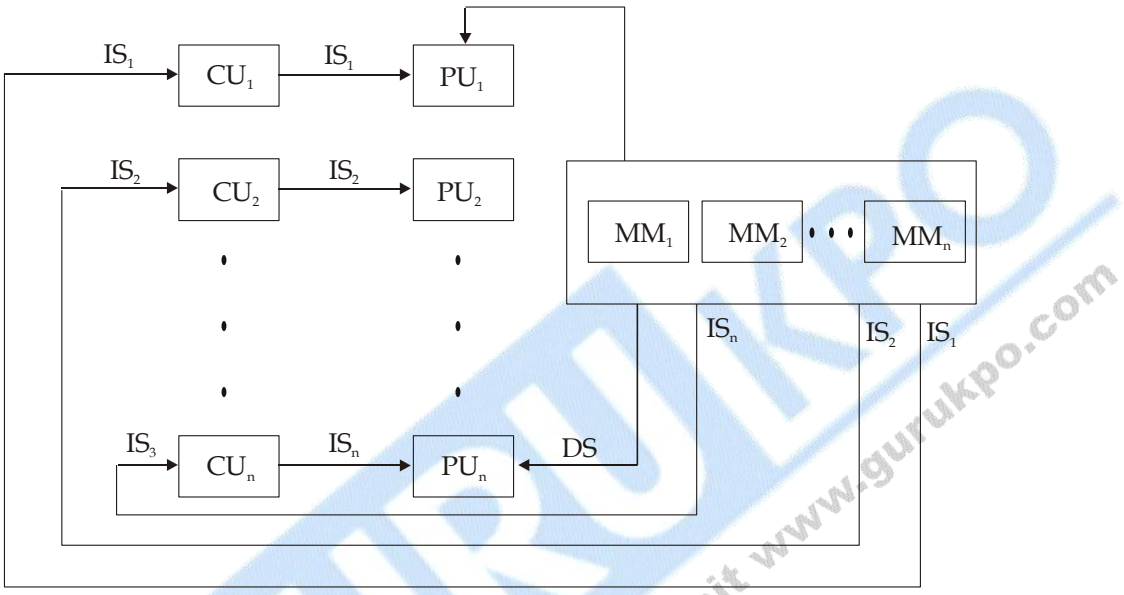
PU: Processing Unit

MM: Memory Module

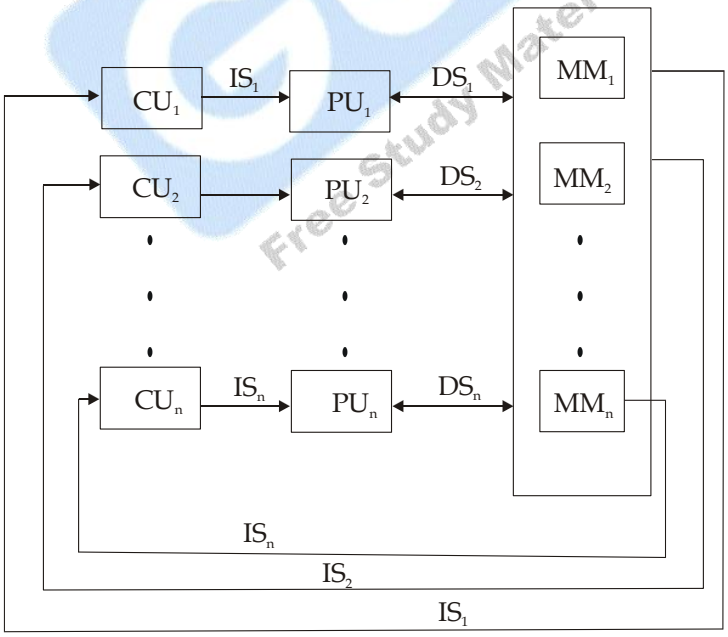
These are divers of ways that parallel processing can be classified. One classification introduced by M.J. Flynn considers the organization of computer system by number of instructions and data items that are manipulated simultaneously. The normal operation of a computer is to fetch instructions

from memory and execute them in the processor. The sequence of instructions read from memory constitutes an instruction stream. The operations performed on the data is processor constitutes a data stream parallel processing may be occur in the instruction stream, in data stream or both.

- Single instruction stream, single Data stream (SISD)
- Single instruction stream, multiple data stream (SIMD)
- Multiple instruction stream, single data stream (MISD)
- Multiple instruction stream, multiple data stream (MIMD)



Multiple Instruction Stream Single Data Stream (MISD)



Multiple Instream stream Multiple Data Stream (MIMD)

Q.3. Explain the state of computing?

Ans. Modern computers are equipped with powerful hardware facilitates driven by extensive software packages. To asses the state of computing we first review historical milestones in the development of computers.

Computer Generations

Over the past five decades, electronic computers have gone through fine generations of development. Each of first three generations lasted about 10 years. The fourth generations covered a time span of 15 years. We have just entered the fifth generations with the use of processors & memory devices with more than 1 million transistors on solo silicon chip. The table shows the new hardware and software features introduced with each generation. Most features introduced in earlier generations have been passed to later generations.

Five Generations of Electronic Computers

Generation	Technology & Architecture	Software & Application	Representative System
First (1945-54)	Vaccuum tubes & relay memories, CPU motivated by Pc & accumulator, fixed point arithmetic.	Machine/assembly languages, single user, no subroutine linkage, programmed I/O using CPU.	ENIAC, Princeton, IAS, IBM 701
Second (1955-64)	Discrete transistors and core memories, floating point arithmetic, I/O processors, multiplexed memory access.	HLL used with compilere, subroutine libraries, batch processing monitor. Multiprogramming & time sharing OS, multi user applications.	IBM 7090, CDC 1604, Univac LARC.
Third (1965-74)	Integrated circuits (SSI-MSI), microprogramming, pipelining, cache & lookahead processors.	Multiprocessor OS, languages, compilers & environment for parallel processing.	IBM 360/370, CDC 6600, TI- ASC, PDP-8
Fourth (1975-90)	LSI/VLSI & semi conductor memory, multiprocessors, vector supercomputers, multi computers.	Massively parallel processing, grand challenge applications, heterogenous processing.	VAX 9000, Gay XMP, IBM 3090 BBN TC 2000
Fifth (1991 present)	ULSI/VHSIC processors, memory & switches, high density packaging, scalable architectures.		Fujitsu VPP 500, Gay/MPP, TMC/CM-5, Intel paragon.

In other words, the latest generation computers have inherited all the bad ones found in previous generations.

Q.4. How is computer Architecture developed?

Ans. Over the past four decades, computer architecture has gone through evolutional rather than revolution changes sustaining features are those that were proven performance delivers.

According to the figure we started with the Von Neumann architecture built as a sequential machine executing scalar data. Sequential computers improved from bit serial to word-parallel operations & from fixed point to floating point operations. The Von Neumann architecture is slow due to sequential execution of instructions in programme.

Lookahead, Paralleism and Pipelining : Lookahead techniques were begin to prefetch instructions in order to overlap I/E (instruction fetch/decode and execution) operations and to enable functional parallelism. Functional parallelism was supported by two approaches: One is to use multiple functional units simultaneously and the other is to practice pipelining at various processing levels.

The latter embrace pipelined instruction execution, pipelined arithmetic computations and memory access operations. Pipelining has proven especially attractive in performing identical operations repeatedly over vector data strings. Vectors operations were originally carried out implicitly by software controlled looping using scalar pipeline processors.

Flynn's Classification: Michael Flynn (1972) established nomenclature of a variety of computer architectures based on concept of instruction and data streams. Traditional sequential machines are SISD (single instruction stream over a single data stream). Vector computers are set with scalar and vector hardware or emerge as SIMD (single instruction stream over multiple data streams). Parallel computers are called MIMD (multiple instruction streams over multiple data streams) machines.

Q.5. What is Parallelism? What are the various conditions of parallelism

Ans. Parallelism is the major concept used in today computer use of multiple functional units is a form of parallelism within the CPU. In early computer only one arithmetic & functional units are there so it cause only one operation to execute at a time. So ALU function can be distributed to multiple functional units, which are operating in parallel.

H.T. Kung has recognized that there is a need to move in three areas namely computation model for parallel computing, inter process communication in parallel architecture & system integration for incorporating parallel systems into general computing environment.

Conditions of Parallelism :

1. Data and resource dependencies : A program is made up of several part, so the ability of executing several program segment in parallel requires that each segment should be independent other segment. Dependencies in various segment of a program may be in various form like resource dependency, control depending & data depending. Dependence graph is used to describe the relation. Program statements are represented by nodes and the directed edge with different labels shows the ordered relation among the statements. After analyzing dependence graph, it can be shown that where opportunity exist for parallelization & vectorization.

Data Dependencies: Relation between statements is shown by data dependences. There are 5 types of data dependencies given below:

(a) Antidependency: A statement S_2 is antidependent on statement ST_1 if ST_2 follows ST_1 in order and if the output of ST_2 overlap the input to ST_1.

(b) Input dependence: Read & write are input statement input dependence occur not because of same variables involved put because of same file is referenced by both input statements.

(c) Unknown dependence: The dependence relation between two statement cannot be found in following situation

- The subscript of variable is itself subscribed.
- The subscript does not have the loop index variable.
- Subscript is non linear in the loop index variable.

(d) Output dependence: Two statements are output dependence if they produce the same output variable.

(e) Flow dependence: The statement ST_2 is flow dependent if an statement ST_1, if an expression path exists from ST_1 to ST_2 and at least are output of ST, feeds in an input to ST_2.

2. Bernstein's condition : Bernstein discovered a set of conditions depending on which two process can execute in parallel. A process is a program that is in execution. Process is an active entity. Actually it is an stumbling block of a program fragment defined at various processing levels. I_i is the input set of process P_i which is set of all input variables needed to execute the process similarly the output set of consist of all output variable generated after execution of all process P_i. Input variables are actually the operands which are fetched from the memory or registers. Output variables are the result to be stored in working registers or memory locations.

Let there are 2 processes P_1 & P_2

Input sets are I_1 & I_2

Output sets are O_1 & O_2

The two processes P_1 & P_2 can execute in parallel & are directed by P_1/P_2 if & only if they are independent and do not create confusing results.

3. Software Parallelism : Software dependency is defined by control and data dependency of programs. Degree of parallelism is revealed in the program profile or in program flow graph. Software parallelism is a function of algorithm, programming style and compiler optimization. Program flow graphs shows the pattern of simultaneously executable operation. Parallelism in a program varies during the execution period.

4. Hardware Parallelism : Hardware Parallelism is defined by hardware multiplicity & machine hardware. It is a function of cost & performance trade off. It present the resource utilization patterns of simultaneously executable operations. It also indicates the performance of the processor resources.

One method of identifying parallelism in hardware is by means by number of instructions issued per machine cycle.

Q.6. What are the different levels of parallelism :

Ans. Levels of parallelism are described below:

1. Instruction Level : At instruction level, a grain is consist of less than 20 instruction called fine grain. Fine grain parallelism at this level may range from two thousands depending an individual program single instruction stream parallelism is greater than two but the average parallelism at instruction level is around fine rarely exceeding seven in ordinary program. For scientific applications average parallel is in the range of 500 to 300 fortran statements executing concurrently in an idealized environment.

2. Loop Level : It embrace iterative loop operations. A loop may contain less than 500 instructions. Some loop independent operation can be vectorized for pipelined execution or for look step execution of SIMD machines. Loop level parallelism is the most optimized program construct to execute on a parallel or vector computer. But recursive loops are different to parallelize. Vector processing is mostly exploited at the loop level by vectorizing compiler.

3. Procedural Level : It communicate to medium grain size at the task, procedure, subroutine levels. Grain at this level has less than 2000 instructions. Detection of parallelism at this level is much more difficult than a finer grain level. Communication obligation is much less as compared with that MIMD execution mode. But here major efforts are requisite by the programmer to reorganize a program at this level.

4. Subprogram Level : Subprogram level communicate to job steps and related subprograms. Grain size here have less than 1000 instructions. Job steps can overlap across diverse jobs. Multiprogramming an uniprocessor or multiprocessor is conducted at this level.

5. Job Level : It corresponds to parallel executions of independent tasks on parallel computer. Grain size here can be tens of thousands of instructions. It is

handled by program loader and by operating system. Time sharing & space sharing multiprocessors explores this level of parallelism.

Q.7. Explain Vector super computers?

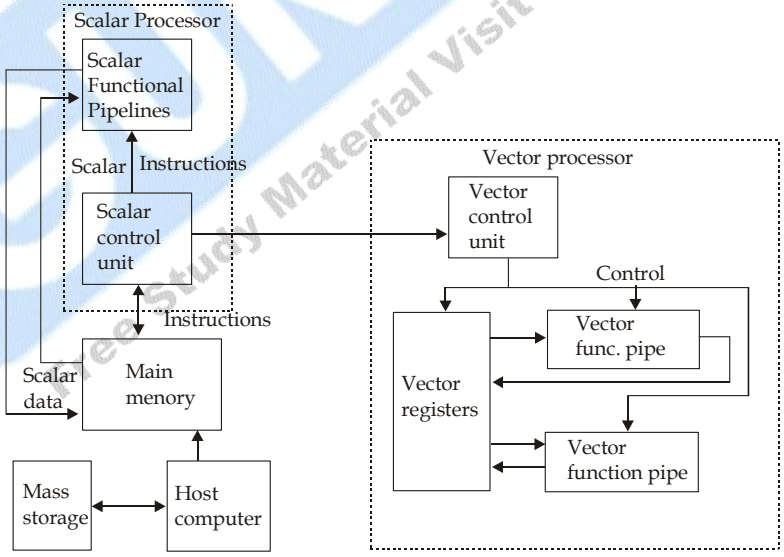
Ans. Program & data are first loaded into the main memory from a host computer. All instructions are first decoded by the scalar control unit. If the decoded instruction is a scalar operation or program control operation it will be directly executed by scalar processor using the scalar functional pipelines.

If the instruction is decoded as a vector procedure, it will be sent to the vector control unit. This control unit will supervise the flow of vector data amid the main memory & vector functional pipelines. The vector data flow is synchronized by control unit. A number of vector functional pipelines may be built into a vector processor.

Computers with vector processing capabilities are in demand in specialized applications. The following are symbolized application areas where vector processing is of utmost importance.

- Long Range weather forecasting
- Petroleum explorations
- Medical diagnosis
- Space flight simulations

Vector Processor Models



The Architecture of vector super computer

Q.8. What are the different shared memory multiprocessor models?

Ans. The most popular parallel computers are those that execute programs in MIMD mode. There are two major classes of parallel computers: shared memory multiprocessor & message – passing multi computers. The major distinction between multiprocessors & multicomputers lies in memory sharing and the mechanisms used for interprocessor communication. The processor in multiprocessor system communicate with each other through shared variable in a common memory. Each computer node in a multicomputer system has a local memory, unshared with other nodes. Inter process communication is done through message passing among nodes.

There are three shared memory multiprocessor models:-

1. Uniform memory access (UMA) model

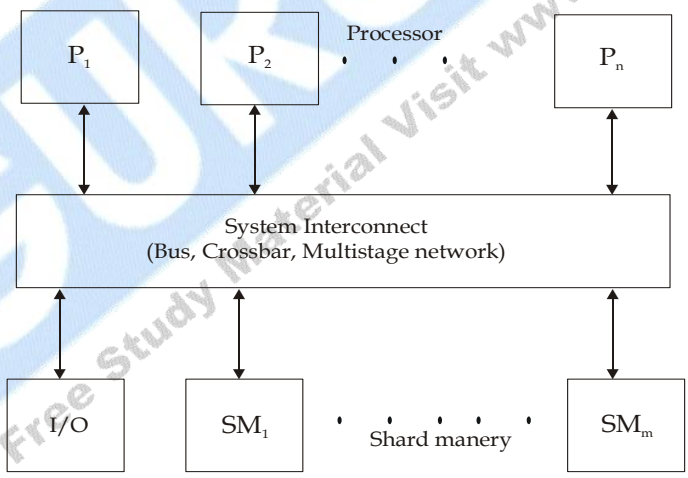
2. Non-uniform memory access (NUMA) model

3. Cache only memory Architecture (COMA) model

These models are differ in how the memory & peripheral resources are shared or distributed.

1. UMA Model:

The UMA multiprocessor model



In this model the physical memory is uniformly shared by all the processors. All processors have equal access time to all memory words, which is why it is called uniform memory access. Each processor may use a private cache. Peripherals are also shared.

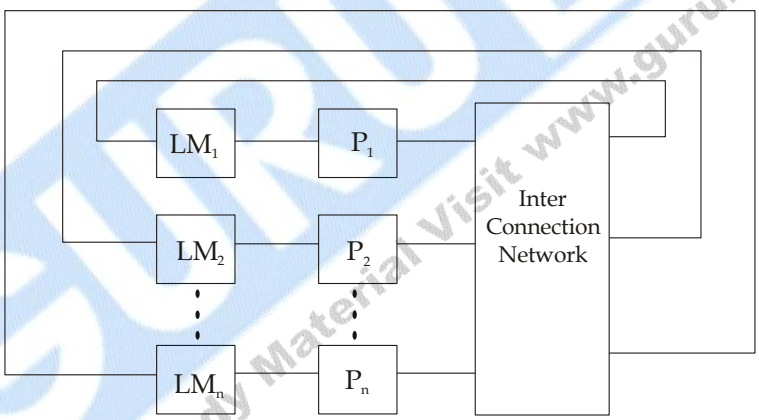
Multiprocessors are called tightly coupled systems for its high degree of resource sharing.

UMA model is suitable for time sharing applications by multiple users. It can be used to speed up the execution of single large program in time critical application.When all processors have equal access to all peripheral devices, the system is called a symmetric multiprocessor. In this case, all the processors are equally capable of running programme, such as kernel.

In an asymmetric multiprocessor, only one or subset of processors are executive capable. An executive or master processor can execute the operating system and handle I/O. The remaining processors called attached processors (AP) runs user code under the supervision of master processor.

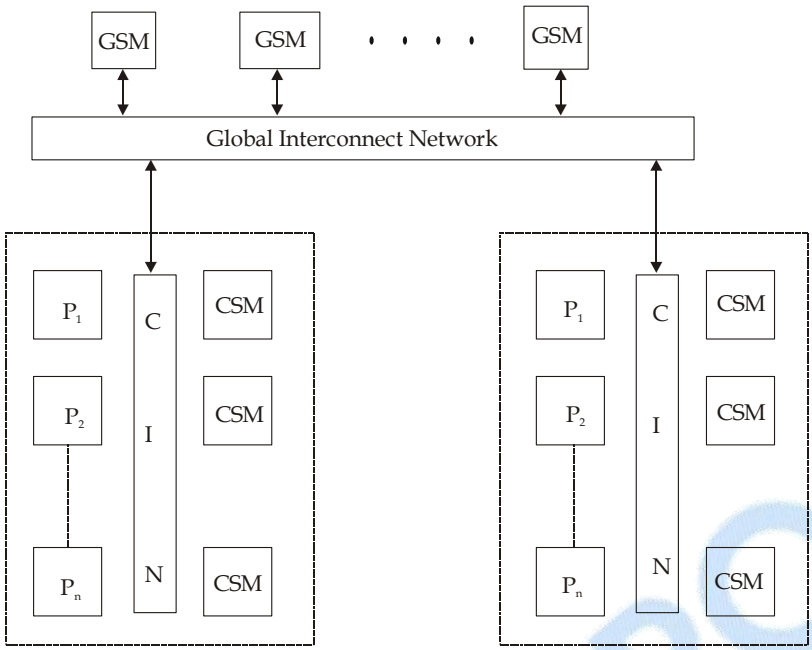
2. NUMA model: A NUMA multiprocessor is a shared memory system in which the access time diverge with the location of memory word. Two NUMA machine models are depicted. The shared memory is physically distributed to all processors, called local memories. The collection of all local memories forms a global address space accessible by all processors.

It is quicker to access a local memory with a local processor. The access of remote memory attached to other processors takes longer due to the added delay through the interconnection network.



Shared Local Memories

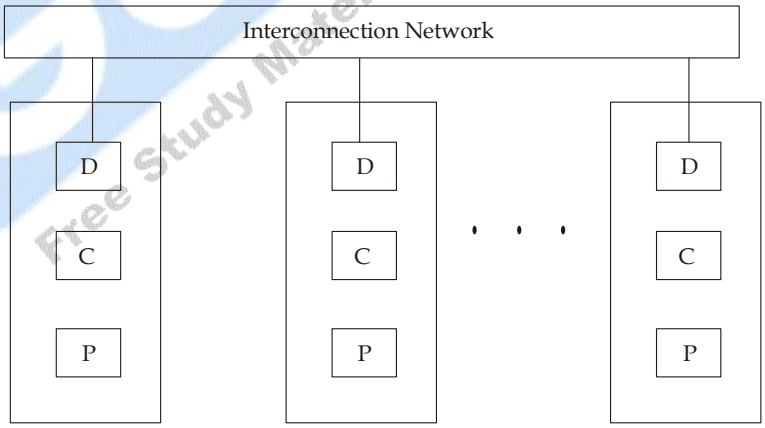
In the hierarchial cluster Model processors are divided into several clusters. Each cluster may be UMA or NUMA Each cluster is connected to shared memory modules. All processors of a single cluster uniformally access the cluster shared memory modules. All cluster equally access to global memory access time to cluster memory is shorter then that of global memory.



A hierarchical cluster models

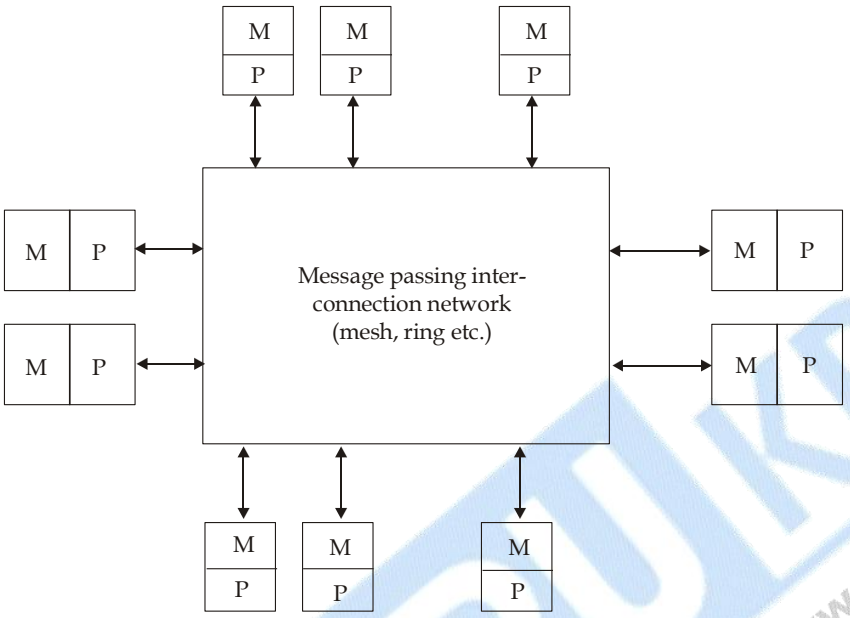
3. Cache Only Memory Architecture:

This model is a special case of NUMA machine where distributed main memories are replaced with cache memory. At individual processor node, there is no memory chain of command(hierarchy). All cache made a global address space. Depending on interconnection network used, directories may be
used to help in locating copies of cache blocks example of COMA includes Swedish Institute of Computer Science's Data Diffusion machine (DDM).



Q.9. What is Distributed Memory Multicomputers?

Ans. A system made up of multiple computers(nodes), interconnected by a message passing network. Each node is autonomous computer consisting of a processor, local memory and from time to time attached disks or I/O peripherals.



All local memories are private & accessible only by local processors. This network presents point-to-point static connection among nodes. Inter node communication is carried out by passing messages through the static connection network.

Q.10. Explain SIMD Computers?

Ans. SIMD connotes single instruction stream and multiple data stream. These computers are array processors. There are multiple processing elements which are supervised under same control unit. Each processing element receives same instruction but operate on different data from distinct module,

SIMD Machine Model

An operational model of an SIMD computer is specified by 5- Triple.

M = [N, C, I, M, R]

Where

(1) N is the number of processing elements (PEs) in the machine.

(2) C is the set of instructions directly executed by control unit including scalar and program flow control instructions.

(3) I is set of instructions broadcast by CPU to all PEs for parallel execution. These include arithmetic, logic, data routing, masking and other local operations executed by each active PE over data within that PE.

(4) M is the set of masking schemes, where each mask partitions the set of PEs into enabled & disabled subsets.

(5) R is the set of data routing functions, specifying various patterns to be set up in the inter connection network for inter PE communications.

Q.11. What are the Architectural development tracks?

Ans. Architecture of todays systems pursue development tracks. There are mainly 3 tracks. These tracks are illustrious by likeness in computational model & technological bases.

1. Multiple Processor tracks: multiple processor system can be shared memory or distributed memory.

(a) Shared Memory track:

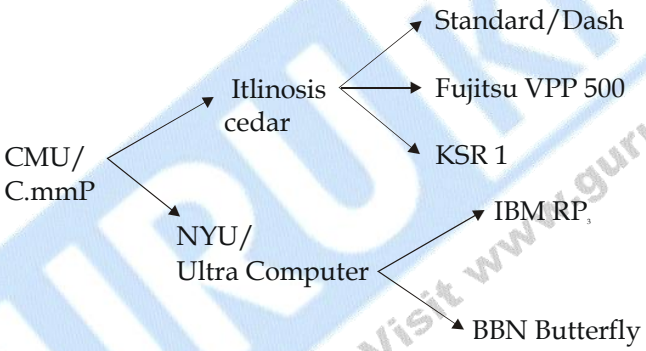


Fig. Shared Memory track

It shows track of multiprocessor development employing a single address space in the entire system c. mmp was a UMA multiprocessor. The c.mmp project poincered shared memory multiprocessor development not only in the cross architecture but in multiprocessor operating system development.

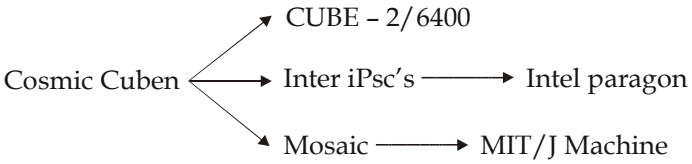
Illinois Codar project and NYO ultra computer project both were developed with a single address space. Both use multi stage network as system inter connect.

Standard Dash is a NUMA multiprocessor with distributed memory forming a global address space cache coherence is there with distributed directories.

KSR-1 is a COMA model.

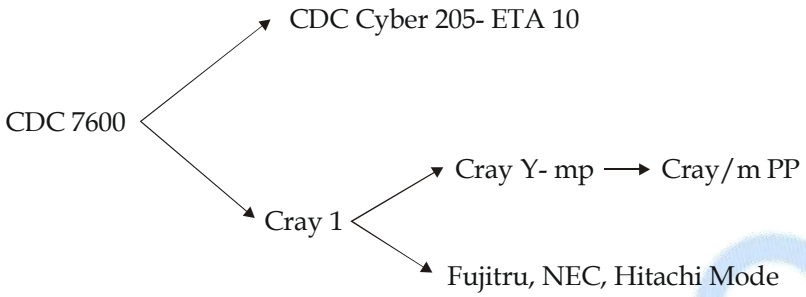
Fujitsu UPP 500 is processor system with a cross bar inter connected shared memories are distributed to all processor nodes.

(b) Message Passing track:



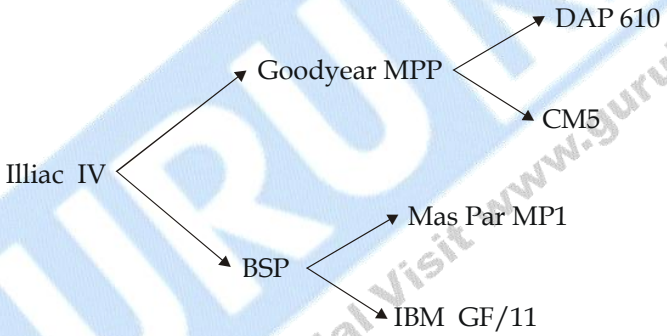
(2) Multivector & SIMD tracks

Multivector track



The CDC 7600 was first vector dual processor system. There are 2 subtracks derived from CDC-7600. The latest cray/mpp is a massively parallel system with distributed shared memory.

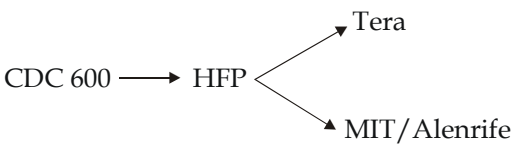
(b) SIMD track



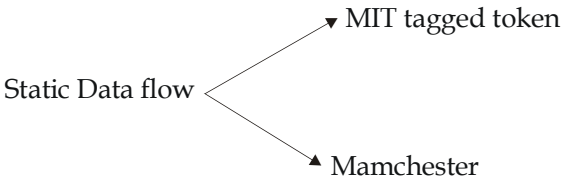
3. Multi threaded and Dataflow tracks:

In case of multi threaded system, each processor can execute multiple context at the same time. So multiple threading means there are multiple threads of control in each processor. So multi threading hides long latency in constructing large scale multiprocessors. This track has been tried out in laboratories.

Multi threaded track



Data Flow Track

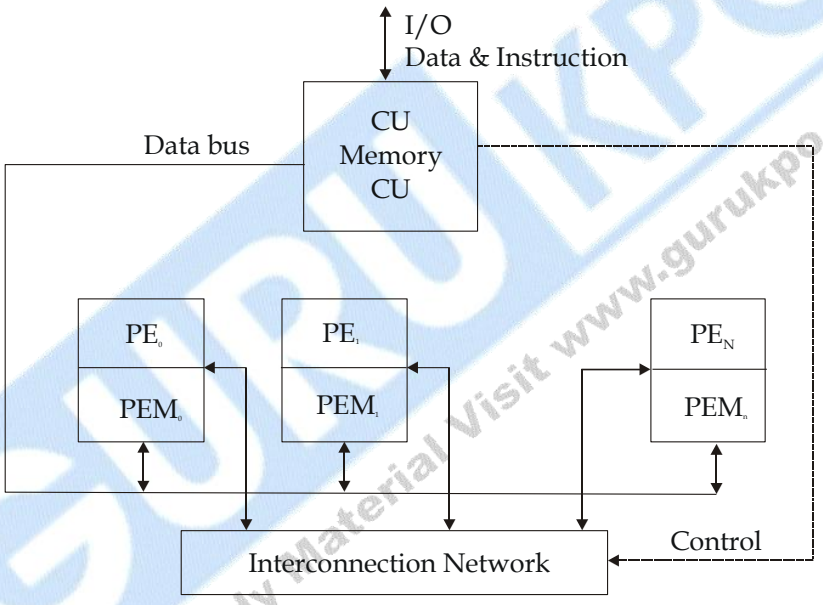


Q.12. What are the two configurations of SIMD array processor.

Ans. Synchronous array of parallel processors is called array processor, which made up of multiple processing element (PES).

SIMD array processor have 2 arrangement

arrangement **I**

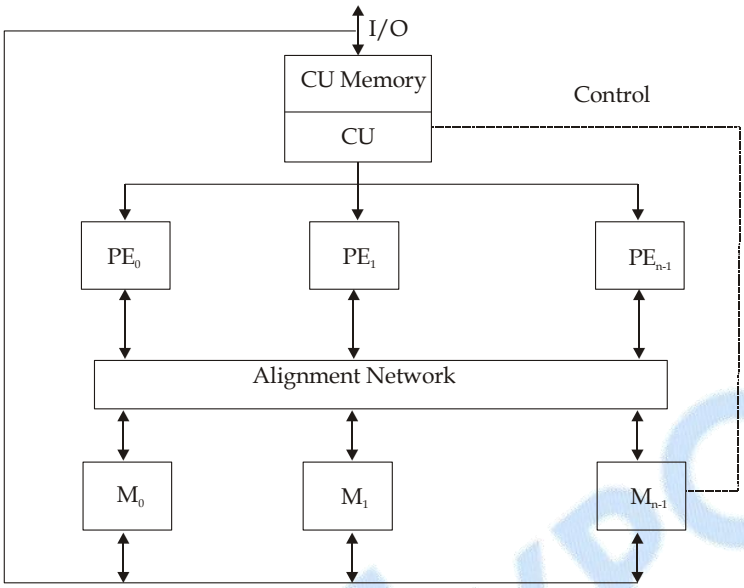


arrangement I (Illiac IV)

First – SIMD array configuration which are introduced in Illiac – IV computer. This is having N synchronized PEs, all are under the control of one CU. Each PE is an arithmetic logic unit (ALU) with attached working register and local memory PEM for storage.

Control unit has its own memory for storage of programs. First user programs are loaded into CU memory and then CU decode all the instructions and find out where the decade instructions should be executed. Scalar and control instructions are executed inside CU and vector instructions are broadcast to the PE for the distributed execution.

arrangement II



arrangement II (BSP)

Main differences in arrangement I and II is in 2 aspects. First the local memories are attached to the PEs are replaced by parallel memory module shared by all the PEs through an alignment network. Second, inter PE network is replace by the inter PE memory alignment network, which is controlled by CU.

Example of configuration II is Burrough Scientific processor (BSP). There are N PEs and P memory modules in configuration II. These two numbers (N and P) are not equal and are relatively prime. The alignment network is a path switching network between PEs and parallel memories.

ppp

Chapter 2
Program Partitioning or Scheduling

Q.1. What are program flow mechanisms?

Ans. Traditional computers are founded on control flow mechanism by which the order of program execution is explicitly stated in the user program. Data flow computers have high degree of parallelism at the fine grain instruction level reduction computers are based on demand driven method which commence operation based on the demand for its result by other computations.

Data flow & control flow computers : There are mainly two sort of computers. Data flow computers are connectional computer based on Von Neumamm machine. It carry out instructions under program flow control whereas control flow computer, executes instructions under availability of data.

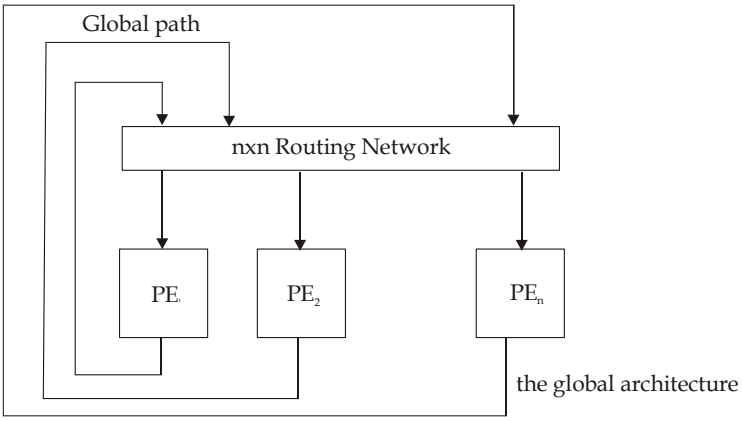
Control flow Computers : Control Flow computers employ shared memory to hold program instructions and data objects. Variables in shared memory are updated by many instructions. The execution of one instruction may produce side effects on other instructions since memory is shared. In many cases, the side effects prevent parallel processing from taking place. In fact, a uniprocessor computer is inherently sequential due to use of control driven mechanism.

Data Flow Computers : In data flow computer, the running of an instruction is determined by data availability instead of being guided by program counter. In theory any instruction should be ready for execution whenever operands become available. The instructions in data driven program are not ordered in any way. Instead of being stored in shared memory, data are directly held inside instructions. Computational results are passed directly between instructions. The data generated by instruction will be duplicated into many copies and forwarded directly to all needy instructions.

This data driven scheme requires no shared memory, no program counter and no control sequencer. However it requires special method to detect data availability, to match data tokens with needy instructions and to enable the chain reaction of asynchronous instructions execution.

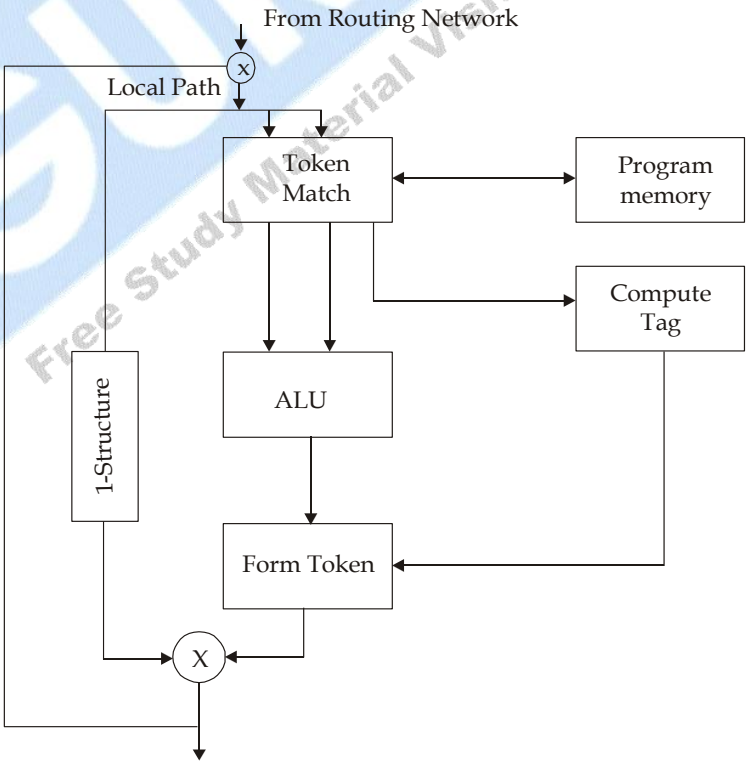
Q.2. Explain data flow architecture?

Ans. There are more than a few new data flow computer projects. Arvind and his associates at MIT have developed a tagged token architecture for constructing data flow computers.



The global architecture incorporate n processing elements (PEs) inter connected by an n x n routing network. The complete system supports pipelined data flow operations in all n PEs. Inter PE communications are done through the pipelined routing network.

Within each PE, the machine offer a low level token matching mechanism which sends off only those instructions whose input data are already available. Each datum is tagged with the address of instruction to which it belongs and context in which the instruction is being executed. Instructions are stored in program memory. Tagged tokens enter the PE through a local path. The tokens can also be passed to the other PE through the routing network. All internal circulation operations are pipelined without blocking.



Interior Design of a Processing Element

You can imagine instruction address in a dataflow computer as replace the program counter & the context identifier replacing the frame base register in control flow computer. It is the machine job to match up data with same tag to needy instructions. In so doing, new data will be produced with a new tag indicating the successor instructions. Thus each instruction represents a synchronization operation. New tokens are formed and circulated along the PE pipeline for sense or to other PEs through global path, which is also pipelined.

Q.3. Explain Grain Sizes and Latency.

Ans. Grain Size or granularity is the amount of computation and manipulation involved in a software process. The simplest way is to count the number of instructions in a given (program segment). Grain size decides the basic program segment chosen for parallel processing. Grain sizes are usually explained as fine, medium or coarse, depending on the processing levels involved.

Latency is a time of the communication overhead acquire amid subsystems for example the memory latency is the tune required by processor to access the memory. The time required for two processes to synchronize with each other is called synchronization latency; computational granularity and communication latency are closely related.

Q.4. How can we partition a program into parallel branches, program modules, microtasks or grains to yield the shortest possible execution time?

Ans. There exists a tradeoff among parallelism and scheduling overheads. The time complexity entail both computation and communication overheads. The program partitioning entail the algorithm designer, programmer, compiler, operating system support etc.

The concept of grain packing is to apply five grain first in order to achieve a higher degree of parallelism. Then one combines multiple fine grain nodes into a coarse grain node if it can remove redundant communications delays or lessen the overall scheduling overhead.

Usually, all five grain operations within a single coarse, grain node are given to some processor for execution. Fine grain partition of a program often demands more inter processor communication than that required in a coarse grain partition. Thus grain pickings' offers a tradeoff between parallelism and scheduling. Internal delays amid fine grain operations within the same coarse grain node are negligible because the communication delay is given chiefly by inter processor delays rather than by delays within the same processor. The selection of optimal grain size is meant to get the shortest schedule for the nodes on a parallel system.

ppp

Chapter 3
System Interconnect Architecture

Q.1. Explain different network properties?

Ans. The topology of an interconnection network can be either static or dynamic. Static networks are created point-to-point direct connections which will not alter during execution. Dynamic networks are applied with switched channels, which are dynamically configured to match the communication demand in user programs.

Static networks are used for fixed connections amid sub systems of a centralized system or multiple computing nodes of a distributed system. Dynamic networks consist of buses, crossbar switches, multistage networks, which are often used in shared memory multi processors. Both types of network have also been employ for inter PE data routing in SIMD computers.

In general, a network is characterized by graph of finite number of nodes linked by directed or undirected edges. The number of nodes in the graph is called the network size.

Node Degree and Network Diameter : The number of edges incident on a node is called the node degree d. In the case of unidirectional channels, the number of channels into a node is the 'in; degree and that out of a node is the 'out' degree. Then the node degree is the total of the two. The node degree reveals the number of I/O ports required per node and their cost of a node. Hence, the node degree should be kept a constant, as small as possible in order to reduce cost. A constant node degree is very much preferred to get modularity in building blocks for scalable systems.

The diameter D of a network is the maximum shortest path amid any two nodes. The path length is measured by the number of links visited. The network diameter show the maximum number of distinct hops amid any two nodes, thus giving a figure of communication pros for the network. thus, the network diameter should be as small as doable from communication point of view.

Q.2. What is Bisection Width?

Ans. When a specified network is cut into two identical halves, the minimum number of edges along the cut is termed as channel bisection width b. In the case of communication network, each edge match up to a channel with w bit wires. Then the wire bisection width is B = bw. This parameter B reflects the wiring density of a network. When B is fixed, the channel width w = B/b. Thus the bisection width offer a fine estimate of maximum communication

band width along the bisect ion of a network. Rest cross sections should be bounded by bisection width.

Q.3. What is Data routing functions? Describe some data routing functions?

Ans. Data routing networks is used for inter PE data exchange. Data routing network can be static or dynamic. In multicomputer network data routing is achieved by message among multiple computer nodes. Routing network reduces the time required for data exchange and thus system performance is enhanced. Commonly used data routing functions are shifting, rotation, permutations, broadcast, multicast, personalized communication, shuffle etc.

Some Data routing functions are described below:

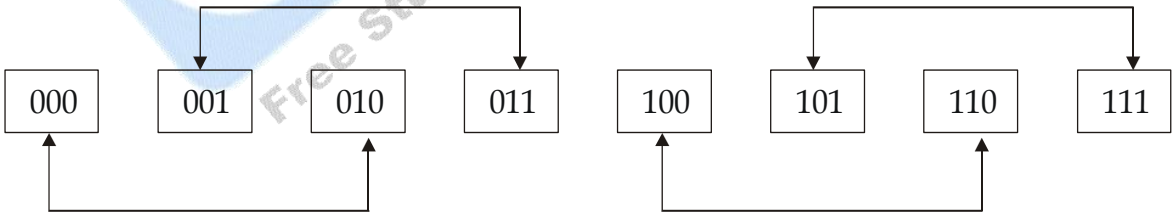
(a) Permutations: Let there are n objects, and then there are nf permutations by which n objects can be recorded. Set of all permutations form a permutation group with respect to composition operation. Generally cycle notation is used to specify permutation function. Cross can be used to implement the permutation. Multi stage network can implement some of the permutations in one or multiple passes through the network. Shifting and broadcast operation are also used to implement permutation operation. Permutation capability of a network is used to indicate the data routing capacity. Permutation speed dominates the performance of data routing network, when n is large.

(b) Hypercube routing function: Three dimensional cube is shown below:

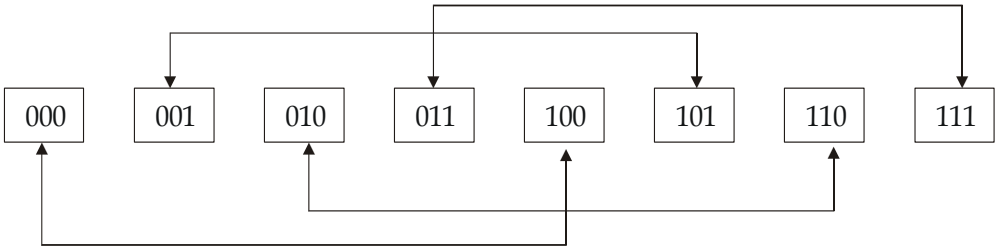
Routing functions are defined by three bits in the node address. Bit order is $C_2C_1C_o$. Data can be exchanged among adjacent nodes which differs in the least significant bit C_o as shown below.

Routing by least significant bit, Co

Similarly routing pattern by using bit C_1 & C_2 is shown below:



Routing by middle bit, C_1



Routing by most significant bit, C_2

common pattern informs that n-dimensional, cube has n-routing functions, which are defined by each bit of the n-bit address. These data routing task are used in routing messages in a hypercube multi workstation.

(c) Broad cast & Multicast: Broad cast is one to all mapping. This is achieved by SIMD computers using a broadcast bus extending from array controller to all PEs. A mechanism is used to broadcast a message in message passing multi computer. Multicast means mapping from one subset to another. There is a variation of broadcast called personalized broadcast. Personalized broadcast sends messages to only selected receivers. Broadcast is a global operation in multi computer. Personalized broadcast may have to be implemented with matching of destination codes in the network.

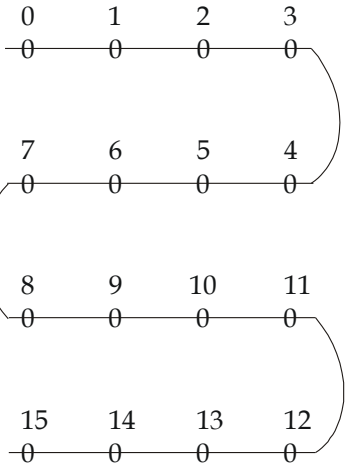
Q.4. What are static interconnection networks?

Ans. Static interconnection networks have many topologies. These topologies are classified according to the dimensions required for layout. Example– one dimension, 2 dimensional, 3- dimensional. One dimensional incorporated linear array which is used for a number of pipelined architecture 2-dimensional includes topology: ring, star, mesh and systolic array. 3 dimensional embrace – completely connected chordal ring, 3-cube and 3- cube connected cycle network.

One dimensional topology

Linear Array: In this N-nodes are connected by N-1 links in the line.

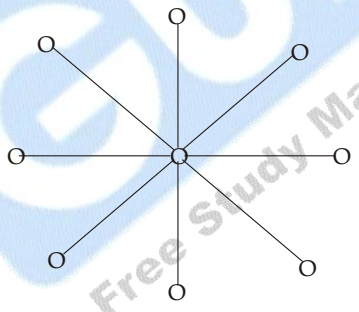
In linear array, each internal node has degree equal to 2. Each external node or terminal nodes have degree equal to 1. Diameter is N -1, which is long for large value of N. The bisection width is b = 1. Linear arrays are actually simplest connection topology. arrangement of linear assays is not symmetric. So when N is large, then communication inefficiency is there.



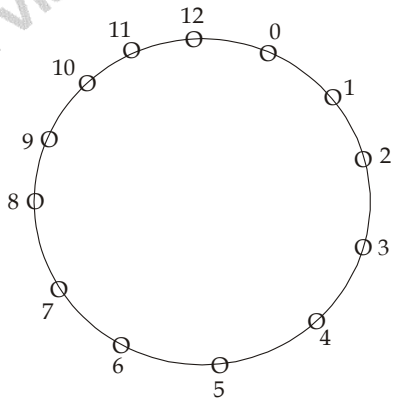
For small N, say N = 2, it is economic to implement a linear array. As diameter increases linearly with respect to N, it should not be used for large N. Linear array is different from bus which is time shared through switching among many nodes attached to it. Concurrent use of different sections of the structure of different source and destination pairs is permitted in linear arrays.

Two Dimensional topology

Star: Star is a two level tree with a high node degree of α = N-1 and a small constant diameter of 2. Star topology is used in systems with a centralized supervisor node.

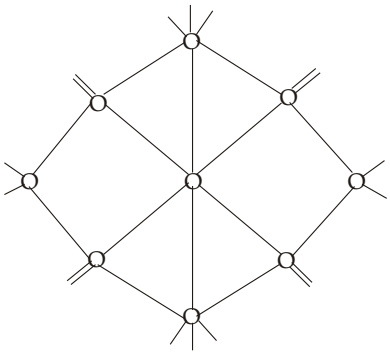


Star topology



Ring topology

Systolic array: For implementing fixed algorithm this type of pipelined array architecture is used. Figure of systolic array topology is shown:

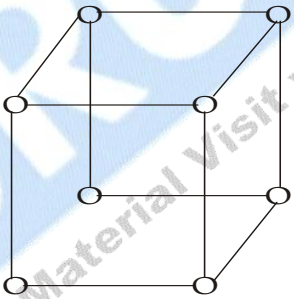


It is designed for matrix multiplication. Degree of interior nodes are equal to 6. Systolic array are pipelined which multi dimensional flow of data streams. Systolic array matches the communication structure of the algorithm. It is similar to the fixed inter connection and synchronous ratio over special applications like signal/image processing. It is difficult to program and thus having limited applications.

Three Dimensional Topology

3- Cube

A 3- cube having B-nodes is shown below A



3- Cube

A 4- cube is made by interconnecting the corresponding nodes of two 3-cubes. Node degree of n-cube is equal to n and so does the network diameter. Nodes degree increases linearly with respect to the dimensions, thus making hypercube difficult to use as a scalable architecture.

Cube-Connected Cycles

Improved architecture of hypercube is the cube connected cycles. 3- Cubes are customized to form 3-cube connected cycles (CCC).

Thus, K-cube connected cycle can be made from the L-cube with $n = 2^x$ cycles nodes. Each vertex of K-dimensional hyper cube is replaced by a ring of K-nodes thus a k- cube is translated into a K-CCC with $K \times 2^K$ nodes.

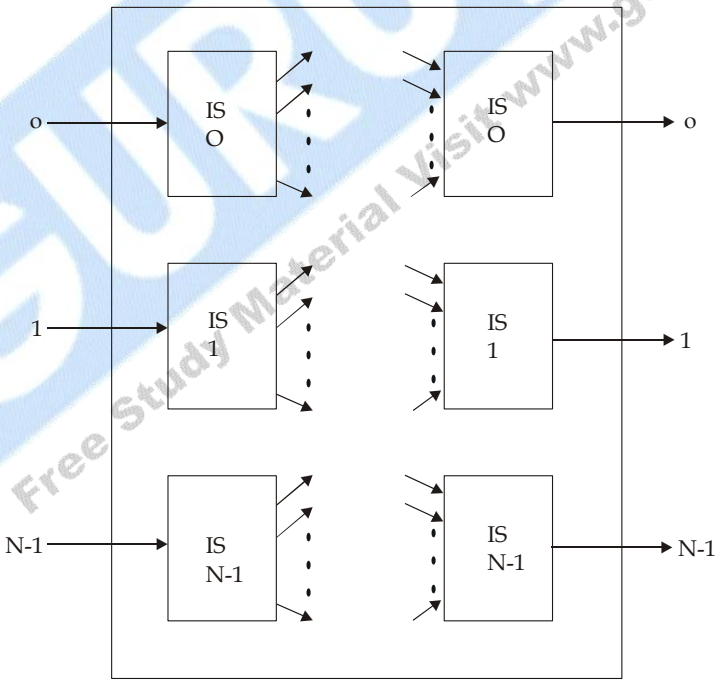
Q.5. Discuss various Dynamic Connection Network.

Ans. For multipurpose and general purpose application we always use dynamic connections. Dynamic connection implements all common wrication patterns based on program demands. Fixed connections with switches on arbiters are used along the connecting path to provide the dynamic connectivity. Basically there are 2 classes of dynamic interconnection network-single stage and multistage network.

Single Stage Network: Single stage network is a switching network with N-input selectors (Is) and N output selectors (Os). Each input selector is 1- to –D demultiplexer and each output selector is an m – to -1 multiplexer where 1 = D = N and 1 = m = N. Single stage network is called recirculating network. Data items are recirculate through the single stage determines the number of recirculations required. Crossbar switching network is a single stage network with D = M = N. For establishing the desired path different control signals are applied to all input selectors and output selectors.

Multistage Network: Many stages of interconnected switchers forms a multistage MIMD network. Multistage network are characterized by 3 properties

(a) Switch box



(b) Network topology

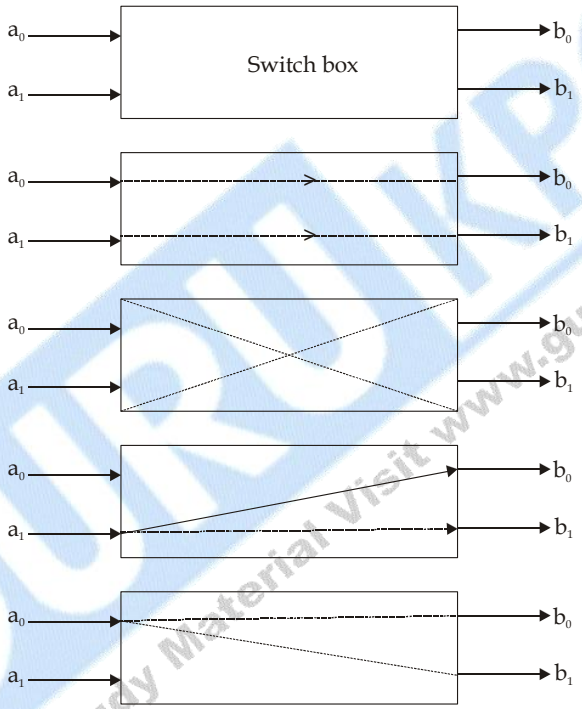
(c) Control structure

Multistage network uses many switch boxes. Each switch is an interchange device with 2 inputs & 2-outputs. There are 4- stage of switch box straight,

exchange, upper broadcast and lower broadcast. A two function switch box can be either in switch can be in any of four legitimate states. Switching box and their inter connection stages are given on subsequent page.

A multistage network connects an arbitrary input terminal to an arbitrary output terminal. There are two kind of multi stage network: one sided or two sided. One sided network is called fill switches and they include input and output ports on the same size. Two-sided multistage network have an input side and output side divided into classes:

Blocking , rearrange able and blocking.



A two by two switching box and its four interconnection states

ppp

Chapter 4
Processors and Memory Hierarchy

Q.1. What is difference between RISC and CISC ?

Ans.

Properties	CISC	RISC
1. Number of instruction used in set architecture	It differs from 120-350	It is less than 100
2. Instruction/data format used	Variable instruction and data format is used.	Fixed format instruction/ data is used.
3. Number of addressing modes	differ from 12-24	differ from 3 to 5
4. Number of general purpose registers used	Vary from 8 to 24	Vary from 32-192
5. Number of memory reference instruction used	Large number of memory reference instructions.	Less number of memory reference instruction are used. Only load and store are memory reference instruction.
6. Number of memory reference instruction used	Large number of memory reference instructions.	Less number of memory reference instruction are used. Only load and store are memory instructions.
7. High level language instructions implementation	Directly employed in hardware	Not directly employed in hardware.
8. Execution efficiency	Execution competence increased.	Execution competence is not increased.
9. Control logic used	Micro programmed control unit is used.	Hardwired control unit is used.
10. Use of control memory	Control memory is employed.	No use of control memory.
11. Cache memory	Unified cache memory is employed.	Splited cache is employed.
12. Clock rate	35-50MHz	50-150 MHz

Q.2. What is Super Scalar Processors?

Ans. In a super scalar processor, multiple instructions are employed, this means that multiple instructions are issued per cycle and multiple results are created per cycle.

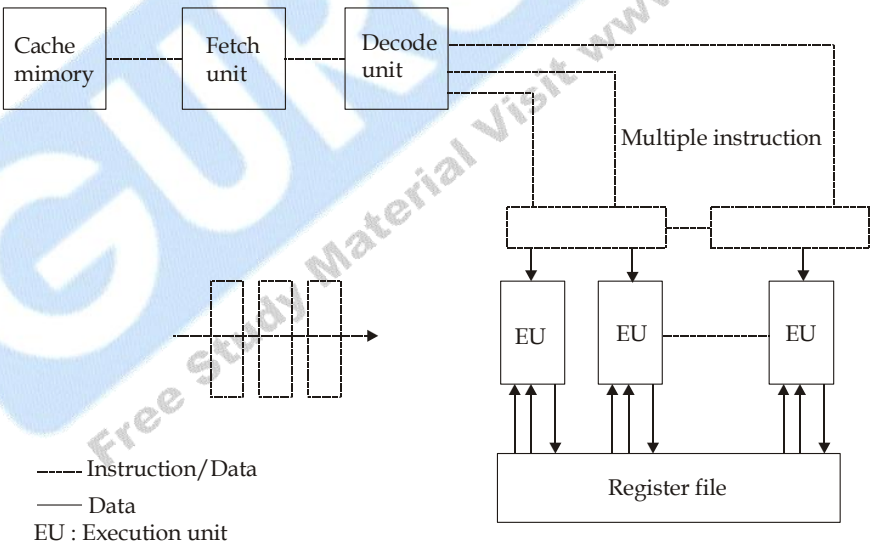
In simple scalar processor one instruction executes per cycle. Only one instruction is employed per cycle and only one completion of instruction is probable per cycle.

Super Scalar process are intended to utilize more instruction level parallelism. Super scalar operate basically in parallel.

Super Scalar Architecture

It involves highly multipored register files. Their input parts are required for each EU.

Super Scalar processors acknowledge a usual sequential stream of instructions but can generate more than are instructions to the EUs in each cycle. Super scalar processors do not presume dependency free code. They cope with dependencies themselves using hardware. Super scalar processors with the same degree of parallel execution are considerable more multifaceted.

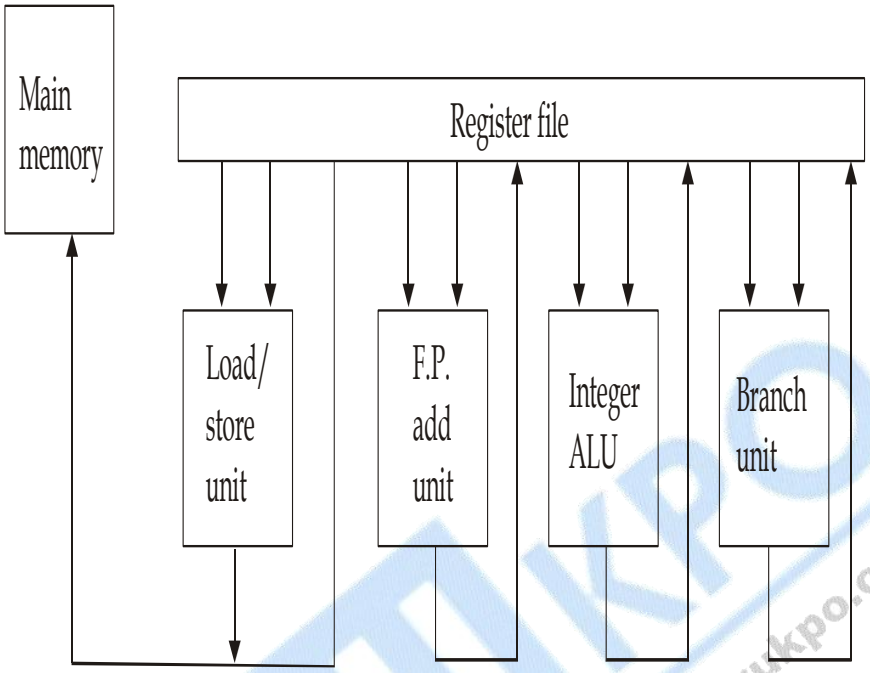


Q.3. What is VLIW architecture?

Ans. The VLIW architecture is generalized. It includes well-known concepts:

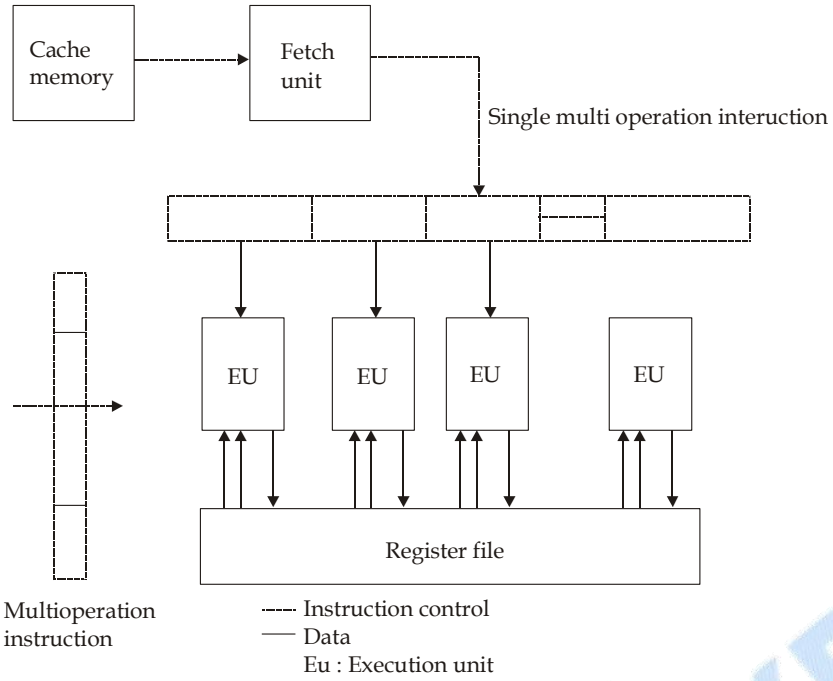
1. Horizontal Microcoding
2. Super scalar processing

A typical VLIW architecture machine has instruction words of hundreds of bits in length VLIW stands for very long instructions word.



VLIW processor

VLIW processor expect dependency free code i.e. multi operation code. VLIW processors are statically programmed. VLIW notion is taken from horizontal micro coding. Different fields of the long instruction word carry the opcodes to be send off to different functional units.



Q.4. Explain Symbolic Processors?

Ans. Symbolic processing applied in numerous cases including theorem proving, pattern recognition, expert systems, text retrieval, cognitive science and machine intelligence, knowledge engineering. In three applications, data and knowledge representation, primitive operations, I/O and special architectural features are different them in numeral computing symbolic processors are named 'prolog processors' or 'symbolic manipulators'.

Characteristics of Symbolic Processing

Attributes	Characteristics
1. Knowledge	Lists, relational databases, scripts, semantic nets, frames, production system.
2. Common operation	Search, sort, pattern matching, filtering, unification, text retrieval, reasoning
3. Memory Requirements	Large number with intensive access pattern. Addressing is often content based.
4. Communication pattern	Message traffic varies in size and destination granularity & format of message unit change with applications.
5. Properties of Algorithm	Non-deterministic, possibly parallel and distributed computations.
6. Input-Output Requirements	User-guided programs, intelligent-person machine interface, input can be graphical.
7. Architecture features	Parallel update of large knowledge bases, dynamic load balancing, dynamic memory allocation, hardware supported garbage collection.

Q.5. What is Virtual memory? In how many classes virtual memory system is categorized?

Virtual memory is a notion used in some large system, that permits user to make program as through large memory space were present, equal to the totality of auxiliary memory. In memory ladder programs and data are first stored in auxiliary memory. Portion of program and data are then brought into main memory as they are needed by CPU. Each address referenced by CPU goes through an address mapping from virtual address to physical address in memory.

Hence virtual memory forever give an false impression that they have large memory at their disposal, even through computer has relatively small memory.

Virtual memory based system provides a mechanism for translating program generated address into correct main memory locations. This all process is done dynamically, when process are executing in main memory. The translation a mapping is handled by automatically using hardware of mapping table. The address used by programs are called virtual address as such addresses set is called address space. An address in main memory is called physical address set of such address is called memory space.

Virtual Memory System is grouped in 2 classes:-

(1) Those with fixed sized blocks called pages.

(2) Those with variable size block called segments.

Paging: It is a memory management method that allows the physical address space of a method to be non-continuous.

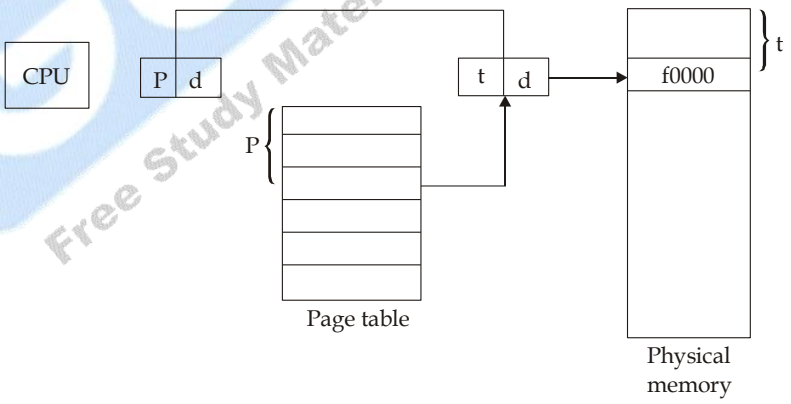


Fig. Paging Hardware

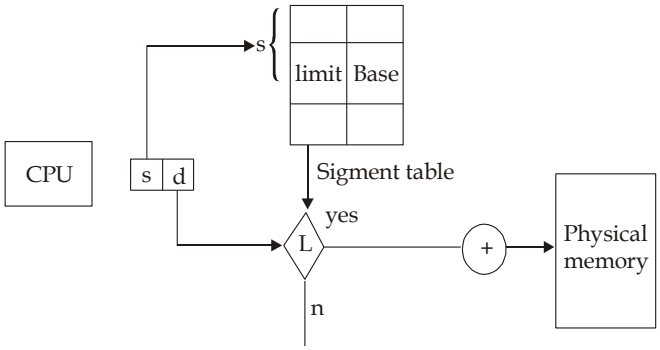
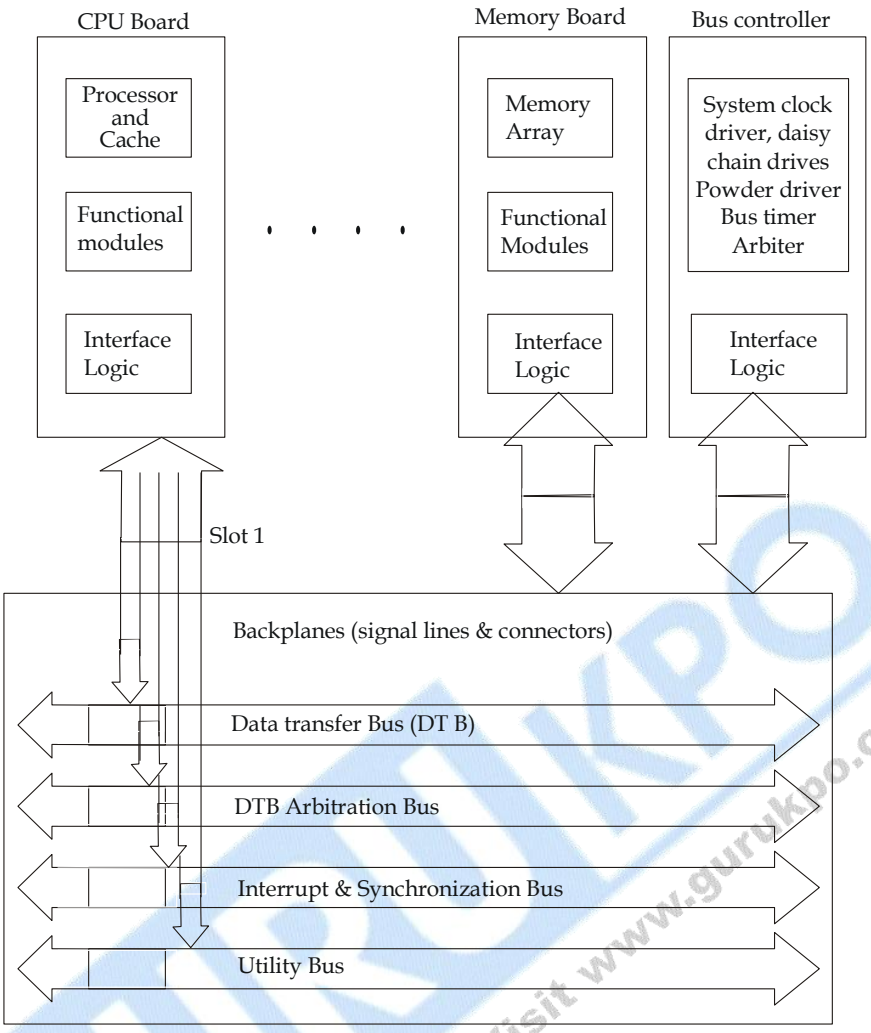


Fig. Segmentation hardware

Q.6. Explain Backplane Bus System?

A backplane bus interconnects processors, data storage and peripheral devices in a tightly coupled hardware arrangement. The system bus must be designed to permit communication amid devices on the bus without disturbing the interval activities of all devices attached to the bus. Timing protocols must be established to arbitrate among multiple requests. Operational rules must be set to guarantee orderly data transfers on the bus. Signal lines on the backplane are often functionally grouped into several buses as shown in the figure. The four groups shown here are very similar to those proposed in the 64 bit VME bus specification.

Various functional boards are plugged into slots on the backplane. Each slot is given with one or more connectors for pop in the boards as shown by the vertical arrows. For example one or two 96-pin connectors are used per slot on the VME backplane.



Backplane buses, system interfaces with slot connections to various functional boards in a multiprocessor system

ppp

Chapter 5
Pipelines Processors

Q.1. What are the characteristics of Pipeline?

- **Ans.**Pipelining refers to the temporal overlapping of processing pipelines. It is more than assembly lines in computing that can be employed for instruction processing. A basic pipeline process a sequence of tasks or instruction, according to the following principle of operation.

  Each task is subdivided into a number of consecutive tasks. The processing of each single instruction can be broken down into four sub tasks:-

  1. Instruction Fetch

  2. Instruction Decode

  3. Execute

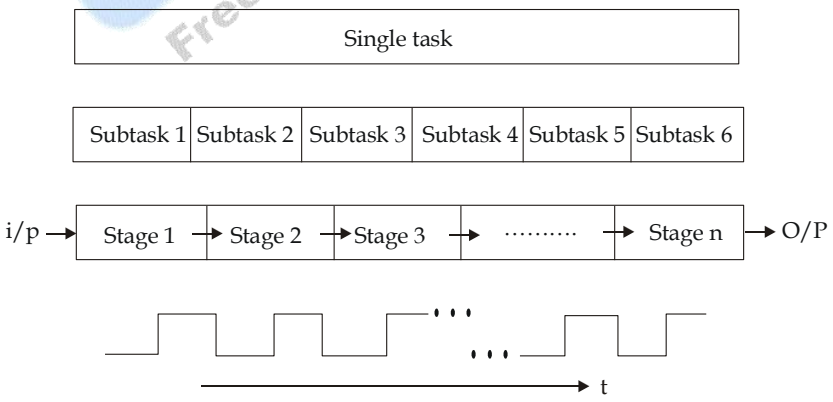
  4. Write back

  It is supposed that there is a pipelined stage associated with each subtask.

  The equal amount of time is available in each stage for performing the required subtask.

  All the pipeline stages work like an assembly line, that is, receiving their input from the previous stage and delivering their output to next stage.

  We also suppose, the basic pipeline operates clocked, in other words synchronously. This means that each stage accepts a non input at start of clock cycle, each stage has a single clock cycle available for performing the required operation and each stage increases the result to the next stage by the beginning of subsequent clock cycle.

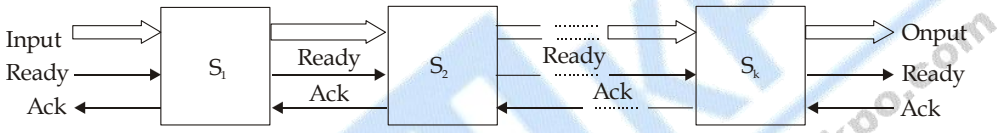


Q.2. Explain Linear Pipeline Processors ?

Ans. A linear Pipeline processor is a flow of processing stages which are linearly connected to perform a fixed function over a stream of data flowing from one end to other. In modern computers, linear pipelines are applied for instruction execution, arithmetic computation, memory access operations.

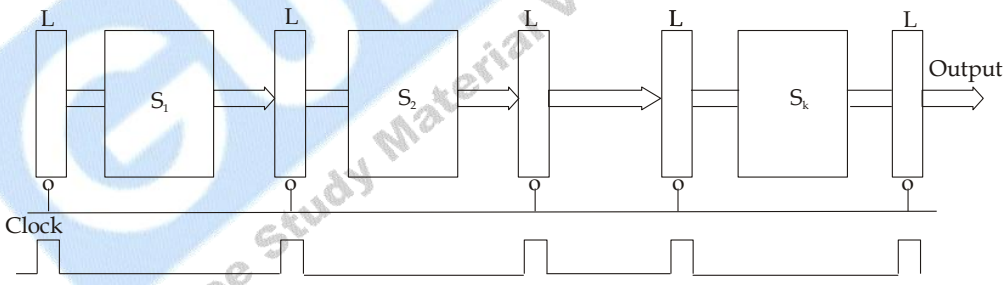
A linear pipeline processor is built with the processing stages. External inputs are inputted into the pipeline at the first stage S_1. The processed results are passed from stage Si to stage Si+1 for all i = 1,2…….K-1. The final result appear from the pipeline at the last stage Sk. Depending on the control of data flow along the pipeline, linear pipelines are formed in two group.

Asynchronous Model: Data flow amid adjacent stages in asynchronous pipeline is controlled by handshaking protocol. When stage S_1 is ready to transmit, it sends a ready signal to Si + 1. After stage Si+1 receives the incoming data, it returns an acknowledge signal to Si.



An Asynchronous pipeline Model

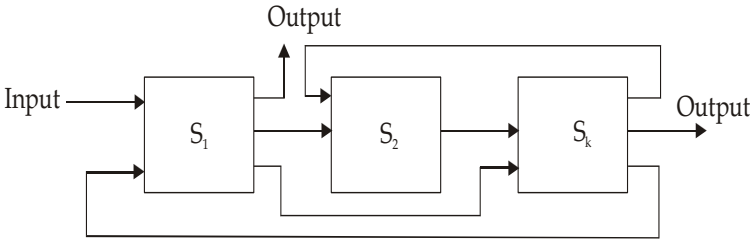
Synchronous Model: Clocked latches are used to interface between stages. The latches are made with master slave flip flops, which can detach inputs from outputs upon the arrival of a clock pulse, all latches transfer data to the next stage simultaneously.



A Synchronous pipeline Model

Q.3. Explain Non linear Pipeline Processors?

Ans. A dynamic pipeline can be reconfigured to carry out variable functions at different times. The traditional linear pipelines are static pipelines because they are used to carry out fixed functions. A dynamic pipeline permit feed forward and feedback connections besides the streamline connections. For this reason, some authors call such a structures as non-linear pipeline.



A three stage pipeline

This pipeline has three stages. Besides the streamline connections from S_1 to S_2 and from S_2 to S_3, there is feed forward connection from S_2 to S_3 and two feedback associations from S_3 to S_2 and from S_3 to S_1.

These feed forward and feedback connections make the scheduling of consecutive event into the pipeline a non trivial task. With these connections, the output of the pipeline is not necessarily from the last stage. In fact, following different dataflow model, one can use the same pipeline to assess different functions.

Q.4. What is Reservation Table in linear pipelining?

Ans. The utilization pattern of successive stages in a synchronous pipeline is mentioned by reservation table. The table is essentially a space time diagram depicting the precedence relationship in using the pipeline stages. For a K-stage linear pipeline, 'K' clock cycles are needed to flow through the pipeline.

Stages	1	2	3	4
S_1	X			
S_2		X		
S_3			X	
S_4				X

Reservation table of 4-Stage

Q.5. What is Reservations table in Non-linear pipelining?

Ans. Reservation table for a dynamic pipeline become more complex and interesting because a non-linear pattern is followed. For a given non-linear pipeline configuration, multiple reservation tables can be generated. Each reservation table will show evaluation of different function.

Each reservation table displays the time space flow of data through the pipeline for one function evaluation. Different function may pursue different paths on the reservation table.

Stages	1	2	3	4	5	6	7	8
S_1	X					X		X
S_2		X		X				
S_3			X		X		X	

Processing sequence

$S_1 \rightarrow S_2 \rightarrow S_1 \rightarrow S_2 \rightarrow S_3 \rightarrow S_1 \rightarrow S_3 \rightarrow S_1$

Reservation table for function 'X'

Q.6. What is Instruction Pipeline Design?

Ans. A stream of instructions can be carry out by pipeline in an overlapped manner. A typical instruction execution consists of a sequence of operations, including

(1) Instruction fetch

(2) Decode

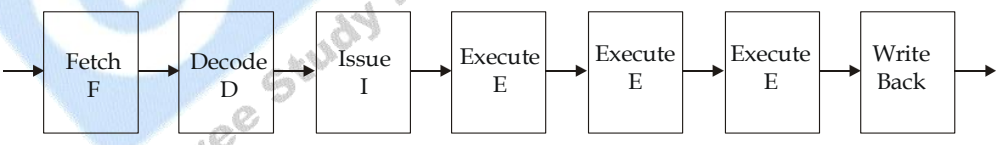
(3) Operand fetch

(4) Execute

(5) Write back phases

Pipeline instruction processing

A typical instruction pipeline has seven stages as depicted below in figures.



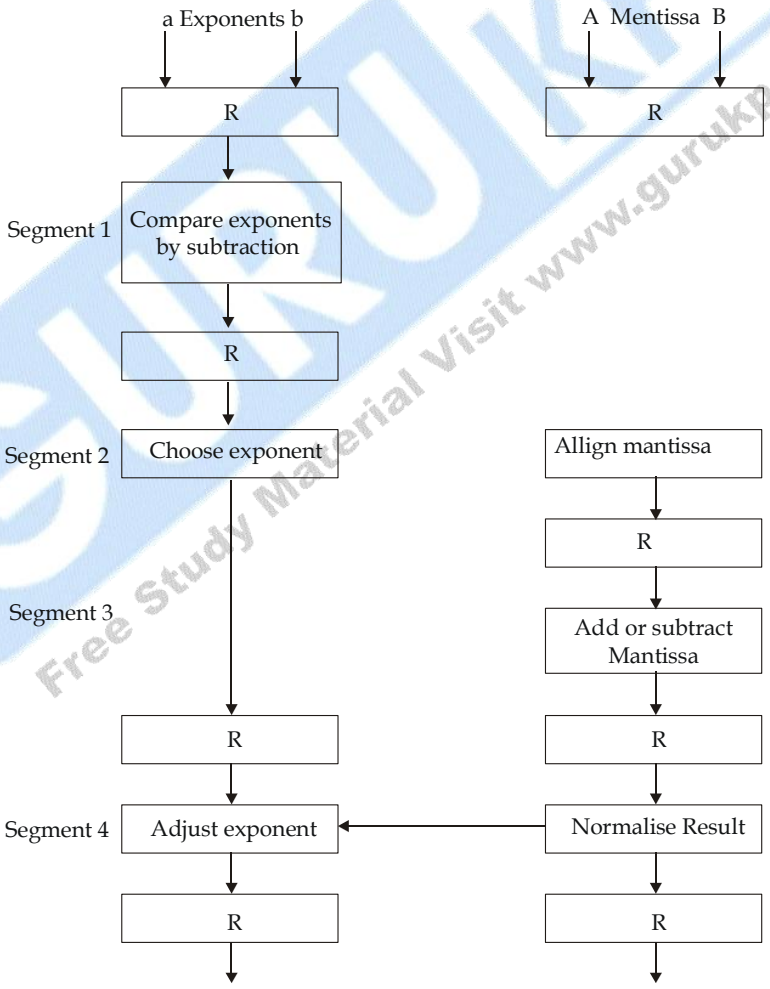
- Fetch stage (F) fetches instructions from a cache memory.
- Decode stage (D) decode the instruction in order to find function to be performed and identifies the resources needed.
- Issue stage (I) reserves resources. Resources include GPRs, bases and functional units.
- The instructions are executed in one or several execute stages (E)
- Write back stage (WB) is used to write results into the registers.
- Memory lead and store (L/S) operations are treated as part of solution.

- Floating point add and multiply operations take four execution clock cycles.
- In many RISC processors fewer cycles are needed.
- Ideal cycles when instruction issues are blocked due to resource conflicts before date Y and Z are located in.
- the store of sum to memory location X must wait three cycles for the add to finish due to flow dependence.

Q.7. Explain Arithmetic Pipeline design?

Pipeline arithmetic units are typically set up in very high speed computers. They are used to apply floating point operation, multiplication of fixed point numbers and similar computations encountered in scientific problems.

- The exponent are compared by subtracting them to determine their difference.



Arithmetic Pipeline for Addition & Subtraction

- Exponent difference determine how many times the mantissa associated with the smaller exponent must be shifted to the right.
- This produces are alignment of two mantissas.
- The teno mantissas are added or subtracted in segment 3.
- Finally result is normalised in segment 4.
- When a overflow occurs, the mantissa of the sum or difference is shifted right and the exponent is incremented by one.
- When an underflow occurs, the number of leading zeroes in the mantissa determines number of left shifts in the mantissa and the number that must be subtracted from the exponent.

ppp

Case Studies

Case Study 1.
Cache Policies.

Consider two alternate caches, each with 4 sectors holding 1 block per sector and one 32-bit word per block. One cache is direct mapped and the other is fully associative with LRU replacement policy. The machine is byte addressed on word boundaries and uses write allocation with write back.

1a) What would the overall miss ratio be for the following address stream on the direct mapped cache? Assume the cache starts out completely invalidated.

read 0x00 **M**
read 0x04 **M**
write 0x08 **M**
read 0x10 **M**
read 0x08 **H**
write 0x00 **M Miss ratio = 5/6 = 0.8333**

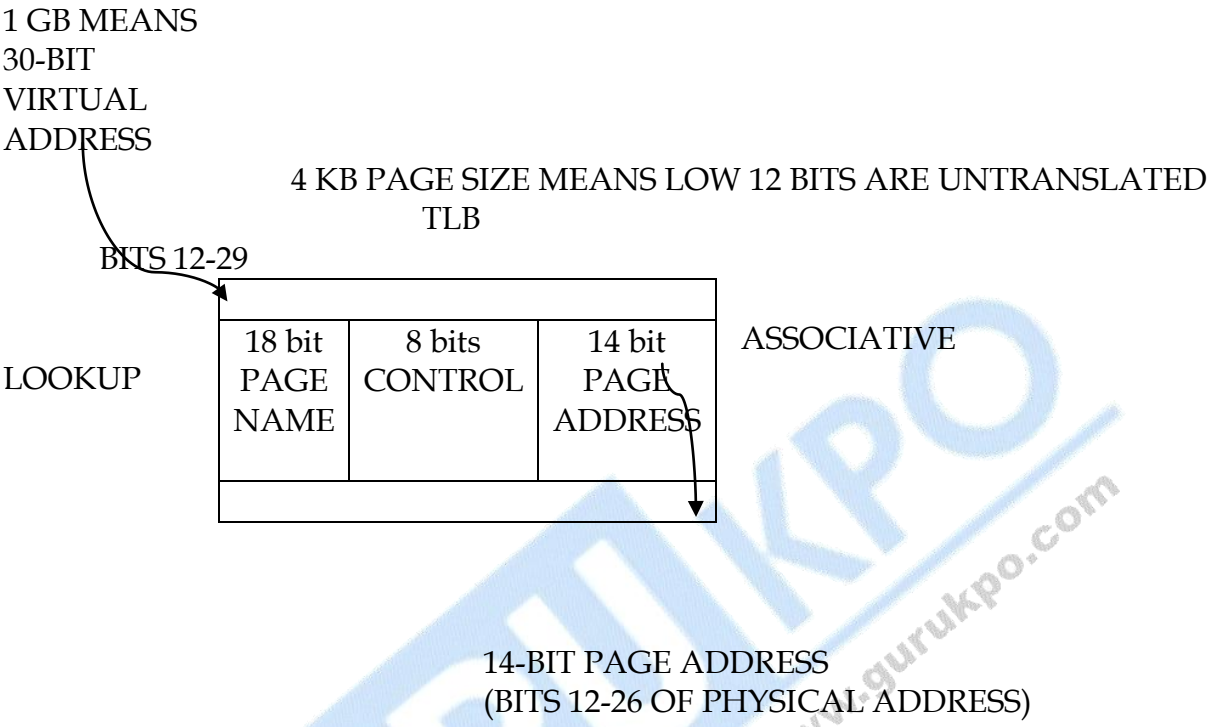
Case Study 2. Virtual Memory and Cache Organization.

The 742LX is a uniprocessor having up to a maximum of 64 MB of addressable physical memory. The cache, virtual memory, and TLB have the following attributes:

Cache	**Virtual**	**Memory TLB**
unified	virtual page size is 4 KB	unified
physically addressed	virtual address space is 1 GB	fully associative
cache holds 20 KB		40 entries
5 way set associative		1 byte control/entry
32 Byte block size		
sector size = block size		
LRU replacement		
write back		
byte addresses on word boundaries		

2a) Sketch a block diagram of how the virtual address is mapped into the physical

address (assuming a TLB hit). Be sure to label exactly which/how many of the address bits go
where. and how many bits are in each of the 3 fields in a TLB entry.



Case Study 3. Multi-Level Caches.

You have a computer with two levels of cache memory and the following specifications:
CPU Clock: 200 MHz Bus speed: 50 MHz
Processor: 32-bit RISC scalar CPU, single data address maximum per instruction
L1 cache on-chip, 1 CPU cycle access
block size = 32 bytes, 1 block/sector, split I & D cache
each single-ported with one block available for access, non-blocking
L2 cache off-chip, 3 CPU cycles transport time (L1 miss penalty)
block size = 32 bytes, 1 block/sector, unified single-ported cache, blocking, non-pipelined
Main memory has 12+4+4+4 CPU cycles transport time for 32 bytes (L2 miss penalty)
Below are the results of a dinero simulation for the L1 cache:
CMDLINE: dinero -b32 -i8K -d8K -a1 -ww -An -W8 -B8
CACHE (bytes): blocksize=32, sub-blocksize=0, wordsize=8, Usize=0,
Dsize=8192, Isize=8192, bus-width=8.
POLICIES: assoc=1-way, replacement=l, fetch=d(1,0), write=w, allocate=n.
CTRL: debug=0, output=0, skipcount=0, maxcount=10000000, Q=0.
Metrics Access Type:

(totals,fraction)	Total	Instrn	Data	Read	Write	Misc
Demand Fetches	10000000	7362210	2637790	1870945	766845	0
	1.0000	0.7362		0.2638	0.1871	0.0767	0.0000
Demand Misses	52206	8466		43740	36764	6976	0
0.0052	0.0011	0.0166	0.0196	0.0091	0.0000		

Words From Memory 180920
(/ Demand Fetches) 0.0181
Words Copied-Back 766845
(/ Demand Writes) 1.0000
Total Traffic (words) 947765
(/ Demand Fetches) 0.0948

3a) What is the *available* (as opposed to used) sustained bandwidth between:
- L1 cache bandwidth available to CPU (assuming 0% L1 misses)?
200 MHz * 2 caches * 32 bytes / 1 clock = 12.8 * 109 B/sec = 11.92 GB/sec
- L2 cache bandwidth available to L1 cache (assuming 0% L2 misses)?
200 MHz * 1 cache * 32 bytes / 3 clocks = 2.133 * 109 B/sec = 1.98 GB/sec
- Main memory bandwidth available to L2 cache?
200 MHz * 32 bytes / (12+4+4+4) clocks = 267 * 106 B/sec = 254 MB/sec

3b) How long does an *average* instruction take to execute (in ns), assuming 1 clock cycle per instruction in the absence of memory hierarchy stalls, no write buffering at the L1 cache
level, and 0% L2 miss rate.
7362210 instructions = 7362210 clock cycles @ 1 clock effective access time
52206 demand misses @ 3 clocks = 156618 clocks delay penalty.
(7362210 + 156618) / 7362210 = 1.0213 clocks / 200 Mhz = 5.1065 ns
3c) A design study is performed to examine replacing the L2 cache with a victim cache.
Compute a measure of speed for each alternative and indicate which is the faster solution. Assume
the performance statistics are
L2 cache local miss ratio = 0.19
Victim cache miss ratio = 0.26; and its transport time from L1 miss = 1 clock
Given fixed L1 cache performance, it is fair to compare these head-to-head (but the comparison
might not stay the same if L1 were changed):
tea for L2 cache beyond the L1 access time is:
3 + 0.19 * (12+4+4+4) = 7.56 clocks in addition to L1 delay
tea for L2 cache beyond the L1 access time is:
1 + 0.26 * (12+4+4+4) = 7.24 clocks in addition to L1 delay
So, in this (contrived) case the victim cache is a slight win in speed, and a whole lot cheaper.

Case Study 4.

Discuss about the advantage(s) and the disadvantages of the von Nuemann concept.

Solution:

The von Neumann concept is a computer design model that uses a single storage model to hold both instructions and data.

Advantages:

- Reprogramming was made easier
- Programs are allowed to modify themselves
- Programs can write Programs
- General flexibility

Disadvantages:

- Malfunctioning programs can damage other programs or the operating system
- von Neumann bottleneck - CPU must wait for Data to transfer to and from memory

Case Study 5.

Define term "delayed branch", its application, and its shortcomings.

Solution:

Delayed branch is technique for reducing the effects of control dependencies by delaying the point where a branch operation effects the program counter. This allows one or more instructions following the branch operation to execute whether or not the branch operation succeeds.

Advantage:

- Allows for pipeline CPUs to reduce the clock cycles wasted due to pipeline flushing during a branch or a jump operation

Disadvantage:

- If the compiler cannot put instructions to execute after the branch due to dependencies, then it must insert no-op instructions which increases the size of program

Case Study 6.

CPU time (T) is defined as:

$T = I_c * CPI * \tau$

I_c stands for the instruction count,

CPI stands for average clock cycles per instruction, and

τ stands for the clock cycle time.

A RISC computer, *ideally*, should be able to execute one instruction per clock cycles. Within the scope of a RISC architecture, name and discuss (briefly) ***distinct*** issues that do not allow ideal performance.

Solution:

Issues:

- Memory Access: Any access to the memory can take longer than one instruction
- Branching: Program branches will flush instructions in a pipeline and cause it to take longer then one instruction

Case Study 7. Loop fusion allows two or more loops that are executed the same number of times and that use the same indices to be combined into one loop:

1. Within the scope of a RISC processor, why does it (**Loop fusion**) improve performance (detail explanation)?

Solution:

In the scope of a RISC processor, Loop fusion can improve performance by decreasing the need for extraneous loop control instructions. In the absence of extraneous loop control instructions, the processor can run a program faster.

Case Study 8s. Interleave memory

1. Define interleaved memory (be as clear as possible);

Solution:

Interleaved memory describes a way to virtually access memory into a number of memory banks.

2. Within the scope of interleaved memory, define mapping of the logical addresses to the physical addresses. Distinguish them from each other.

Solution:

In interleaved memory, the memory is divided into *N* banks of memory where virtual address, *i*, would actually reside in memory bank *i/N* (ignoring the remainder), logically addressed by *i mod N*.

3. What is the main difference between an interleaved memory and a parallel memory?

Solution:

Interleaved memory requires 2 to N memory banks to look up multiple contiguous virtual memory locations where parallel memory only requires 1 memory bank.

MCQ's

Set-A

1. RISC stands for:

   (a) Register Instruction Set Computer

   (b) Reduced Instruction Set Computer

   (c) Reduced Instruction Set Clock

   (d) None of the above ( )

2. CISC processor have.....length instruction format.

   (a) Variable

   (b) Fixed

   (c) Can not say

   (d) None of the above ( )

3. CISC stands for:

   (a) Clock Instruction Set Computer

   (b) Control Instruction Set Computer

   (c) Complex Instruction Set Computer

   (d) None of the above ( )

4. .....is a term used to denote a large class of techniques that are used to provide simultaneous data processing tasks

   (a) Shared memory

   (b) Parallel Processing

   (c) Memory hierarchy

   (d) None of the above ( )

5. .....is a technique of decomposing a sequential process into sub operations.

(a) Pipelining (b) Parallel Processing

(c) Vector Processing (d) None of the above ( )

6. Personal computer were appeared in:

(a) Ist generation

(b) 2nd generation

(c) 4th generation

(d) 5th generation ( )

7. A.....contains the address of the next instructions to be executed.

(a) Data Register

(b) Accumulator

(c) Instruction Register

(d) Program Counter ( )

8. A.....is an interconnected set of processing elements which cooperate by communicating with one another to solve large problem

(a) Parallel Computer

(b) Personal Computer

(c) Laptop Computer

(d) None of the above ( )

9. Many operating system are designed to enable the CPU to process a number of independent program concurrently. This concept is called:

(a) Cache Memory

(b) Multiprogramming

(c) Multiprocessor

(d) None of the above ( )

10. A.....system is an interconnection of two more CPU with memory and I/O equipment.

(a) Processor (b) Synchronization

(c) Multiprocessor (d) None of the above ( )

11. MIMD stands for:

(a) More Instruction Stream, Multiple data Stream

(b) Multiple Instruction Stream, Multiple Data Stream

(c) Many Instruction Stream, Many Data Stream

(d) None of the above ( )

12. The components that form a multiprocessor system are:

(a) CPUs (b) IOPs

(c) Memory Unit (d) All of the above ( )

13. Computers are interconnected with each other by means of communication lines to form a:

(a) Computer Network

(b) Multiprocessor

(c) Data Dependency

(d) None of the above ( )

14. A multiprocessor system with common shared memory is called:

(a) Loosely coupled system

(b) Tightly coupled system

(c) Both a and b

(d) None of the above ( )

15. Loosely coupled system are more efficient when the interaction between task is:

(a) Maximum (b) Minimum

(c) Can not say (d) None of the above ( )

16. In a .....has it own private local memory

(a) Crossbar switch

(b) Tightly coupled system

(c) Loosely coupled system

(d) None of the above ( )

17. The memory connected to the common system bus is.....by all processors.

(a) Shared (b) Partitioned

(c) Distributed (d) None of the above ( )

18. The .....organization consists of number of cross points that are placed at intersection between buses and memory module paths

(a) Multiport memory (b) Crossbar switch

(c) Multistage switch (d) None of the above ( )

19. A bus that connects components in a multiprocessor system, is called:

(a) Control bus

(b) Data bus

(c) Address bus

(d) System bus ( )

20. A typical system bus consists of approximately.....signals lines

(a) 100 (b) 2

(c) 3 (d) None of the above ( )

21. The signal lines in system bus are divided into.....functional groups.

(a) 1 (b) 2

(c) 3 (d) None of the above ( )

22. The purpose of parallel processing is to:

(a) Speed up the processing

(b) Increase memory

(c) Decrease memory

(d) None of the above ( )

23. M.J. Flynn's parallel processing classification is based on:

(a) Multiple Instructions

(b) Multiple data

(c) Both (a) and (b)

(d) None of the above ( )

24. .....represents an organization that includes many processing units under the supervision of a common control unit.

(a) SISD (b) SIMD

(c) MIMD (d) None of the above ( )

25. A.....can be be visualized as a collection of processing segments through which binary information flows:

(a) Memory (b) I/O devices

(c) Processor (d) Pipeline ( )

26. The pipeline used for floating point operations is called:

(a) Arithmetic pipeline (b) Instruction pipeline

(c) Both (a) and (b) (d) None of the above ( )

27. The finest level of pipelining is called:

(a) Micro pipelining

(b) Macro pipelining

(c) Linear pipelining

(d) None of the above ( )

28. VLIW stands for:

(a) Very Long Instruction Word

(b) Very Long Instruction Word

(c) Very Large Information Word

(d) None of the above ( )

29. MIPS stands for:

(a) Memory Instruction Per Second

(b) Major Instruction Per Second

(c) Main Information Per Second

(d) Million Instruction Per Second ( )

30. Router is a :

(a) Data Transfer Protocol

(b) Networking device

(c) Modem

(d) None of the above ( )

Answer

1. (b)	2. (b)	3. (c)	4. (b)	5. (a)	6. (c)	7. (d)	8. (a)	9. (b)	10. (c)
11. (b)	12. (d)	13. (a)	14. (b)	15. (b)	16. (c)	17. (a)	18. (a)	19. (d)	20. (a)
21. (c)	22. (a)	23. (c)	24. (b)	25. (a)	26. (a)	27. (a)	28. (a)	29. (d)	30. (b)

Set-B

1. The channel width of a .....network increases as we ascend from leaves to the root.

(a) Binary fat tree

(b) Star

(c) Ring

(d) Binary tree ( )

2. The time required for two processes to synchronize with each other is called:

(a) Synchronization time

(b) Synchronization Latency

(c) Process Latency

(d) Memory latency ( )

3. If the number of links is 2N, then this would be which kind of network?

(a) Illiac mesh

(b) 2D Mesh

(c) Both (a) and (b)

(d) None of the above ( )

4. TLB is used in:

(a) Paging

(b) Segmentation

(c) Both (a) and (b)

(d) None of the above ( )

5. The topology of an interconnection network can be:

(a) Static (b) Dynamic

(c) Either (a) and (b) (d) None of the above ( )

6. SIMD is a :

(a) Memory management scheme

(b) Processor for multiple organization

(c) Attachment array processor

(d) Programming technique ( )

7. The diameter of a network is the:

(a) Maximum shortest path between any two nodes

(b) Minimum shortest path between any two nodes

(c) Minimum shortest path between any two adjacent nodes

(d) Minimum longest path between any two adjacent nodes ( )

8. The size of program is determined of:

(a) Clock Rate

(b) Clock Count

(c) Instruction Execution Rate

(d) Instruction count ( )

9. Multiprocessor is one with:

(a) One CPU executing several processors

(b) One CPU and several channels

(c) Several CPU

(d) None of the above ( )

10. a crossbar switch network is a :

(a) Regular connection network

(b) Irregular connection network

(c) Static connection network

(d) Dynamic connection network ( )

11. VLIW stands for:

(a) Vector Large Instruction Word

(b) Very Long Instruction Word

(c) Very Large Integrated Word

(d) Very Low Integrated Word ( )

12. The major disadvantage of pipeline is:

(a) High cost individual dedicated

(b) Initial setup time

(c) If branch instruction is encountered the pipe has to be flushed

(d) All of the above ( )

13. .....networks are controlled by a global clock

(a) Asynchronous

(b) Synchronous

(c) Both (a) and (b)

(d) Neither (a) nor (b) ( )

14. .....is a shared memory system in which the access time varies with the location of the memory word:

(a) COMA

(b) UMA

(c) NUMA

(d) All of the above ( )

15. Which is not a valid data routing function?

(a) Perfect shuffle and exchange

(b) Permutation

(c) Multicast

(d) Broadband ( )

16. To find out cache performance, we can use:

(a) Program trace driven simulation

(b) Hit Ratio

(c) Creedy Cycles

(d) Cycle count ( )

17. Which are the valid vector access memory schemes?

(a) C-access Memory Organization

(b) Synchronous Memory Organization

(c) D-Access memory organization

(d) Asynchronous memory organization ( )

18. Which of the example of blocking network?

(a) Baseline

(b) Delta

(c) Omega

(d) All of the above ( )

19. MAL stands for:

(a) Minimal Average Latency

(b) Minimum Allocation Latency

(c) Maximum Allocation Latency

(d) Maximum Average Latency ( )

20. The process of assigning control of the data transfer bus to a requester is called:

(a) Interleaving

(b) Interruption

(c) Synchronization

(d) Arbitration ( )

21. DOP stands for:

(a) Dual Operating (b) Dual of Parallelism

(c) Degree of processing (d) Degree of parallelism ( )

22. In general vector processing is faster and.....scalar processing:

(a) Less efficient than

(b) Equally efficient to

(c) More efficient than

(d) None of the above ( )

23. Processors that use multiphase clock with a much increases clock rate ranging from 100 to 500 MHz.

(a) RISC

(b) VLIW

(c) Both a and b

(d) None of the above ( )

24. .....computing is achieved through the use of an array of processing elements synchronized by the same controller;

(a) MIMD (b) SIMD

(c) Both a and b (d) None of the above ( )

25. An/a .....is a request from I/O or other devices to a processor for services or attention:

(a) Transaction (b) Arbitration

(c) Interrupt (d) None of the above ( )

26. The accumulated rate of all stage utilization determines:

(a) Bounds of MAL (b) Pipeline throughout

(c) Pipeline efficiency (d) Delay speed ( )

27. LRU stands for:

(a) Last recently used

(b) Least Recently used

(c) Last Rarely Used

(d) Least Rarely Used ( )

28. The memory hierarchy developed was based on a program behaviour is known is:

(a) Locality of reference

(b) Locality of coherence

(c) Coherence property

(d) None of the above ( )

29. In a UMA multiprocessor model all processor have.....access time to all memory words:

(a) Asynchronous

(b) Equal

(c) Different

(d) None of the above ( )

30. Throughout is measure of:

(a) Number of instruction set executed per unit of time

(b) Time for the completion of the task

(c) Work done by the CPU

(d) Memory Speed ( )

Answer

1. (a)	2. (b)	3. (c)	4. (a)	5. (c)	6. (b)	7. (a)	8. (d)	9. (a)	10. (a)
11. (b)	12. (d)	13. (b)	14. (c)	15. (d)	16. (b)	17. (a)	18. (d)	19. (a)	20. (b)
21. (d)	22. (c)	23. (c)	24. (b)	25. (c)	26. (b)	27. (b)	28. (a)	29. (b)	30. (c)

Set C

1. Cache memory is:

   (a) Temporary and costly

   (b) Primary

   (c) High speed memory

   (d) All of the above ( )

2. .....instruction is used to store the contents of accumulator into the memory word specified by the effective addresses:

   (a) LDA

   (b) BUN

   (c) STA

   (d) BSA ( )

3. What does RISC stand for?

   (a) Register Instruction Set Counter

   (b) Reduced Instruction Set Computer

   (c) Reduced Instruction Set Counter

   (d) Register Instruction Set Computer ( )

4. A computer system consists of a CPU, a memory and one or more specialized I/O processor called:

   (a) Bandwidth

   (b) Data Channels

   (c) Interrupt

   (d) None of the above ( )

5. Which of the following is bus architecture:

   (a) ISA

   (b) AGA

   (c) MCA

   (d) All of the above ( )

6. SIMM is a :

   (a) Single Instruction memory modular

   (b) Single in Line Memory Modular

   (c) Single Instruction Memory Manufacturer

   (d) Single in Line Micrograms Modular ( )

7. Which of not an address mapping scheme:

   (a) Associate Mapping

   (b) Direct Mapping

   (c) Direct Associate Mapping

   (d) Set Associate Mapping ( )

8. Example of zero address instruction is:

   (a) ADD B

(b) ADD

(c) ADD R1, B

(d) ADD R1, A, B ( )

9. The speed of microcomputer measure in:

(a) MIPS

(b) Picoseconds

(c) Megahertz

(d) Milihertz ( )

10. The memory used in a computer system is based on the following principle:

(a) Principle of parallel computing

(b) Principle of concurrent occur

(c) Principle of locality

(d) None ( )

11. Instruction to be executed resides:

(a) Program counter

(b) Accumulator

(c) MBR

(d) Instruction Register ( )

12. One nibble is equivalent to:

(a) 8 bits

(b) 4 bytes

(c) 8 bytes

(d) 4 bits ( )

13. RAID is:

(a) A computer

(b) Storage device

(c) A type of input device

(d) A type of output device ( )

14. The instruction set of a.....processor usually contains 200 to 300 instructions:

(a) CISC

(b) SMP

(c) RISC

(d) All of the above ( )

15. The transformation of data from main memory to cache memory is called:

(a) Mapping

(b) Processing

(c) Counting

(d) Multiplexing ( )

16. A memory deices in which a bit is stored as a charge across the stray capacitance:

(a) SRAM

(b) EPROM

(c) DRAM

(d) Bubble Memory ( )

17. Multiprocessor is one with:

(a) One CPU and several channels

(b) Several CPU

(c) One CPU executing several processors

(d) None of the above ( )

18. The size of virtual memory depends on:

(a) The size of data bus

(b) The size of the main memory

(c) The size of the address bus

(d) None ( )

19. Swapping is also called:

(a) Roll out technique

(b) Roll in technique

(c) Roll out roll in technique

(d) All of the above ( )

20. .....is responsible for multiplexing the CPU:

(a) Device manager

(b) Device controller

(c) Scheduler

(d) None ( )

21. The term 'Baud Rate' is a measure of the :

(a) Memory capacity

(b) Speed at which data travels over the network

(c) Instruction execution time

(d) All of the above ( )

22. Two or more CPU's present in a computer system which share some or all of the memory called:

(a) Paralled (b) Multipgramming

(c) Multi tasking (d) Random File processing ( )

23. Which mode transits data in both directions, but not at the same time:

(a) Simplex mode

(b) Half duplex mode

(c) Full duplex

(d) None ( )

24. If a process does not have direct and unassisted access to data items these items are said to be:

(a) Off line (b) Time shared

(c) On line (d) None ( )

25. Virtual memory is:

(a) A part of main memory

(b) Shared memory

(c) Part of cache memory

(d) A mechanism to process fast ( )

26. Throughout is a measures of:

(a) Memory

(b) Number of instruction sets executed per unit of time

(c) Work done by the CPU

(d) Time for the completion of the risk ( )

27. Pipelining is:

(a) Programming technique

(b) Decomposing of sequential process into sub operations

(c) Hardware module

(d) None ( )

28. Vector processing is not part of :

(a) Multiprocessing

(b) Parallel processing

(c) Batch mode processing

(d) Array processors ( )

29. Memory interleaving is:

(a) Modular memory

(b) Virtual memory

(c) Shared memory

(d) Cache memory ( )

30. SIMD is a :

(a) Memory management scheme

(b) Processor for multiple data organization

(c) Attached array processor

(d) Programming technique ( )

Answer

1. (d)	2. (c)	3. (b)	4. (d)	5. (d)	6. (a)	7. (c)	8. (b)	9. (a)	10. (c)
11. (d)	12. (d)	13. (b)	14. (a)	15. (a)	16. (c)	17. (c)	18. (c)	19. (c)	20. (c)
21. (b)	22. (a)	23. (b)	24. (a)	25. (d)	26. (b)	27. (b)	28. (c)	29. (b)	30. (b)

S

Set – D

1. .....modules are used to select one out of n read or write requested for service:

   (a) Multiplexer

   (b) Demultiplexer

   (c) Crossbar

   (d) All of the above ( )

2. In these types of computers, the execution on instruction is driven by data availability insured of being guided by a program counter:

   (a) Control Flow Computer

   (b) Data Flow Computer

   (c) Both (a) and (b)

   (d) Neither (a) nor (b) ( )

3. It manager the allocation and deal location of resources during the exeuction of user programs:

   (a) CPU

   (b) OS

   (c) Monitor

   (d) Keyboard ( )

4. Multi-processor, vector-supercomputer, and multi computer were appeared in:

   (a) 1st generation

   (b) 2nd generation

   (c) 3rd generation

   (d) 4th generation ( )

5. Full form of MIPS is:

(a) Multi instructions

(b) Million Instructions Per Second

(c) Multi Instructions Processor System

(d) None of the above ( )

6. The physical memory is uniformly shared by all the processors in:

(a) NUMA

(b) COMA

(c) UMA

(d) All of the above ( )

7. Which is not valid architecture of a vector super computer?

(a) Register to register

(b) Memory to memory

(c) Both a and b are invalid

(d) None of the above ( )

8. .....is a measure of the amount of compilation involved in a software process:

(a) Grain size (b) Granularity

(c) Both a and b (d) neither a nor b ( )

9. The diameter of a network is the :

(a) Maximum shortest path between any two nodes

(b) Minimum shortest path between any two nodes

(c) Maximum shortest path between any two adjacent nodes

(d) Minimum longest path between two adjacent nodes ( )

10. The channel width of a fat tree increase as we ascend form:

(a) Leaves to the roots

(b) Roots to the leaves

(c) Width

(d) None of the above ( )

11. The total number of messages the network can handle is:

(a) Network efficiency

(b) Network throughout

(c) Network output

(d) All of the above ( )

12. Which dynamic connection network has a low with limited bandwidth features?

(a) Multistage interconnection

(b) Crossbar switch

(c) Bus system

(d) All of the above ( )

13. Which dynamic connection network provides highest bandwidth and interconnection?

(a) Crossbar networks (b) Multi stage networks

(c) Bus system (d) None of the above ( )

14. DOP stands for:

(a) Dual Operating Processor

(b) Degree of parallelism

(c) Dual of parallelism

(d) Degree of processing ( )

15. .....is a cascade of processing stage which are linearly connected to perform a fixed function over a stream of data flowing from one end to the other:

(a) Omega network

(b) Tree Network

(c) Linear Pipeline

(d) Parallel Processor ` ( )

16. The finest level of pipelining is called:

(a) Macro pipelining

(b) Micro pipelining

(c) Man pipelining

(d) None of the above ( )

17. When the addressed data/instruction is found in cache it is called:

(a) Cache hit

(b) Cache miss

(c) Cache found

(d) Cache trace ( )

18. In proposed future bus + standard, the.....are used to declare special bus transaction:

(a) Command Lines (b) Status lines

(c) Capability lines (d) Miscellaneous lines ( )

19. The percentage of time that each pipeline stage is used over a sufficiently long series of task initiation is the:

(a) Pipeline throughout (b) Pipeline efficiency

(c) Pipeline latency (d) Pipeline clock ( )

20. The effective bandwidth available to each processor is inversely proportional to.....contending for the bus

(a) Number of terminal

(b) Number of processor

(c) Number of operating systems

(d) All of the above ( )

21. Flynn's classification is based on:

(a) Memory instructions

(b) Hardware types

(c) Software types

(d) Notion of instruction and data streams ( )

22. The size of program is determined by:

(a) Clock Rate

(b) Instruction Execution Rate

(c) Instruction Count

(d) Clock Count ( )

23. The.....model is a special case of NUMA machine, in which the distributed main memories are converted to caches:

(a) UMA

(b) Special NUMA

(c) COMA

(d) None of the above ( )

24. The.....network provide point to point static connections among the nodes:

(a) Message passing (b) Data Passing

(c) Both a and b (d) Neither a nor b ( )

25. MAL stands for:

(a) Minimum allocation Latency

(b) Minimal Average Latency

(c) Maximum Average Latency

(d) Maximum Allocation Latency ( )

26. Latencies that causes collision are called:

(a) Minimum Allocation Latency

(b) Minimal Average Latency

(c) Maximum Average Latency

(d) Maximum Allocation Latency ( )

27. .....is a pair of nodes that accounts for a disproportionately large portion of the total network traffic.

(a) Hit ration

(b) Hot ratio

(c) Hot spot

(d) Hit spot ( )

28. The memory hierarchy developed was based on a program behaviour is known as:

(a) Coherence property

(b) Locality of reference

(c) Locality of coherence

(d) None of the above ( )

29. Write through and write back are two strategies for maintaining:

(a) Locality of reference (b) Collision

(c) Coherence (d) All of the above ( )

30. In paging, if demanded page is not found it is declared is:

(a) Page miss

(b) Page fault

(c) Both a and b

(d) Electronic data interchange for administration commerce and trade ( )

Answer

1. (a)	2. (b)	3. (b)	4. (d)	5. (b)	6. (c)	7. (d)	8. (a)	9. (a)	10. (a)
11. (b)	12. (c)	13. (a)	14. (b)	15. (c)	16. (b)	17. (a)	18. (a)	19. (c)	20. (b)
21. (d)	22. (c)	23. (b)	24. (a)	25. (b)	26. (c)	27. (c)	28. (b)	29. (d)	30. (b)

BACHELOR OF COMPUTER APPLICATIONS

(Part III) EXAMINATION

(Faculty of Science)

(Three – Year Scheme of 10+2+3 Pattern)

PAPER 314

ADVANCED COMPUTER ARCHITECTURE

OBJECTIVE PART- I

Year - 2011

Time allowed : One Hour *Maximum Marks : 20*

The question paper contains 40 multiple choice questions with four choices and students will have to pick the correct one. (Each carrying ½ marks.).

1. TLB is used in:
   (a) Paging
   (b) Segmentation
   (c) Both (a) and (b)
   (d) None of the above (c)

2. The size of Program is determined by:

   (a) Clock Rate

(b) Clock Count

(c) Instruction Execution Rate

(d) Instruction count ( )

3. VLIW stands for:

(a) Vector large instruction word

(b) Very long instruction word

(c) Very large integrated word

(d) Very low integrated word ( )

4. .....networks are controlled by a global clock.

(a) Asynchronous

(b) Synchronous

(c) Both (a) and (b)

(d) Neither (a) nor (b) ( )

5. LRU stands for:

(a) Last recently used (b) Least recently used

(c) Last rarely used (d) None of the above ( )

6. Router is a :

(a) Data transfer protocol

(b) Networking device

(c) Modem

(d) None of the above ( )

7. Personal computer were appeared in:

(a) Ist generation

(b) IInd generation

(c) IVth generation

(d) Vth generation ( )

8. Cache memory is:

(a) Temporary and costly

(b) Primary

(c) High speed memory

(d) All of the above ( )

9. SIMM is a :

(a) Single Instruction Memory Modular

(b) Single in-Line memory modular

(c) Single instruction memory manufacturer

(d) Single In-Line Micro programs Modular ( )

10. The speed of microcomputer is measured in:

(a) MIPS (b) Picoseconds

(c) Megahertz (d) Millihertz ( )

11. One nibble is equivalent to:

(a) 8-bits

(b) 4-bytes

(c) 8-bytes

(d) 4-bits ( )

12. Virtual memory is:

(a) A part of main memory

(b) Shared memory

(c) Part of cache memory

(d) A mechanism to execute large size programs ( )

13. Which gate is a universal gate?

(a) NAND

(b) OR

(c) AND

(d) None of the above ( )

14. If a process does not have direct and unassisted access to data items, these items are said to be:

(a) Off-line

(b) Time shared

(c) On-line

(d) None of the above ( )

15. Vector processing is not par to of:

(a) Multiprocessing

(b) Parallel processing

(c) Batch mode processing

(d) Array processors ( )

16. Swapping is also called:

(a) Roll out technique

(b) Roll in technique

(c) Roll out roll in technique

(d) All of the above ( )

17. Full form of MIPS is:

(a) Multi Instructions Per Second

(b) Million Instructions Per Second

(c) Million Instruction Processor System

(d) None of the above ( )

18. The total number of message the network can handle in:

(a) Network Efficiency

(b) Network throughput

(c) Network output

(d) All of the above ( )

19. Flynn's classification is based on:

(a) Memory Instruction

(b) Hardware types

(c) Software types

(d) Notation of instructions and data streams ( )

20. In Paging, if demanded page is not found it is declared as:

(a) Page miss

(b) Page Fault

(c) Both (a) and (b)

(d) Neither (a) nor (b) ( )

21. Omega Network is a.....network.

(a) High stage

(b) Low stage

(c) Single stage

(d) Multistage ( )

22. For a reservation table with n columns, the maximum forbidden latency (m) :

(a) $m \leq n$

(b) $m \leq n - n$

(c) $m \geq n$

(d) $m \geq n - 1$ ( )

23. Switching complexity of multistage network is:

(a) $O(\log_k n)$

(b) $O(\omega)$

(c) $O(n \log_k n)$

(d) O (n) ( )

24. The full form of PRAM is:

(a) Parallel Random Access Machine

(b) Parallel Remote Access Machine

(c) Powerful Random Access Memory

(d) Partial Random Access Memory ( )

25. In Binary tree network the bisection width would be:

(a) 1

(b) 2

(c) N/2

(d) $(N/2)^2$ ( )

26. The T3D is a :

(a) SIMD machine

(b) MIMD machine

(c) Both (a) and (b)

(d) None of the above ( )

27. In future Bus + standard, the 64-bit address line are multiplexed with:

(a) Lower order 64-bit data lines

(b) High order 64-bit data lines

(c) Lower order 32-bit data lines

(d) Any one of the above ( )

28. The dimensions of locality property are:

(a) Temporal, parallel and sequential

(b) Temporal, spatial and sequential

(c) Spatial, parallel and sequential

(d) None of the above ( )

29. Pipelining is:

(a) Programming Techniques

(b) Decomposing of sequential process into sub operations

(c) Hardware module

(d) None of the above ( )

30. Which is example of blocking network?

(a) Baseline

(b) Omega

(c) Delta

(d) All of the above ( )

31. Bootstrap is:

(a) A memory device (b) A startup program

(c) Error correction technique (d) None of the above ( )

32. Only.....of the instruction of a complex instruction set are frequently used about 95% of the time:

(a) 75%

(b) 25%

(c) 80%

(d) 30% ( )

33. An asynchronous bus allow.....device(s) to be connected on the same bus.

(a) Fast

(b) Slow

(c) Fast and Slow

(d) None of the above ( )

34. Ideally, linear pipeline of k stage can process n tasks in.....Time:

(a) [n + (k – 1)]

(b) [n + (k + 1)]

(c) [k + (n –1)]

(d) [k – (n + 1)] ( )

35. Which of the following is/are representative CISC scalar processor?

(a) Intel i 486 (b) Motorola MC 68040

(c) NS 32532 (d) All of the above ( )

36. Which of the following is/are supercomputer?

(a) Cray Y-MP

(b) NEC SX2

(c) Fujitsu VP 400

(d) All of the above ( )

37. In Pipelined instruction Processing the.....process the instruction function to be performed and identified the resources needed.

(a) Fetch stage

(b) Decode stage

(c) Issue stage

(d) Write back stage ( )

38. A crossbar switch network is a/an:

(a) Dynamic Connection Network

(b) Static Connection Network

(c) Regular Connection Network

(d) Irregular Connection Network ( )

39. The problem of aliasing is associated with.....cache.

(a) Physical address

(b) Virtual address

(c) Split cache

(d) Both (a) and (b) ( )

40. CPI stands for:

(a) Cycle Per Instruction

(b) Communication Process Interconnect

(c) Calls Per instruction

(d) None of the above ( )

DESCRIPTIVE PART-II

Year- 2011

Time allowed : 2 Hours ***Maximum Marks : 30***

Attempt any four descriptive types of questions out of the six. All questions carry 7½ marks each.

1. Define the following:
   (i) BUS;
   (ii) Primary and Secondary Memory;
   (iii) RAM and ROM;
   (iv) Processor;
   (v) Cache Memory

2. (a) What do you mean by pipelining? How do improve performance of a computer system using pipelining?

   (b) Compare Linear and non-linear pipelined processor.

3. (a) Compare CISC and RISC.

   (b) Write a short note on Shared Memory?

4. (a) What are various conditions of Parallelism.

   (b) Write short note on Static Interconnection Network and Dynamic Interconnection Network.

5. (a) Explain virtual memory management technology?

   (b) Write a short note on Vector on Processing.

6. Write short notes on the following:

   (a) SIMD computers;

   (b) Program Flow mechanisms;

   (c) Vector VLIW and symbolic processors.

BACHELOR OF COMPUTER APPLICATIONS

(Part III) EXAMINATION

(Faculty of Science)

(Three – Year Scheme of 10+2+3 Pattern)

PAPER 314

ADVANCED COMPUTER ARCHITECTURE

OBJECTIVE PART- I

~~Year - 2010~~

Time allowed : One Hour *Maximum Marks : 20*

The question paper contains 40 multiple choice questions with four choices and students will have to pick the correct one. (Each carrying ½ marks.).

1. RISC stands for:

   (a) Register Instruction Set Computer

   (b) Reduced Instruction Set Computer

   (c) Reduced Instruction Set Clock

   (d) None of the above ( )

2. CISC processor have.....length instruction format.

(a) Variable

(b) Fixed

(c) Can not say

(d) None of the above ( )

3. CISC stands for:

(a) Clock Instruction Set Computer

(b) Control Instruction Set Computer

(c) Complex Instruction Set Computer

(d) None of the above ( )

4. .....is a term used to denote a large class of techniques that are used to provide simultaneous data processing tasks

(a) Shared memory

(b) Parallel Processing

(c) Memory hierarchy

(d) None of the above ( )

5. .....is a technique of decomposing a sequential process into sub operations.

(a) Pipelining (b) Parallel Processing

(c) Vector Processing (d) None of the above ( )

6. Personal computer were appeared in:

(a) Ist generation

(b) 2nd generation

(c) 4th generation

(d) 5th generation ( )

7. A.....contains the address of the next instructions to be executed.

(a) Data Register

(b) Accumulator

(c) Instruction Register

(d) Program Counter ( )

8. A.....is an interconnected set of processing elements which cooperate by communicating with one another to solve large problem

(a) Parallel Computer

(b) Personal Computer

(c) Laptop Computer

(d) None of the above ( )

9. Many operating system are designed to enable the CPU to process a number of independent program concurrently. This concept is called:

(a) Cache Memory

(b) Multiprogramming

(c) Multiprocessor

(d) None of the above ( )

10. A.....system is an interconnection of two more CPU with memory and I/O equipment.

(a) Processor (b) Synchronization

(c) Multiprocessor (d) None of the above ( )

11. MIMD stands for:

(a) More Instruction Stream, Multiple data Stream

(b) Multiple Instruction Stream, Multiple Data Stream

(c) Many Instruction Stream, Many Data Stream

(d) None of the above ( )

12. The components that form a multiprocessor system are:

(a) CPUs (b) IOPs

(c) Memory Unit (d) All of the above ( )

13. Computers are interconnected with each other by means of communication lines to form a:

(a) Computer Network

(b) Multiprocessor

(c) Data Dependency

(d) None of the above ( )

14. A multiprocessor system with common shared memory is called:

(a) Loosely coupled system

(b) Tightly coupled system

(c) Both a and b

(d) None of the above ( )

15. Loosely coupled system are more efficient when the interaction between task is:

(a) Maximum (b) Minimum

(c) Can not say (d) None of the above ( )

16. In a .....has it own private local memory

(a) Crossbar switch

(b) Tightly coupled system

(c) Loosely coupled system

(d) None of the above ( )

17. The memory connected to the common system bus is.....by all processors.

(a) Shared (b) Partitioned

(c) Distributed (d) None of the above ( )

18. The .....organization consists of number of cross points that are placed at intersection between buses and memory module paths

(a) Multiport memory (b) Crossbar switch

(c) Multistage switch (d) None of the above ( )

19. A bus that connects components in a multiprocessor system, is called:

(a) Control bus

(b) Data bus

(c) Address bus

(d) System bus ( )

20. A typical system bus consists of approximately.....signals lines

(a) 100 (b) 2

(c) 3 (d) None of the above ( )

21. The signal lines in system bus are divided into.....functional groups.

(a) 1 (b) 2

(c) 3 (d) None of the above ( )

22. The purpose of parallel processing is to:

(a) Speed up the processing

(b) Increase memory

(c) Decrease memory

(d) None of the above ( )

23. M.J. Flynn's parallel processing classification is based on:

(a) Multiple Instructions

(b) Multiple data

(c) Both (a) and (b)

(d) None of the above ( )

24. .....represents an organization that includes many processing units under the supervision of a common control unit.

(a) SISD (b) SIMD

(c) MIMD (d) None of the above ( )

25. A.....can be be visualized as a collection of processing segments through which binary information flows:

(a) Memory (b) I/O devices

(c) Processor (d) Pipeline ( )

26. The pipeline used for floating point operations is called:

(a) Arithmetic pipeline (b) Instruction pipeline

(c) Both (a) and (b) (d) None of the above ( )

27. The finest level of pipelining is called:

(a) Micro pipelining

(b) Macro pipelining

(c) Linear pipelining

(d) None of the above ( )

28. VLIW stands for:

(a) Very Long Instruction Word

(b) Very Long Instruction Word

(c) Very Large Information Word

(d) None of the above ( )

29. MIPS stands for:

(a) Memory Instruction Per Second

(b) Major Instruction Per Second

(c) Main Information Per Second

(d) Million Instruction Per Second ( )

30. Router is a :

(a) Data Transfer Protocol

(b) Networking device

(c) Modem

(d) None of the above ( )

31. Two or more CPUs present in a computer system which share some or all of the memory?

(a) Parallel Processing

(b) Multiprogramming

(c) Random file processing

(d) Multitasking ( )

32. Flynn's classified parallel computers into.....categories.

(a) 2

(b) 3

(c) 4

(d) 8 ( )

33. Which of the following is an interconnection network?

(a) Time shared common bus (b) Crossbar switch

(c) Multistage switch (d) All of the above ( )

34. Through is measure of:

(a) Number of instruction set executed per unit of time

(b) Time for the completion of the task

(c) Work done by the CPU

(d) Memory speed ( )

35. DOP stands for:

(a) Dual Operating Processor

(b) Dual of Parallelism

(c) Degree of Processing

(d) Memory speed ( )

36. .....Networking are controlled by a global clock.

(a) Asynchronous

(b) Synchronous

(c) Both (a) and (b)

(d) None of the above ( )

37. Multiprocessor is one with:

(a) One CPU executing several processor

(b) Several CPU

(c) One CPU and several channels

(d) None of the above ( )

38. The topology of an interconnection network can be:

(a) Dynamic (b) Static

(c) Both a and b (d) None of the above ( )

39. To find out cache performance we can use:

(a) Program trace driven simulation

(b) Hit ration

(c) Greedy cycles

(d) Cycle Count ( )

40. .....is a concept used in some large computer systems that permit the user to construct programs as thought a large memory space.

(a) Cache memory

(b) Random access memory

(c) Virtual memory

(d) None of the above ( )

Answer Key

1. (b)	2. (b)	3. (c)	4. (b)	5. (a)	6. (c)	7. (d)	8. (a)	9. (b)	10. (c)
11. (b)	12. (d)	13. (a)	14. (b)	15. (b)	16. (c)	17. (a)	18. (a)	19. (d)	20. (a)
21. (c)	22. (a)	23. (c)	24. (b)	25. (a)	26. (a)	27. (a)	28. (a)	29. (d)	30. (b)
31. (d)	32. (c)	33. (b)	34. (a)	35. (d)	36. (b)	37. (b)	38. (c)	39. (b)	40. (c)

DESCRIPTIVE PART-II

Year- 2010

Time allowed : 2 Hours ***Maximum Marks : 30***

Attempt any four descriptive types of questions out of the six. All questions carry 7½ marks each.

Q.1 (a) What is meant by Parallelism? What are conditions of parallelism? Discuss the network properties.
(b) Explain the static interconnection network.

Q.2 Write short notes on:
(a) Superscalar
(b) Memory hierarchy technology

Q.3 Differentiate the following :
(a) Linear and non-linear Pipeline Processors;
(b) Static and Dynamic Interconnection network.

Q.4 (a) What is meant by cache memory? Discuss the virtual memory technology
(b) Write short note on shared memory

Q.5 (a) What is meant by pipelining? Discuss the instruction pipeline design.
(b) Explain RISC processors.

Q.6 Write short notes on:
(a) Buses;
(b) Multi vector Multiprocessors;
(c) VLIW

———

OBJECTIVE PART- I

Year - 2009

Time allowed : One Hour *Maximum Marks : 20*

The question paper contains 40 multiple choice questions with four choices and student will have to pick the correct one. (Each carrying ½ marks.).

1. The channel width of a .....network increases as we ascend from leaves to the root.

   (a) Binary fat tree

   (b) Star

   (c) Ring

   (d) Binary tree ( )

2. The time required for two processes to synchronize with each other is called:

   (a) Synchronization time

   (b) Synchronization Latency

   (c) Process Latency

   (d) Memory latency ( )

3. If the number of links is 2N, then this would be which kind of network?

   (a) Illiac mesh

   (b) 2D Mesh

(c) Both (a) and (b)

(d) None of the above ( )

4. TLB is used in:

(a) Paging

(b) Segmentation

(c) Both (a) and (b)

(d) None of the above ( )

5. The topology of an interconnection network can be:

(a) Static (b) Dynamic

(c) Either (a) and (b) (d) None of the above ( )

6. SIMD is a :

(a) Memory management scheme

(b) Processor for multiple organization

(c) Attachment array processor

(d) Programming technique ( )

7. The diameter of a network is the:

(a) Maximum shortest path between any two nodes

(b) Minimum shortest path between any two nodes

(c) Minimum shortest path between any two adjacent nodes

(d) Minimum longest path between any two adjacent nodes ( )

8. The size of program is determined of:

(a) Clock Rate

(b) Clock Count

(c) Instruction Execution Rate

(d) Instruction count ( )

9. Multiprocessor is one with:

(a) One CPU executing several processors

(b) One CPU and several channels

(c) Several CPU

(d) None of the above ( )

10. a crossbar switch network is a :

(a) Regular connection network

(b) Irregular connection network

(c) Static connection network

(d) Dynamic connection network ( )

11. VLIW stands for:

(a) Vector Large Instruction Word

(b) Very Long Instruction Word

(c) Very Large Integrated Word

(d) Very Low Integrated Word ( )

12. The major disadvantage of pipeline is:

(a) High cost individual dedicated

(b) Initial setup time

(c) If branch instruction is encountered the pipe has to be flushed

(d) All of the above ( )

13. .....networks are controlled by a global clock

(a) Asynchronous

(b) Synchronous

(c) Both (a) and (b)

(d) Neither (a) nor (b) ( )

14. .....is a shared memory system in which the access time varies with the location of the memory word:

(a) COMA

(b) UMA

(c) NUMA

(d) All of the above ( )

15. Which is not a valid data routing function?

(a) Perfect shuffle and exchange

(b) Permutation

(c) Multicast

(d) Broadband ( )

16. To find out cache performance, we can use:

(a) Program trace driven simulation

(b) Hit Ratio

(c) Creedy Cycles

(d) Cycle count ( )

17. Which are the valid vector access memory schemes?

(a) C-access Memory Organization

(b) Synchronous Memory Organization

(c) D-Access memory organization

(d) Asynchronous memory organization ( )

18. Which of the example of blocking network?

(a) Baseline

(b) Delta

(c) Omega

(d) All of the above ( )

19. MAL stands for:

(a) Minimal Average Latency

(b) Minimum Allocation Latency

(c) Maximum Allocation Latency

(d) Maximum Average Latency ( )

20. The process of assigning control of the data transfer bus to a requester is called:

(a) Interleaving

(b) Interruption

(c) Synchronization

(d) Arbitration ( )

21. DOP stands for:

(a) Dual Operating (b) Dual of Parallelism

(c) Degree of processing (d) Degree of parallelism ( )

22. In general vector processing is faster and.....scalar processing:

(a) Less efficient than

(b) Equally efficient to

(c) More efficient than

(d) None of the above ( )

23. Processors that use multiphase clock with a much increases clock rate ranging from 100 to 500 MHz.

(a) RISC

(b) VLIW

(c) Both a and b

(d) None of the above ( )

24. .....computing is achieved through the use of an array of processing elements synchronized by the same controller;

(a) MIMD (b) SIMD

(c) Both a and b (d) None of the above ( )

25. An/a .....is a request from I/O or other devices to a processor for services or attention:

(a) Transaction (b) Arbitration

(c) Interrupt (d) None of the above ( )

26. The accumulated rate of all stage utilization determines:

(a) Bounds of MAL (b) Pipeline throughout

(c) Pipeline efficiency (d) Delay speed ( )

27. LRU stands for:

(a) Last recently used

(b) Least Recently used

(c) Last Rarely Used

(d) Least Rarely Used ( )

28. The memory hierarchy developed was based on a program behaviour is known is:

(a) Locality of reference

(b) Locality of coherence

(c) Coherence property

(d) None of the above ( )

29. In a UMA multiprocessor model all processor have.....access time to all memory words:

(a) Asynchronous

(b) Equal

(c) Different

(d) None of the above ( )

30. Throughout is measure of:

(a) Number of instruction set executed per unit of time

(b) Time for the completion of the task

(c) Work done by the CPU

(d) Memory Speed ( )

31. A asynchronous bus allows.....devices to be connected on the same bus:

(a) Fast

(b) Fast and flow

(c) Broadway

(d) Slow ( )

32. Omega network is a .....network:

(a) High Stage

(b) Low Stage

(c) Single Stage

(d) Multistage ( )

33. .....is a pair of nodes that accounts for a disproportionately large portion of the total network traffic.

(a) Hot spot

(b) Hit Spot

(c) Hot ratio

(d) Hit ratio ( )

34. MIPS stands for:

(a) Memory Instructions Per Second

(b) Major Instructions Per Second

(c) Main Instructions Per Second

(d) Million Instructions Per Second ( )

35. The finest level of pipelining is called:

(a) Micro pipelining (b) Macro pipelining

(c) Linear Pipeline processor (d) None of the above ( )

36. Router is a :

(a) Data Transfer protocol

(b) Networking device

(c) Modem

(d) None of the above ( )

37. Two or more CPUs present in a computer system which share some or all of the memory:

(a) Parallel Processing

(b) Multiprogramming

(c) Random file processing

(d) Multitasking ( )

38. A non-linear pipeline allows:

(a) Vector large instruction word

(b) Very low integrated word

(c) Very large integrated word

(d) Very long instruction word ( )

39. Which of not an address mapping scheme:

(a) Associate mapping

(b) Direct Associate Mapping

(c) Direct Mapping

(d) Set Associate Mapping ( )

40. Personal computers were appeared in:

(a) I^{st} generation

(b) 2^{nd} generation

(c) 4^{th} generation

(d) 5th generation ( )

Answer Key

1. (a)	2. (b)	3. (c)	4. (a)	5. (c)	6. (b)	7. (a)	8. (d)	9. (a)	10. (a)
11. (b)	12. (d)	13. (b)	14. (c)	15. (d)	16. (b)	17. (a)	18. (d)	19. (a)	20. (b)
21. (d)	22. (c)	23. (c)	24. (b)	25. (c)	26. (b)	27. (b)	28. (a)	29. (b)	30. (c)
31. (b)	32. (d)	33. (b)	34. (d)	35. (b)	36. (b)	37. (b)	38. (d)	39. (c)	40. (c)

DESCRIPTIVE PART - II

Year 2009

Time allowed : 2 Hours ***Maximum Marks : 30***

Attempt any four questions out of the six. All questions carry 7½ marks each.

Q.1 (a) Discuss and describe a typical superscalar architecture for a RISC processor.

(b) What do you understand by superscalar and vector processes?

Q.2 (a) Distinguish between multiprocessors and multicomputer.

(b) Describe the UMA; NUMA and COMA shared memory multiprocessor models.

Q.3 Discuss the following cache performance issues:

(a) Hit Ratio

(b) Effect of block size

(c) Cycle Counts.

Q.4 (a) Discuss the terms data transfer bus (DTB) bus arbitration and control and Financial modules related to backplane bus.

(b) What do you mean by Backplane Bus system?

Q.5 (a) What do you mean by dynamic interconnection network?

(b) Discuss various factors which affect the performance of an interconnection network.

Q.6 What is the basic difference between a linear pipeline processor and non-linear pipeline processor? Discuss the asynchronous and synchronous models of linear pipeline processor.

_____

OBJECTIVE PART- I

Year - 2008

Time allowed : One Hour *Maximum Marks : 20*

The question paper contains 40 multiple choice questions with four choices and student will have to pick the correct one. (Each carrying ½ marks.).

1. Cache memory is:

   (a) Temporary and costly

   (b) Primary

   (c) High speed memory

   (d) All of the above ( )

2. .....instruction is used to store the contents of accumulator into the memory word specified by the effective addresses:

   (a) LDA

   (b) BUN

   (c) STA

   (d) BSA ( )

3. What does RISC stand for?

   (a) Register Instruction Set Counter

   (b) Reduced Instruction Set Computer

(c) Reduced Instruction Set Counter

(d) Register Instruction Set Computer ( )

4. A computer system consists of a CPU, a memory and one or more specialized I/O processor called:

(a) Bandwidth

(b) Data Channels

(c) Interrupt

(d) None of the above ( )

5. Which of the following is bus architecture:

(a) ISA

(b) AGA

(c) MCA

(d) All of the above ( )

6. SIMM is a :

(a) Single Instruction memory modular

(b) Single in Line Memory Modular

(c) Single Instruction Memory Manufacturer

(d) Single in Line Micrograms Modular ( )

7. Which of not an address mapping scheme:

(a) Associate Mapping

(b) Direct Mapping

(c) Direct Associate Mapping

(d) Set Associate Mapping ( )

8. Example of zero address instruction is:

(a) ADD B

(b) ADD

(c) ADD R1, B

(d) ADD R1, A, B ( )

9. The speed of microcomputer measure in:

(a) MIPS

(b) Picoseconds

(c) Megahertz

(d) Milihertz ( )

10. The memory used in a computer system is based on the following principle:

(a) Principle of parallel computing

(b) Principle of concurrent occur

(c) Principle of locality

(d) None ( )

11. Instruction to be executed resides:

(a) Program counter

(b) Accumulator

(c) MBR

(d) Instruction Register ( )

12. One nibble is equivalent to:

(a) 8 bits

(b) 4 bytes

(c) 8 bytes

(d) 4 bits ( )

13. RAID is:

(a) A computer

(b) Storage device

(c) A type of input device

(d) A type of output device ( )

14. The instruction set of a.....processor usually contains 200 to 300 instructions:

(a) CISC

(b) SMP

(c) RISC

(d) All of the above ( )

15. The transformation of data from main memory to cache memory is called:

(a) Mapping

(b) Processing

(c) Counting

(d) Multiplexing ( )

16. A memory deices in which a bit is stored as a charge across the stray capacitance:

(a) SRAM

(b) EPROM

(c) DRAM

(d) Bubble Memory ( )

17. Multiprocessor is one with:

(a) One CPU and several channels

(b) Several CPU

(c) One CPU executing several processors

(d) None of the above ( )

18. The size of virtual memory depends on:

(a) The size of data bus

(b) The size of the main memory

(c) The size of the address bus

(d) None ( )

19. Swapping is also called:

(a) Roll out technique

(b) Roll in technique

(c) Roll out roll in technique

(d) All of the above ( )

20. .....is responsible for multiplexing the CPU:

(a) Device manager

(b) Device controller

(c) Scheduler

(d) None ( )

21. The term 'Baud Rate' is a measure of the :

(a) Memory capacity

(b) Speed at which data travels over the network

(c) Instruction execution time

(d) All of the above ( )

22. Two or more CPU's present in a computer system which share some or all of the memory called:

(a) Paralled (b) Multipgramming

(c) Multi tasking (d) Random File processing ( )

23. Which mode transits data in both directions, but not at the same time:

(a) Simplex mode

(b) Half duplex mode

(c) Full duplex

(d) None ( )

24. If a process does not have direct and unassisted access to data items these items are said to be:

(a) Off line (b) Time shared

(c) On line (d) None ( )

25. Virtual memory is:

(a) A part of main memory

(b) Shared memory

(c) Part of cache memory

(d) A mechanism to process fast ( )

26. Throughout is a measures of:

(a) Memory

(b) Number of instruction sets executed per unit of time

(c) Work done by the CPU

(d) Time for the completion of the risk ( )

27. Pipelining is:

(a) Programming technique

(b) Decomposing of sequential process into sub operations

(c) Hardware module

(d) None ( )

28. Vector processing is not part of :

(a) Multiprocessing

(b) Parallel processing

(c) Batch mode processing

(d) Array processors ( )

29. Memory interleaving is:

(a) Modular memory

(b) Virtual memory

(c) Shared memory

(d) Cache memory ( )

30. SIMD is a :

(a) Memory management scheme

(b) Processor for multiple data organization

(c) Attached array processor

(d) Programming technique ( )

31. Multi-programming is:

(a) A technique to perform more than one task in memory

(b) Capability to keep more than one program

(c) A technique to perform paralel processing

(d) None of the above ( )

32. The major disadvantages of pipelining is :

(a) Initial setup time

(b) If branch instruction is encountered the pipe has to be flushed

(c) High cost of individual dedicated

(d) All of the above ( )

33. Bootstrap is:

(a) A memory device

(b) a device to support the computer

(c) A startup correction technique

(d) an error correction technique ( )

34. Asynchronous communication protocols:

(a) Transmit data in blocks

(b) Serial data transfer

(c) Continuous data transfer

(d) Discontinuous data transfer ( )

35. Router is a:

(a) Networking device

(b) Data transfer protocol

(c) Modem

(d) None ( )

36. Bus is a:

(a) Logical Channel for transferring data

(b) Electronic pathway for transferring data

(c) Dedicated path

(d) None ( )

37. Which one not deal in network component ?

(a) Novel

(b) CISCO

(c) Dell

(d) Microsoft ( )

38. Which gate is a universal gate?

(a) NAND

(b) OR

(c) AND

(d) None ( )

39. Which company does no deal with computer hardware?

(a) IBM

(b) Microsoft

(c) HCL

(d) Zenith ( )

40. The size of program is determined by:

(a) Clock rate (b) Clock count

(c) Instruction execution (d) Instruction count ( )

Answer Key

1. (d)	2. (c)	3. (b)	4. (d)	5. (d)	6. (a)	7. (c)	8. (b)	9. (a)	10. (c)
11. (d)	12. (d)	13. (b)	14. (a)	15. (a)	16. (c)	17. (c)	18. (c)	19. (c)	20. (c)
21. (b)	22. (a)	23. (b)	24. (a)	25. (d)	26. (b)	27. (b)	28. (c)	29. (b)	30. (b)
31. (a)	32. (d)	33. (c)	34. (a)	35. (a)	36. (a)	37. (c)	38. (a)	39. (b)	40. (d)

DESCRIPTIVE PART - II

Year 2008

Time allowed : 2 Hours ***Maximum Marks : 30***

Attempt any four questions out of the six. All questions carry 7½ marks each.

Q.1 What do you understand with virtual memory? Describe the page replacement techniques in virtual memory

Q.2 Write short notes on the following:

(a) Memory Hierarchy

(b) Characteristics of multiprocessors

Q.3 Explain the interconnection structures of network. Describe the multistage switching network with the help of diagram.

Q.4 What do you understand with pipelining processor? Describe the arithmetic pipeline with the help of example

Q.5 Describe:

(i) Vector Processing principles

(ii) Memory interleaving

Q.6 Differentiate between the RISC and CISC processors. Explain also the characteristics of both.

———

OBJECTIVE PART- I

Year - 2007

Time allowed : One Hour *Maximum Marks : 20*

The question paper contains 40 multiple choice questions with four choices and student will have to pick the correct one. (Each carrying ½ marks.).

1. .....modules are used to select one out of n read or write requested for service:

   (a) Multiplexer

   (b) Demultiplexer

   (c) Crossbar

   (d) All of the above ( )

2. In these types of computers, the execution on instruction is driven by data availability insured of being guided by a program counter:

   (a) Control Flow Computer

   (b) Data Flow Computer

   (c) Both (a) and (b)

   (d) Neither (a) nor (b) ( )

3. It manager the allocation and deal location of resources during the exeuction of user programs:

   (a) CPU

(b) OS

(c) Monitor

(d) Keyboard ( )

4. Multi-processor, vector-supercomputer, and multi computer were appeared in:

(a) 1st generation

(b) 2nd generation

(c) 3rd generation

(d) 4th generation ( )

5. Full form of MIPS is:

(a) Multi instructions

(b) Million Instructions Per Second

(c) Multi Instructions Processor System

(d) None of the above ( )

6. The physical memory is uniformly shared by all the processors in:

(a) NUMA

(b) COMA

(c) UMA

(d) All of the above ( )

7. Which is not valid architecture of a vector super computer?

(a) Register to register

(b) Memory to memory

(c) Both a and b are invalid

(d) None of the above ( )

8. .....is a measure of the amount of compilation involved in a software process:

(a) Grain size (b) Granularity

(c) Both a and b (d) neither a nor b ( )

9. The diameter of a network is the :

(a) Maximum shortest path between any two nodes

(b) Minimum shortest path between any two nodes

(c) Maximum shortest path between any two adjacent nodes

(d) Minimum longest path between two adjacent nodes ( )

10. The channel width of a fat tree increase as we ascend form:

(a) Leaves to the roots

(b) Roots to the leaves

(c) Width

(d) None of the above ( )

11. The total number of messages the network can handle is:

(a) Network efficiency

(b) Network throughout

(c) Network output

(d) All of the above ( )

12. Which dynamic connection network has a low with limited bandwidth features?

(a) Multistage interconnection

(b) Crossbar switch

(c) Bus system

(d) All of the above ( )

13. Which dynamic connection network provides highest bandwidth and interconnection?

(a) Crossbar networks (b) Multi stage networks

(c) Bus system (d) None of the above ( )

14. DOP stands for:

(a) Dual Operating Processor

(b) Degree of parallelism

(c) Dual of parallelism

(d) Degree of processing ( )

15. .....is a cascade of processing stage which are linearly connected to perform a fixed function over a stream of data flowing from one end to the other:

(a) Omega network

(b) Tree Network

(c) Linear Pipeline

(d) Parallel Processor ` ( )

16. The finest level of pipelining is called:

(a) Macro pipelining

(b) Micro pipelining

(c) Man pipelining

(d) None of the above ( )

17. When the addressed data/instruction is found in cache it is called:

(a) Cache hit

(b) Cache miss

(c) Cache found

(d) Cache trace ( )

18. In proposed future bus + standard, the.....are used to declare special bus transaction:

(a) Command Lines (b) Status lines

(c) Capability lines (d) Miscellaneous lines ( )

19. The percentage of time that each pipeline stage is used over a sufficiently long series of task initiation is the:

(a) Pipeline throughout (b) Pipeline efficiency

(c) Pipeline latency (d) Pipeline clock ( )

20. The effective bandwidth available to each processor is inversely proportional to.....contending for the bus

(a) Number of terminal

(b) Number of processor

(c) Number of operating systems

(d) All of the above ( )

21. Flynn's classification is based on:

(a) Memory instructions

(b) Hardware types

(c) Software types

(d) Notion of instruction and data streams ( )

22. The size of program is determined by:

(a) Clock Rate

(b) Instruction Execution Rate

(c) Instruction Count

(d) Clock Count ( )

23. The.....model is a special case of NUMA machine, in which the distributed main memories are converted to caches:

(a) UMA

(b) Special NUMA

(c) COMA

(d) None of the above ( )

24. The.....network provide point to point static connections among the nodes:

(a) Message passing (b) Data Passing

(c) Both a and b (d) Neither a nor b ( )

25. MAL stands for:

(a) Minimum allocation Latency

(b) Minimal Average Latency

(c) Maximum Average Latency

(d) Maximum Allocation Latency ( )

26. Latencies that causes collision are called:

(a) Minimum Allocation Latency

(b) Minimal Average Latency

(c) Maximum Average Latency

(d) Maximum Allocation Latency ( )

27. .....is a pair of nodes that accounts for a disproportionately large portion of the total network traffic.

(a) Hit ration

(b) Hot ratio

(c) Hot spot

(d) Hit spot ( )

28. The memory hierarchy developed was based on a program behaviour is known as:

(a) Coherence property

(b) Locality of reference

(c) Locality of coherence

(d) None of the above ( )

29. Write through and write back are two strategies for maintaining:

(a) Locality of reference (b) Collision

(c) Coherence (d) All of the above ( )

30. In paging, if demanded page is not found it is declared is:

(a) Page miss

(b) Page fault

(c) Both a and b

(d) Electronic data interchange for administration commerce and trade ( )

31. LRU stands for:

(a) Last recently used (b) Least Recently Used

(c) Both a and b (d) Least Rarely Used ( )

32. The performance of page replacement algorithm depends on the:

(a) Page trace

(b) Program behaviour

(c) Both a and b

(d) Neither a nor b ( )

33. Broad call is :

(a) Write operation (b) Read Operation

(c) Both a and b (d) Neither a nor b ( )

34. For a reservation table with n columns, the maximum forbidden latency (m):

(a) $M \leq n$ (b) $n \leq n-1$

(c) $M \geq n$ (d) $n \geq n-1$ ( )

35. Intrinsic parallel computer are those that execute program in:

(a) SIMD mode only

(b) MIMD Mode only

(c) SIMD and MIMD modes

(d) None of the above ( )

36. .....is a shared memory system in which the access time varies with the location of the memory word.

(a) UMA

(b) COMA

(c) NUMA

(d) All of the above ( )

37. The topology of an interconnection network can be:

(a) Static

(b) Dynamic

(c) Either a or b

(d) None of the above ( )

38. For inter PE data exchange network that is used be:

(a) Static (b) Dynamic

(c) Either a or b (d) None of the above ( )

39. .....networking are controlled by a global clock

(a) Synchronous (b) Asynchronous

(c) Both a and b (d) Neither a nor b ( )

40. The portion of the operating system kernel which handles the allocation and deallocation of main memory to executing processes is called:

(a) Memory Swapper

(b) Memory Manager

(c) Process Swapper

(d) Process Manager ( )

Answer Key

1. (a)	2. (b)	3. (b)	4. (d)	5. (b)	6. (c)	7. (d)	8. (a)	9. (a)	10. (a)
11. (b)	12. (c)	13. (a)	14. (b)	15. (c)	16. (b)	17. (a)	18. (a)	19. (c)	20. (b)
21. (d)	22. (c)	23. (b)	24. (a)	25. (b)	26. (c)	27. (c)	28. (b)	29. (d)	30. (b)
31. (b)	32. (c)	33. (b)	34. (a)	35. (c)	36. (c)	37. (c)	38. (b)	39. (a)	40. (d)

DESCRIPTIVE PART - II

Year 2007

Time allowed : 2 Hours ***Maximum Marks : 30***

Attempt any four questions out of the six. All questions carry 7½ marks each.

Q.1 Compare the relative four cache memory organization.

(a) Direct mapping

(b) Fully associative

(c) Set Associative

(d) Sector Mapping

Q.2 Describe static and dynamic connection networks.

Q.3 Describe :

(i) Generations of electronic computers.

(ii) Elements of moderns computer

Q.4 Explain instruction set architecture in RISC and CISC processor.

Q.5 Explain Omega Network and Crossbar Network in detail.

Q.6 Describe the following terms associated with program partitioning and scheduling:
(a) Grain Sizes and latency
(b) Grain packing and scheduling

OBJECTIVE PART- I

Year - 2006

Time allowed : One Hour *Maximum Marks : 20*

The question paper contains 40 multiple choice questions with four choices and student will have to pick the correct one. (Each carrying ½ marks.).

1. Personal computer were appeared in:

   (a) 1st generation

   (b) 2nd generation

   (c) 4th generation

   (d) 5th generation ( )

2. Full form of MPP is:

   (a) Massively Pipeline Processing

   (b) Master Parallel Processor

   (c) Massive Parallel Processing

   (d) Master Pipeline Processor ( )

3. In UMA multiprocessor model, all the processors have unequal access time to all memory words:

   (a) True

   (b) False ( )

4. The number of edges incident on a node is called:

(a) Node degree (b) Node diameter

(c) Network degree (d) Network diameter ( )

5. Harold stone (1971) introduced special permutation function that was:

(a) Multicast (b) Perfect Shuffle

(c) Broadcast (d) Routing ( )

6. Switching complexity of multistage network is:

(a) O ($\log_k$ n) (b) O (ω)

(c) O (n $\log_k$ n) (d) O (n) ( )

7. The finest level of pipelining is:

(a) Macropipelining

(b) Micropipelining

(c) Both a and b

(d) Neither a nor b ( )

8. Prior to 1945 computers were made up of:

(a) Mechanical and electronic (b) Mechanical and electron mechanical

(c) Electronic and electron mechanical (d) All of the above ( )

9. .....computing is achieved through the use of an array or processing elements synchronized by the same controller:

(a) MIMD (b) SIMD

(c) 13 (d) None of the above ( )

10. Barrel shiffer is a:

(a) Static connection network

(b) Dynamic connection network

(c) Storage device

(d) Switching device ( )

11. A greedy cycle must be:

(a) A simple cycle

(b) Each state appears only once

(c) Average latency must be greater than those of other simple cycles

(a) Both i and ii are true (b) Both i and iii

(c) Both ii and iii (d) All three are true ( )

12. Which is the valid vector access memory scheme?

(a) C-Access memory organization

(b) Asynchronous

(c) Synchronous memory organization

(d) D-Access memory organization ( )

13. The full form of PRAM is:

(a) Parallel Random Access Machine

(b) Parallel Remote Access Machine

(c) Powerful Random Access Memory

(d) Partial Random Access Memory ( )

14. .....is a measure of the amount of computation involved in a software process:

(a) Grain size (b) Latency

(c) Bisection width (d) Network diameter ( )

15. Which of the most expensive dynamic connection network?

(a) Digital buses (b) Multistage

(c) Crossbar (d) Can't say ( )

16. The accumulated rate of all state utilization determines:

(a) Pipeline throughout (b) Pipeline efficiency

(c) Bounds on MAL (d) Delay Speed ( )

17. Processors that use multiphase clocks with a muck increase clock rate ranging from 100 to 500 MHz are:

(a) VLIW (b) RISC

(c) Memory interleaving (d) Super view ( )

18. .....is a process of moving blocks of information between the levels of memory hierarchy:

(a) Memory swapping

(b) Memory allocation

(c) Memory interleaving

(d) Memory scheduling ( )

19. Which is not a valid data routing functions?

(a) Permutation

(b) Perfect shuffle and exchange

(c) Broadband

(d) Multicast ( )

20. In binary tree network the bisection width would be:

(a) 1

(b) 2

(c) N/2

(d) $\{N/2\}^2$ ( )

21. The T3D is a :

(a) SIMD machine

(b) MIMD machine

(c) Both a and b

(d) None of the above ( )

22. The typical clock rate of today's CISC processor ranges from:

(a) 1 to 40 MHz

(b) 20 to 33 MHz

(c) 33 to 50 MHz

(d) All of the above ( )

23. TLB is used is:

(a) Paging (b) Segmentation

(c) Both a and b (d) None of the above ( )

24. In shared cache approach:

(a) Private caches are allowed

(b) Shared caches are allowed

(c) (i) is true

(d) None is true ( )

25. The effective bandwidth available to each processor is inversely:

(a) Number of I/O devices

(b) Number of processors

(c) Types of I/O devices

(d) Types of processors ( )

26. The main objective of scheduling evnets in a pipeline is:

(a) to obtain shortest latency between initiations without causing cohesion

(b) to obtain highest latency between initiations without causing collisions

(c) To obtain shortest latency between initiations without causing collisions

(d) All of the above ( )

27. In future Bus + standards, the 64 bit address lines are multiplexed with:

(a) Lower order 64 - bit data lines

(b) High order 64-bit data lines

(c) Lower order 32 bit data lines

(d) Any one ( )

28. The time in cycles required between the issuing of two adjacent instruction is:

(a) Instruction issue rate

(b) Instruction pipeline cycle

(c) Instruction operations latency

(d) Instruction issue latency ( )

29. .....refers to the process in which a resident page in main memory is repaced by a new page transferred from the disk

(a) Page allocation (b) page replacement

(c) both a and b (d) Neither a nor b ( )

30. To find out cache performance, we can use:

(a) Program trace driven simulation (b) Greedy cycles

(c) Hit ration (d) Hit ration ( )

31. If the number of links is 2NB, then this would be which kind of network:

(a) Illiac mesh (b) 2D Mesh

(c) Both a and b (d) None of the above ( )

32. .....techniques were introduced for prefect instructions in order to overlap I/E operations:

(a) Sequential (b) Look ahead

(c) Both a and b (d) None of the above ( )

33. .....uses high order bits as the module address and low order bits as the word address within each module:

(a) Low order interleaving (b) High order interleaving

(c) Low order interlacing (d) High order interlacing ( )

34. Printed circuit on which many connectors are used to plus in functional boards?

(a) I/O Buses (b) Hierarchical Buses

(c) Cache (d) Backplane Buses ( )

35. .....is an operation that fetches the non zero elements of sparse vector from the memory using indicates:

(a) Masking (b) Gather

(c) Scatter (d) Reduction ( )

36. The number of clock cycles between two initiations of a pipeline is:

(a) latency cycle (b) Gather

(c) Scatter (d) Evaluation analysis ( )

37. .....consist of an address transfer followed by a block of I or more data to 1 or more contiguous addresses:

(a) Address only transfer (b) Packet data transfer

(c) Evaluation cycle (d) All of the above ( )

38. Three dimensions of locality property are:

(a) Temporal, parallel and sequential

(b) Temporal, spatial and sequential

(c) Spatial, parallel and sequential

(d) None of the above ( )

39. The motorola MC 68040 is a :

(a) 8 Hm MOS Microprocessor

(b) .7 Hm CMOS Microprocessor

(c) .8 Hm HCMOS Microprocessor

(d) .7 Hm HCMOS Microprocessor ( )

40. Which is the example of blocking network?

(a) Baseline (b) Omega

(c) Delta (d) All of the above ( )

Answer Key

1. (c)	2. (c)	3. (b)	4. (a)	5. (b)	6. (c)	7. (b)	8. (b)	9. (c)	10. (a)
11. (a)	12. (b)	13. (a)	14. (a)	15. (c)	16. (a)	17. (c)	18. (a)	19. (c)	20. (c)
21. (c)	22. (c)	23. (c)	24. (c)	25. (b)	26. (d)	27. (d)	28. (d)	29. (b)	30. (c)
31. (b)	32. (c)	33. (b)	34. (a)	35. (a)	36. (b)	37. (d)	38. (b)	39. (c)	40. (d)

DESCRIPTIVE PART - II

Year 2006

Time allowed : 2 Hours ***Maximum Marks : 30***

Attempt any four questions out of the six. All questions carry 7½ marks each.

Q.1 What do you understand by shared memory multiprocessor and distributed memory multi computers ? Explain different models of shared memory multiprocessor.

Q.2 Explain the following terms associated with program partitioning and scheduling:
(a) Grain sizes and latency
(b) Grain packing and scheduling

Q.3 Explain all the factors on which the performance of interconnected network depends. Discuss the following dynamic connection networks.
(a) Digital buses
(b) Omega network

Q.4 Describe:
(a) Locality of reference
(b) Write back caches
(c) Write through caches

Q.5 Explain different page replacement policies with suitable example.

Q.6 What do you mean by vector processing? Explain different types of vector instructions with example.

Key Terms:

A

Access Time	Time required to place read/write heads of the disk over a particular track & sector. Rotational delay and seek time should also be considered.
Accumulator	CPU register that has the outcome of operations and occasionally the operands
Address Bus	System bus used to move addresses in RAM or I/O device
ALU	element of the CPU that does arithmetic and logical operations
ASCII (American Standard Code for Information Interchange)	A 7-bit standard character set that signify characters inside the computer.
ASRAM (Asynchronous RAM)	Static RAM is the one for transferring data without using the system clock.
Assembler	A system program that interpret a mnemonic assembly language to low level language.
Associative Memory	Memory whose location are recognized by their contents, rather than their position

B

Binary Operator	An operator that perform on two operands.
Bit (Binary Digit)	A single memory unit that has a single binary value (0 or 1)
Boolean Algebra	Mathematics laws applied by the processor to do logical and shift operations.
Buffer	Memory locations used to hold input or output data. It is required to balance difference in speed amid the CPU and the I/O devices.
Bus	Communication path consisting of a group of lines that carry signals, addresses, or data amid PC's elements. A bus can be used by all computer elements.
Byte	Memory unit that embrace 8 bits.

C

Cache	A small, fast memory - perform like a buffer. It is used to improve performance of CPU.
Chipset	A collection of typical PC functions pooled onto one or more integrated circuit.
Clock	Square wave with equal intervals. Used to harmonize CPU process. Events typically happen at rising or falling rim of the clock.
Combinational (combinatorial) Circuit	Logic circuit who's yield is a function of its input only at any specified time. There is no storage capacity of preceding contents of the circuit.
COMA	Cache-only memory architecture
Control Bus	System bus for transferring control signals among processor and other apparatus.
Control Unit	Part of the CPU accountable for calculating and coordinate computer functions.
CPU (Central Processing Unit)	It is accountable for performing instructions and controlling all other components.
Computer Architecture	the trait of a computer as noticed by the machine language Programmer which facilitate machine language programmer to write functionally correct, time autonomous programs.
Computer Organization	hardware arrangement surrounding the major operational units, data paths, and control.

D

Data Bus	System bus for transferring data.
Decoder	Combinational circuit for transferring input signal combination on numerous input lines into one specific 2^n-output lines.

Distributed Memory	Physical memory that is alienated into module every allocated to a processor in a multiprocessor organization.
DMA (Direct Memory Access)	I/O method that permit direct data swap between memory and I/O devices without holding the processor time. CPU only begins the I/O request and is interrupted after the transfer is complete.
DRAM (Dynamic RAM)	RAM put into practice using capacitors and that requires to be sporadically re-energized

E

EEPROM (Electronically Erasable Programmable Read-Only Memory)	usually used in BIOS chip and can be reorganized with a procedure known as **flashing** using dedicated software.
Error-Correcting Code	Code used for sending/receiving signals or characters used to automatically correct errors.
Error-Detecting Code	Code used for sending/receiving signals or characters used to automatically detect errors.
Exclusive-OR Gate (Function)	The logic - produce logical value "True" if both input values are dissimilar else produce "False".

F

Fetch Cycle	It is used for obtaining the instruction to be carried out from memory.
Fixed-Point Representation System	Representation of Real number in which the radix (decimal for radix 10) is kept in a fixed place.
Flip-Flop	A memory unit that include one binary value and in which the output signify the current state. The next state depends on current state and the input.
Floating-Point Representation System	Real number system in which the number is symbolize as two distinct parts- mantissa and exponent.

G

Gate	Combinational circuit component that make an output that look like simple Boolean function (And, OR, or NOT) of the

	functional input.
GB (Gigabyte)	= 1, 073,741, 824 bytes ≈1 Billion bytes

H

Hexadecimal Numbers	A base-16 number system that characterize 16 values (0 to 9 and A to F). usually signify memory addresses or data.
Hit Ratio	A measure of cache efficiency = (cache hits / cache misses)
Hz (Hertz)	The number of clock cycles per second. by and large specified in KHz (Kilohertz) or MHz (Megahertz).

I

IC (Integrated Circuit / Chip)	A hardware part generally prepared of silicon that hosts dozens to millions of transistors on a tiny region.
Instruction Format	Instruction outline that break up instruction to fields related to element of instruction (opcode, operands,)
Instruction Set	Total collection of instructions used by a machine.
Interrupt	An exception that arrives from outside the processor.
Interrupt Handler	A software program part that is run when an interrupt happens.
ISA (Instruction Set Architecture)	An conceptual medium between the hardware and the software of a device that include essential information to write accurate machine-language program. It comprise the requirement of commands, registers, memory size, instruction, ...etc.

K

K (Kilo)	$2^{10} = 1024$

L

L1 (Level 1) Cache	Cache situated contiguous to the processor. That is Primary cache.
L2 (Level 2) Cache	Cache positioned outside the processor. Known as secondary cache.

LAN (Local Area Network)	Network link that transmit data in a small geographic region, classically within the same building.
Latency	Wait or delay time(milliseconds).
Link Editor (Linker)	A system program that merges separately integrate machine language program and determine indeterminate labels. The consequential code is in executable code form.
Local Variable	A variable is defined and accessed in a particular unit of a program only.
Locality (of Reference) Principle	propensity of a program to access the *same* set of memory locations continually over small phase of time.
LRU (Least Recently Used) Scheme	A substitute method in which the new preferred block replaces the block that has been idle the longest time.

M

M (Mega)	2^{20} = 1,048,576
Mantissa	The part of a floating point number which, when multiply by its base raised to the power of its exponent, provide its value.
MAR (Memory address Register)	A CPU registers for keeping address of memory location being accessed.
Microinstruction	Low-level control instruction in which machine instruction is used to produce control signals.
Micro-operation	Basic CPU operation, carried out for the period of one clock cycle.
Microprocessor	Integrated circuits making the heart of the PC that include ALU, general and special registers, and Control units.
Micro program	Microinstruction sequence.
MIMD (Multiple Instruction stream, Multiple-Data stream)	The categorization under Flynn's nomenclature of a parallel processor where many functional parts carry out different function on different data.
MIPS (Million Instruction Per Second)	Determine execution speed. MIPS = Number of instructions in a program / (program execution time x 10^6)

MISD	Multiple instruction single data stream
Miss Rate	Portion of memory access not found in cache.
Motherboard	A large printed-circuit board used to host PC components
Multiprocessor	Computer having more than one processor with common main memory and single address room.
Multiprogramming	Programming mode that permit two or more programs to execute interleaved by a single CPU.

N

Nonvolatile memory	Memory whose data keeps integral even when the power is turned off.
NUMA	Non uniform memory access

O

Opcode (Operation Code)	Component of an instruction that indicate the operation and format of an instruction.
Operand	Entity on which an operation is carry out. piece of an instruction.
Operating System	System software to control program execution, assign and deal with resources, program tasks, control I/O operations, and manage data.

P

Page	A fixed length memory blocks that has virtual address and is swap as a entity amid two memory types (RAM & cache or RAM & secondary memory).
Page Fault	A condition that takes place when referencing a memory word that is not in RAM. It originates interrupt & needs loading the page ongoing the preferred word before the program can go on.
Page Frame	A block in RAM that can keep a page.

Parity Bit	An extra bit attached to a word and basis for sum of all digits to be either odd or even, depending on the type of parity (odd or even parity).
Peer-to-Peer Network	Two or more computers directly linked and directly share the data and hardware resources.
Pipeline	The procedure employed to begin one function in every cycle without waiting for the final outcome to be created, or completion of formerly commenced functions.
PRAM	Parallel random access machine

R

Radix (Base)	Representation of Number system.
Register	High-speed memory constituent exist in in the CPU used to keep data.

S

SCSI (Small Computer System Interface)	A bus used as a standard for I/O devices.
Seek Time	Time required for the head actuator to travel the read/write head from one track to the next.
Segmentation	Variable-size address mapping method in which an address is alienated into two parts: a part number and part offset.
Sequential Circuit	Logic circuit in which the next state is a function of both the current state and the input. It works as a memory element.
Sign-Magnitude Representation	Number representation used to represent binary integers. The leftmost bit is used to represent the sign (1 for negative, 0 for positive). rest bits keep the magnitude of the number.
SIMD (Single-Instruction Stream / Single-Data Stream)	Multiprocessor architecture that can do a single function on multiple set of data.
SIMD (Single-Instruction	The categorization under Flynn's nomenclature for a parallel

stream, Multiple-Data stream) (Or "data parallel")	processor where many processing part do the same action on different data. There is often a central controller that broadcasts the instruction stream to all the processing elements.
SIMM (Single-Inline Memory Module)	Memory unit made up of DRAM chip in special packaging. Soldered on a tiny circuit board with 30- or 72- edge connector.
SISD (Single-Inline, Single-Data Stream)	Computer organization in Flynn's classification that refers to the conservative processor.
Snooping Cache Memory	technique for retain cache coherency in which all cache controllers scrutinize the bus to decide whether or not they have the preferred block.
Spatial Locality	Locality principle that states that data referencing be apt to reference close by addresses.
SRAM (Static RAM)	RAM put into practice with flip-flops. Data keeps as long as the power is on. No periodic revitalizing is required.
Stack	A list that is efforts on LIFO (Last-In First-Out) basis.
Sum-of-Product	A logical expression merge AND terms (Product) and then applies the OR operator (Sum) on them.
Superscalar Pipelining	A system that copies the internal computer components to allow multiple instructions to be run in every pipeline stage.
Superscalar Processor	An advanced pipelining modus operandi in which more than one instruction can execute during one clock cycle, each on a different pipeline stage.
Synchronous Timing	Timing practice in which incidence of events on a bus are given by the clock.
System Bus	A bus used to be linked major computer components.

T

Tag	A field in a table having address information to discover a memory block in which a particular word is found.
TB (Terabytes)	= 1, 099,511, 627, 776 bytes ≈1 TB
TLB (Translation Lookaside buffer	Used in virtual memory systems. A cache that keeps track of lately used address mapping to circumvent an access to the page table. It lists the physical address page number related with

	every virtual address page number.
Transistor	Electronic circuit that holds electrical voltage representing one bit.
Truth table	Table showing logic task by listing all potential input combinations and their subsequent output values.
Throughput	A measure of how many programs can be executed per second

U

Unary Operator	An operator that perform on one operand only
Underflow	A condition that can take place when the outcome of a floating-point function would be lesser in scale (closer to zero, either positive or negative) than the smallest quantity characterizeable. Underflow is in fact (negative) overflow of the exponent of the floating-point quantity. It happens when a negative exponent is too great to be characterized. That means the number is too small to be represented.
UMA	Uniform memory access

V

Virtual Address	A memory location accessed in a system by an application program with virtual memory such that intervening hardware and/or software maps the virtual address to real (physical) memory.
Virtual Memory	Address space that can be seen as addressable main memory by the user. They are plotted by the processor into physical address space. Usually the virtual address space is bigger than the physical address space.
Volatile Memory	Memory that lose its contents when the power is off. Example: RAM.

W

Write Back	A cache structural design in which data is only written to main memory when it is enforced out of the cache. Contrary to write-through.
Write Through	A cache structural design in which data is written to main memory at the similar time as it is cached.

Websites:

- http://williamstallings.com/COA5e.html
- http://iiusatech.com/murdocca/CAO/
- http://courses.soe.ucsc.edu/courses/cmpe202
- http://www.randelshofer.ch/fhw/gri/float.html#chapterfloatapplet
- http://courses.soe.ucsc.edu/courses/cmpe110
- http://booksite.mkp.com/9780123838728/
- http://inst.eecs.berkeley.edu/~cs152/sp12/
- http://www.randelshofer.ch/fhw/gri/float.html
- http://www.britannica.com/EBchecked/topic/163278/digital-computer
- http://williamstallings.com/COA/COA7e.html
- http://csg.csail.mit.edu/6.823/lecnotes.html
- http://www.cs.berkeley.edu/~pattrsn/252S01/
- http://gs.fanshawec.ca/tlc/math270/
- http://courses.cs.vt.edu/~csonline/NumberSystems/Lessons/BinaryNumbers/index.html

- http://www.math.grin.edu/~stone/courses/fundamentals/IEEE-reals.html
- http://www.randelshofer.ch/fhw/gri/doubleapplet.html
- http://www.intel.com/products/processor (for Intel Itanium Processor)
- http://www.ibm.com/servers/eserver/pserieslhardware/whitepapers/power/ppc - arch.html
- http://www . i bm .com! servers/ eserver/pserics/hardware/wh itepapers/power/ppc arch 2.html

Bibliography

- Thomas C Bartee "Computer architecture and logic design" TMH
- Kai Hwang "Advanced computer architecture: Parallelism, scalability, programability", TMH
- Hamacher, Vranesic, and Zaki "Computer organization" TMH
- Hayes "Computer architecture and organization", THH

1. Book Name : Computer Systems Design And Architecture

Edition: 2/e

ISBN : 9788177584837

Author : Vincent P. Heuring,Harry F. Jordan,T.G Venkatesh

2. Book Name : Computer Architecture: Concepts And Evolution

ISBN : 9788131726143

Author : Gerrit A. Blaauw, Frederick P. Brooks

Edition : 1/e

3. Book Name : Computer Systems Organization & Architecture

ISBN : 9788177587678

Author : John D. Carpinelli

Edition : 1/e

4. Book Name : Essentials Of Computer Architecture

ISBN : 9788177584431

Author : Douglas E. Comer

Edition : 1/e

5. Book Name : Principles Of Computer Organization And Assembly Language

ISBN : 9788131721711

Author : Patrick Juola

Edition : 1/e

6. Book Name : Computer System Architecture

ISBN : 9788131700709

Author : M. Morris Mano

Edition : 3/e

7. Book Name : Computer Organization And Architecture

ISBN : 9788131732458

Author : William Stallings

Edition : 8/e

8. Book Name : Computer Architecture: A Quantitative Approach,

Author : John L. Hennessy , David A. Patterson

Edition :4th Edition

9. Book Name : Parallel Computer Architecture: A Hardware/Software Approach

Author : David Culler and J.P. Singh with Anoop Gupta

10. Book Name : Digital Design And Computer Organisation

ISBN : 978-81-318-0345-5

Author : D. Nasib S. Gill, J.B. Dixit

Edition : 1/e

11. Book Name : Structured Computer Organization (5th edition)

Author : Andrew S. Tannenbaum, Prentice Hall

12. Book Name : Computer Organization and Architecture: Designing for Performance

Edition:7th Ed

Author : William Stallings, Prentice-Hall.

13. D.P. Siewiorek, C.G. Bell, A. Newell, Computer Structures: Principles and Examples, McGraw-Hill Advanced Computer Science Series, 1982.
14. The SPARC Architecture Manual, Version 9, David L. Weaver, Tom Germond, Editors, Prentice Hall 1994.
15. W. Stallings,Computer Organization and Architecture, MacMillan Publishing Company, 1993.
16. G. Radin, "The 801 Minicomputer", IBM T.J.Watson Research Center, Report RC 9125, November 11, 1981, also in SIGARCH Computer Architecture News 10, No.2, p.39-47, March 1982.
17. D.A. Patterson, C.H.Sequin, "A VLSI RISC", *IEEE Computer Magazine*, September 1982.
18. J. L. Hennessy, "VLSI Processor Architecture", *IEEE Transactions on Computers*, Vol. C-33, No.12, December 1984.
19. M. E. Hopkins, "A Perspective on the 801 / Reduced Instruction Set Computer", IBM Systems Journal, Vol. 26, No.1, 1987.
20. book by William Stalings, "Computer Organization and Architec*ture*", MacMillan Publishing Company, 1993.
21. book by David A. Patterson and John L. Hennessy,"Computer Organization and Design: The Hardware / Software Interface", Morgan Kaufmann Publishers, 1994.
22. Kai Hwang, Faye A. Briggs, "Computer Architecture and Parallel Processing"

McGrawhill international Edition

23. Kai Hwang, "Advanced Computer Architecture", Tata McGrawhill Edition

14. V.Rajaraman, L Sivaram Murthy, "Parallel Computers", PID.
15. Kai Hwang, Scalable Parallel Computing
16. Harrold Stone, High performance computer Architceture
17. Richard Y. Kain , Advanced Computer Architecture