

Microprocessor and Computer Architecture

UE20CS252

4th Semester, Academic Year 2021-22

Date:

24/1/2022

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Week# 2
 1

Program Number:

Title of the Program

Write an ALP using ARM instruction set to check if a number stored in a register is even or odd. If even, store 00 in R0, else store FF in R0

I. ARM Assembly Code(1)

mov r1,#9

ands r2,r1,#1

beq even

mov r0,#0xff

b odd

even : mov r0,#0x00

odd : swi 0x011

II. Output Screen Shot (1)

The output should be verified for both even and odd numbers.

The left screenshot shows the 'RegistersView' window with the 'General Purpose' tab selected. The register values are displayed in hexadecimal. R0 is 00000000, R1 is 00000008, R2 is 00000000, R3 is 00000000, R4 is 00000000, R5 is 00000000, R6 is 00000000, R7 is 00000000, R8 is 00000000, R9 is 00000000, R10(sl) is 00000000, R11(fp) is 00000000, R12(ip) is 00000000, R13(sp) is 00011400, R14(lr) is 00000000, and R15(pc) is 00001018. The 'CodeView' window shows the assembly code for 'prog4.o'. The code is as follows:

```
00001000:E3A01008  mov r1,#8
00001004:E2112001  ands r2,r1,#1
00001008:0A000001  beq even
0000100C:E3A000FF  mov r0,#0xFF

00001010:EA000000  b odd
00001014:E3A00000  even : mov r0,#0x00
00001018:EF000011  odd : swi 0x011
```

The right screenshot shows the 'RegistersView' window with the 'General Purpose' tab selected. The register values are displayed in hexadecimal. R0 is 000000ff, R1 is 00000009, R2 is 00000001, R3 is 00000000, R4 is 00000000, R5 is 00000000, R6 is 00000000, R7 is 00000000, R8 is 00000000, R9 is 00000000, R10(sl) is 00000000, R11(fp) is 00000000, R12(ip) is 00000000, R13(sp) is 00011400, R14(lr) is 00000000, and R15(pc) is 00001018. The 'CodeView' window shows the assembly code for 'prog4.o'. The code is as follows:

```
00001000:E3A01009  mov r1,#9
00001004:E2112001  ANDS r2,r1,#1
00001008:0A000001  BEQ even
0000100C:E3A000FF  mov r0,#0xFF

00001010:EA000000  B odd
00001014:E3A00000  even : mov r0,#0x00
00001018:EF000011  odd : SWI 0x011
```

III. Output table (1)

Included in screenshots above

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Week# ____1____
____2____

Program Number:

Title of the Program

**Write an ALP to compare the value of R0
and R1, add if R0 = R1, else subtract**

1.ARM Assembly Code(1)

```
mov r0,#10
mov r1,#10
CMP r0,r1
BEQ equal
B notequal
notequal :
    SUB r3,r0,r1
    B end
equal :
    ADD r3,r0,r1
    B end
end : .end
```

2. Output Screen Shot (1)

Considering both equal and not equal:

The image displays two side-by-side screenshots of a debugger interface, showing the state of registers and code execution. Both screenshots show the same assembly code for a program named 'prog5.o'.

RegistersView (Left Screenshot):

- General Purpose: Floating
- Hexadecimal: 0000000a, 00000009, 00000000, 00000001, 00000000, 00000000, 00000000, 00000000, 00000000, 00000000, 00000000, 00000000, 00000000, 00000000, 00000000, 00000000
- Unsigned Decimal: 10, 9, 0, 1, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0
- Signed Decimal: 10, 9, 0, 1, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0
- R10(sl): 00000000
- R11(fp): 00000000
- R12(ip): 00000000
- R13(sp): 00011400
- R14(lr): 00000000
- R15(pc): 00001024

CodeView (Left Screenshot):

```
00001000:E3A0000A  mov r0,#10
00001004:E3A01009  mov r1,#9
00001008:E1500001  CMP r0,r1
0000100C:0A000002  BEQ equal
00001010:EAffFFFF  B notequal
00001014:E0403001  notequal : SUB r3,r0,r1
00001018:EA000001  B end
0000101C:E0803001  equal : ADD r3,r0,r1
00001020:EAffFFFF  B end
end : .end
```

RegistersView (Right Screenshot):

- General Purpose: Floating
- Hexadecimal: 0000000a, 0000000a, 00000000, 00000014, 00000000, 00000000, 00000000, 00000000, 00000000, 00000000, 00000000, 00000000, 00000000, 00000000, 00000000, 00000000
- Unsigned Decimal: 10, 10, 0, 14, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0
- Signed Decimal: 10, 10, 0, 14, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0
- R10(sl): 00000000
- R11(fp): 00000000
- R12(ip): 00000000
- R13(sp): 00011400
- R14(lr): 00000000
- R15(pc): 00001024

CodeView (Right Screenshot):

```
00001000:E3A0000A  mov r0,#10
00001004:E3A0100A  mov r1,#10
00001008:E1500001  CMP r0,r1
0000100C:0A000002  BEQ equal
00001010:EAffFFFF  B notequal
00001014:E0403001  notequal : SUB r3,r0,r1
00001018:EA000001  B end
0000101C:E0803001  equal : ADD r3,r0,r1
00001020:EAffFFFF  B end
end : .end
```

CPSR Register (Left Screenshot):

- Negative(N): 0
- Zero(Z): 0
- Carry(C): 1
- Overflow(V): 0
- IRQ Disable: 1
- FIQ Disable: 1
- Thumb(T): 0
- CPU Mode: System

CPSR Register (Right Screenshot):

- Negative(N): 0
- Zero(Z): 1
- Carry(C): 1
- Overflow(V): 0
- IRQ Disable: 1
- FIQ Disable: 1
- Thumb(T): 0
- CPU Mode: System

Disclaimer:

- The programs and output submitted is duly written, verified and executed by me.
- I have not copied from any of my peers nor from the external resource such as internet.
- If found plagiarized, I will abide with the disciplinary action of the University.

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