

Question-3

- ① LDR R1, [R2, #40] F D E M W
 ② ADD R2, R3, R3 F D E M W
 ③ ADD R1, R2, R2 F D E M W
 ④ STR R1, [R2, #20] F D E M W

~~without forwarding:~~

- a) ~~① & ② : Anti dependence on R2
 ② & ③ : true dependence on R2
 ② & ③ : true dependence on R1
 ③ & ④ : output dependence on R1
 ① & ④ : " " "
 ① & ③ : Output " " "~~

a) without forwarding.

- ① & ② : Anti dependence on R2
 ① & ③ : Output dependence on R1
 ① & ④ : true dependence on R1
 if no partitioning.
 ② & ③ : true dependence on R2
 ② & ④ : true dependence on R2
 ③ & ④ : true dependence on R1

1) Considering Separate I-cache & D-cache
 with fwding without:

① & ③

① ③

① ④ if no partition

② ③

② ④

③ ④

- c) ① ins
② ins
Nop (mem access)
③ ins
④ ins.

→ Question: 4

a) LDR F D E M W
 BEQ F D E M W
 ADD discarded → F D Not executed
 BEQ F D E M W
 STR F D E M W
 AND F D E M W

b) with delay: (Branch logic in EX stage)

LDR F D E M W
 BEQ F D E M W
 SAFE: INSTRUCTION.
 SAFE INSTRUCTION.
 BEQ F D E M W
 STR F D E M W
F D E M W