University of Moratuwa

Faculty of Engineering

Department of Electronic Telecommunication Engineering

High Frequency Amplifier

Group Members (Group 01)	
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Contents

Abstract

This report provides an in-depth exploration of the design process for a high-frequency amplifier dedicated to amplifying a sinusoidal wave within the frequency range of 20 kHz to 100 kHz.

The target output impedance for the amplifier is 8 Ω, and the design adheres to specific project guidelines that mandate the use of transistors, with a minimum requirement of three transistors. The primary objective is to achieve a high-power gain output while maintaining minimal distortion.

The report encompasses the following key stages in the development of the high-frequency amplifier:

- **Initial Calculations Using Small Signal Model:**
- **NI Multisim 14.2 Simulation**
- **PCB Design Using Altium Designer (22.9.1)**
- **Breadboard Implementation**
- **Enclosure Design Using SolidWorks 2023**
- **Comprehensive Data Sheet**

The step-by-step process outlined in this report demonstrates a systematic approach to designing and implementing a high-frequency amplifier. The utilization of Multisim simulation, PCB design, and 3D modeling contributes to the overall success of the project. The comprehensive data sheet serves as a valuable resource for future reference and dissemination of project findings.

1. Introduction & Functionality

1.1. Introduction

As frequency increases, the gain of a standard amplifier typically decreases. This is because the amplifier's transistors are not able to switch as quickly at higher frequencies. Additionally, the bandwidth of the amplifier limits the range of frequencies that can be amplified without distortion. High-frequency amplifiers are designed to overcome these limitations.

High frequency amplifier is a device used to amplify signals at higher frequencies with a high-power gain and no distortions. Finally, a speaker with a lower impedance receives the signal. The necessary actions were taken to reduce the distortions there as well.

1.2. Functionality

- This project aims to generate a distortion-free output for an input signal comprising a single-tone sine wave with a peak-to-peak amplitude of 0.1 V.

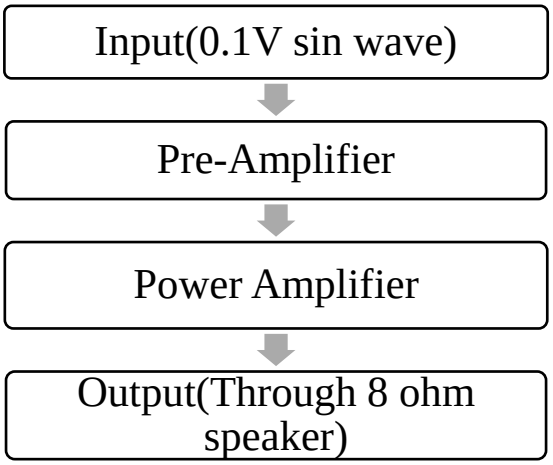
- This output should drive an 8-ohm speaker. For low input signal amplitudes, the signal power is also low, and 0.1 V is not enough to activate the speaker. Hence, the signal power and SNR must be enhanced. At low amplitudes, noise becomes more prominent.

- Therefore, the input sine wave amplitude should be amplified initially. This is accomplished using a voltage amplifier as a preamplification stage.

- After that, to obtain the power amplification, power amplifier is used.

2. System Architecture

2.1. Block Diagram



2.2. Stage 1 – Pre-Amplifier

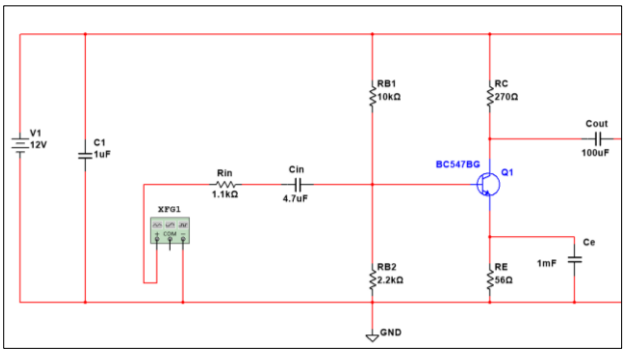


Figure 1: Stage 1 – Pre-Amplifier

2.2.1. Transistor configuration

Transistor configuration selection for voltage amplification is an important part of the design of a high frequency amplifier aimed at amplifying sinusoidal waves in the frequency range from 20 kHz to 100 kHz.

For voltage amplification, BJT transistors can be used in three different configurations: common collector, common emitter, and common base. Each configuration offers unique characteristics suitable for a particular application.

1. **Common Collector configuration**:

   The common collector configuration provides a voltage gain of approximately equal to one, which acts primarily as a buffer due to its active current gain. While this design ensures minimal voltage gain, it is effective in maintaining signal integrity.

2. **Common Base configuration:**

   A commonly used base configuration of equal current gain was not selected for the preamplification phase because it does not provide the desired power gain required for the project objectives

3. **Common Emitter configuration:**

   The conventional emitter configuration was chosen because of its significant power gain capability for the preamplification phase. Despite the low voltage gain compared to a normal collector, it provides high power, making it the ideal choice for driving the output signal to the headset

The typical emitter configuration is selected based on its ability to achieve the highest voltage with a BJT transistor for the preamplification phase. This design ensures a substantial increase in signal strength, so that the output signal is optimally delivered at 8 Ω of resistance.

2.2.2. DC Analysis

Q point selection

- Based on the datasheet of BC547 transistor, a quiescent current of 20 mA is selected to maximize the gain bandwidth product. ($I_{CQ} = 20\ mA$)
- To maintain the quiescent point near the mid-point we have chosen the quiescent point voltage as half of the supply voltage. ($V_{CEQ} = 6\ V$)

Calculation of R_C

- Using Kirchhoff's Current Law (KCL),

$$V_{CC} = I_C R_C + V_{CE} + V_E$$

- Since V_E is set to be less than 10% of V_{CC},

$$12\ V = 20\ mA * R_C + 6\ V + 1.2\ V$$

$$R_C = 240\ \Omega$$

Calculation of R_E

- Since I_B is a very small, it is negligible

$$I_C \approx I_E$$

- Using $V = I\ R$,

$$V_{CE} = I_E R_E,$$

$$1.2\ V = 20mA * R_E$$

$$R_E = 60\ \Omega$$

Input Side Considerations:

- Utilizing the Potential Divider Bias method,

$$V_B = V_{BE} + V_E$$

$$V_B = 0.7V + 1.2\ V$$

$$V_B = 1.9\ V$$

- Let $R_{B1} = 10\ K\Omega$. Then,

$$V_B = \frac{R_{B2}}{R_{B1} + R_{B2}} * V_{CC}$$

$$1.9V = \frac{R_{B2}}{10\ K\Omega + R_{B2}} * 12\ V$$

$$R_{B2} = 1.88\ k\Omega$$

2.2.3. AC Analysis:

Calculation of C_E

- For AC signal analysis, an emitter bypass capacitor is introduced to counteract negative feedback effects caused by the emitter degeneration resistor.
- To neglect emitter resistance in the AC signal, the capacitor impedance must be much lower than the emitter resistor.
- Since our given maximum frequency is 100 kHz and taking the minimum impedance of capacitor as 2 $m\Omega$ the minimum capacitor value is calculated as below.

$$X_E = \frac{1}{2\pi f * C_E}$$

$$2m\Omega = \frac{1}{2\pi * 100\ kHz * C_E}$$

$$C_E = 795.77\ \mu F$$

Calculation of coupling capacitors

Coupling capacitors are needed in the hybrid π model for BJT using small signal analysis to prevent distortion. For input and output coupling capacitors, specific values need to be determined based on the circuit requirements.

- For input, $Cin = 3\mu F$
- For output, $Cout = 100\mu F$

2.3. Stage 2- Power Amplifier

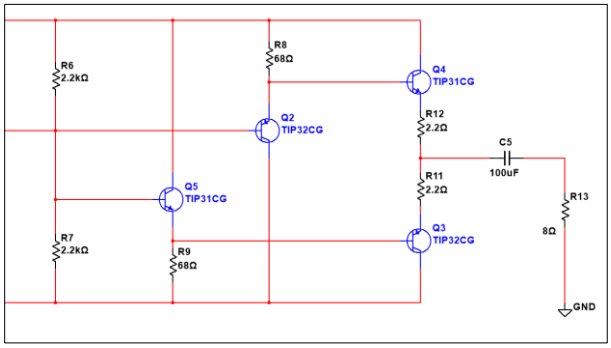


Figure 2: Stage 2- Power Amplifier

2.3.1. Class of the Amplifier

For the second stage, a transistor-based power amplifier is essential to generate the required output. Transistor-based power amplifiers are

categorized into several classes: Class A, Class B, Class AB, and Class C.

- **Class A**

  Class A amplifiers position the Q point almost in the middle, resulting in a continuous current flow through the transistor even without an input signal. However, this design leads to significant power loss, with theoretical efficiency capped at 50%. Moreover, the efficiency is contingent on the nature of the output (inductive or capacitive), making Class A unsuitable for our objectives.

- **Class B**

  Class B amplifiers place the Q point in the cutoff region, making them more power-efficient (theoretically up to 78.5%). Nevertheless, these amplifiers suffer from crossover distortion, a consequence of needing to forward-bias each transistor's base-emitter junctions. The biasing process utilizes a portion of the input voltage, introducing distortion into the output signal.

- **Class AB**

  Class AB amplifiers, operating at the edge of the cutoff and active regions, offer a compromise. The voltage necessary to forward bias the base-emitter junctions is already present, reducing reliance on the input signal for biasing and thereby eliminating crossover distortion.

Considering these factors, the decision is to utilize **Class AB** for power amplification. Initial forward biasing of the two junctions is necessary before introducing the input signal. Transistors, diodes, or resistors can achieve this, but the use of resistors may result in impedance imbalances. Opting for common collector transistors yields favorable outputs.

In addition to providing the initial forward bias for the two junctions, the transistor's buffer plays a crucial role in impedance matching when cascading two stages: the pre-amplifier and the power amplifier.

Our system model has been constructed with careful consideration of the outlined factors, ensuring a balanced approach to efficiency, distortion, and impedance matching.

3. Component Selection

3.1. Transistors

- **BC547**

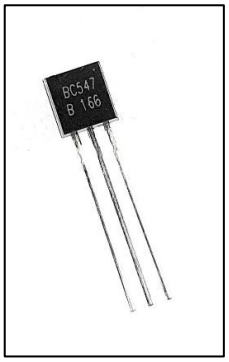


Figure 3: BC547 Transistor

The BC547 transistor emerges as the optimal choice for the Common Emitter amplifier in the voltage amplification stage of the high-frequency amplifier.

1. **High Transition Frequency:**

   The BC547 transistor is chosen for its advanced transition frequency, a vital element in excessive-frequency applications. This function guarantees green performance in amplifying indicators inside the detailed frequency range, contributing to the overall effectiveness of the amplifier.

2. **Stable Current Gain:**

   The BC547 transistor demonstrates excessive and stable cutting-edge benefit,

making it appropriate for packages wherein consistent amplification is critical. The stability of modern-day advantage regarding versions in collector modern and temperature ensures dependable performance throughout one of a kind operating condition**.**

3. **Relatively Fast Switching and Response Time:**

The BC547 is thought for its tremendously speedy switching and reaction times. This feature is effective in excessive-frequency applications, where a swift and correct reaction is vital for keeping sign integrity and minimizing distortion.

- **TIP31C & TIP32C**

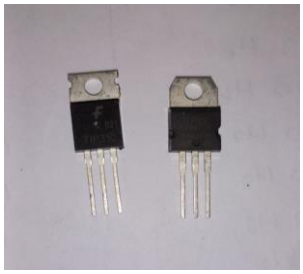


Figure 4: TIP31C and TIP32C Transistor

A substantial current flow through the transistors in the power amplification stage, necessitating power transistors capable of handling high currents. In our Multisim simulations, we observed a peak-to-peak voltage output of 2.9 V from the voltage amplifier.

Assuming no voltage drops in the signal, the output voltage signal should indeed have a peak-to-peak voltage of 2.9 V (or 1.45 V amplitude). Connecting this signal to an 8-ohm resistor would yield a maximum current of 181 mA. Consequently, a power transistor with a control capacity of 200 mA is required for safe operation. Furthermore, to achieve AB class operation, a complementary symmetry pair is necessary.

Considering the need for through-hole transistors, we have chosen the complementary symmetry pair TIP31 and TIP32. It is essential to note that these transistors offer a maximum collector current of 5 A, providing a comfortable margin for our application. This selection ensures that the transistors can handle the required currents while operating in a complementary manner for effective Class AB amplification.

3.2. Resistors

To ensure practicality in component values, certain adjustments were made based on the results of our computations. After implementing the circuit on a breadboard, it became apparent that ideal values could not be used due to considerations such as wire resistance. To maintain the Q point within the linear region in the output characteristic, the following modifications were made:

- **Practical values:**

$$R_C = 220\Omega$$

$$R_E = 68\,\Omega$$

- **Adjusted Values after Breadboard Implementation:**

$$R_E = 56\,\Omega$$

$$R_{B2} = 2.2\,\Omega$$

These changes were made to account for practical constraints and ensure the circuit operates within the desired linear range.

3.3. Capacitors

Since the capacitor value should be in practical manner, we need to modify the values of the input coupling capacitor and emitter bypass

capacitor while keeping the values of the other capacitors as same as calculated before.

$$C_E = 1\ mF$$

$$C_{in} = 4.7\ \mu F$$

$$C_{out} = 100 \mu F$$

4. PCB Design

The PCB layout has been specifically crafted to meet the demands of high-frequency applications while mitigating temperature increases. The orientation of adjacent current-carrying lines adopts an obtuse angle to minimize interference. Trace widths are determined based on maximum current considerations, with a focus on average temperature rises to facilitate efficient current flow.

A two-layer PCB design has been implemented to diminish high-frequency noise and ensure rapid signal grounding. Once the board design was finalized, we forwarded it to JLPCB to produce a high-quality PCB, aiming to minimize noise interference.

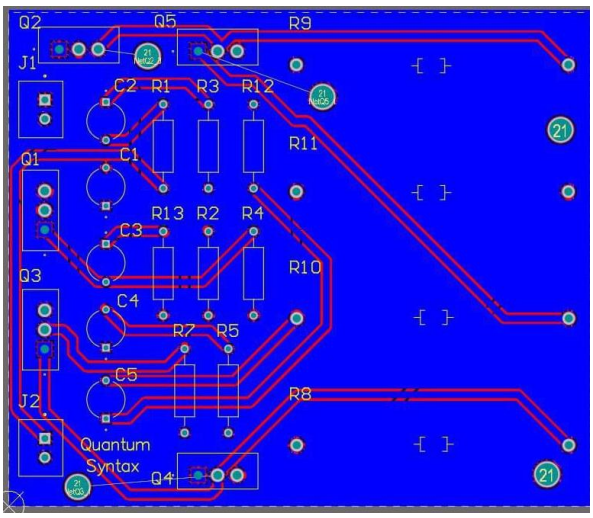


Figure 5: Bottom layer of PCB

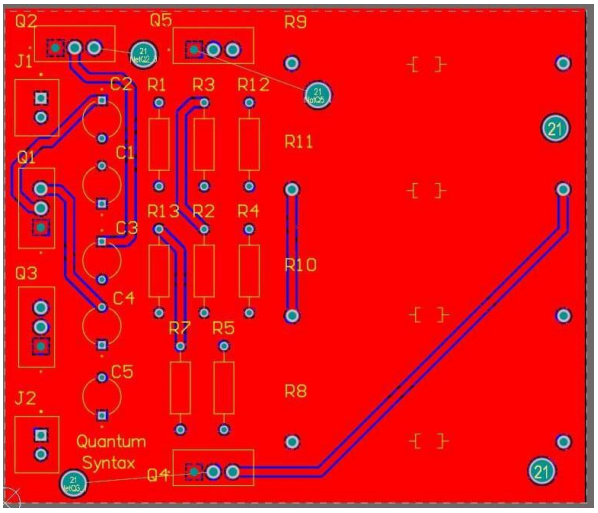


Figure 6: Top layer of PCB

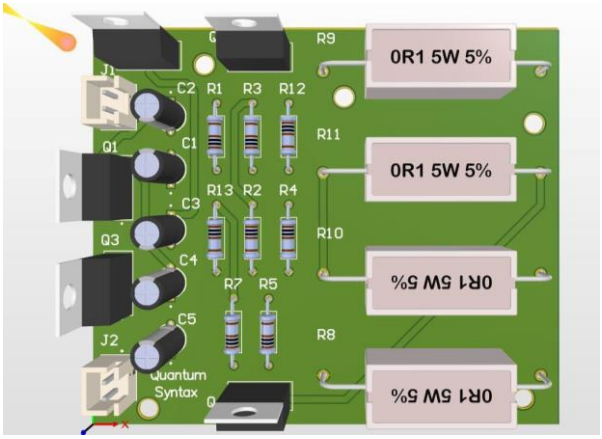


Figure 7: 3D view of the PCB

5. Enclosure design

The enclosure layout carefully considers the minimal dimensions of 127 x 97 x 44.44 mm^3 to place the PCB successfully. The wall thickness of three mm, the enclosure achieves a stability of strength and lightness. Thoughtful placement of vents, aligned with the power transistors on the PCB, enables the green to go with the flow of heated air, preventing energy transistors from overheating.

Furthermore, on the rear side, there is a DC Base Barrel Female Socket. In the front there are RCA port, and a two-way speaker

connector. These ports facilitate the linking of an audio jack for input signals, a 12V power supply jack, and a speaker for monitoring the device's output signal as sound. To simplify maintenance, both the PCB and the ports are connected to the lower section of the enclosure.

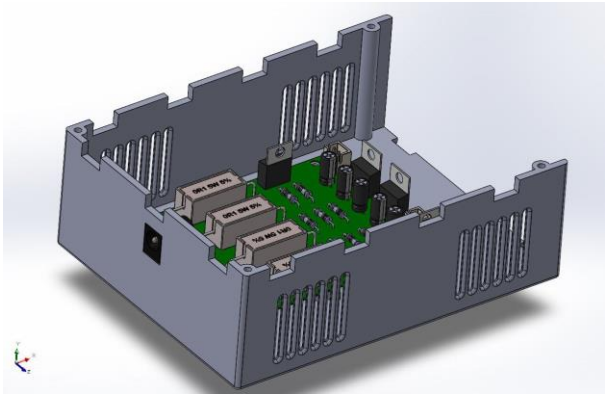


Figure 8: Bottom part

Figure 9: Full enclosure

6. Software Simulation and Hardware Testing

6.1. Multisim Simulation

The initial simulations conducted in Multisim unveiled a slight deviation of the output sine wave from the anticipated waveform. Notably, the power amplifier stage's output exhibited considerable distortion, a phenomenon also observed in the preamplifier output. This observation prompted the realization that the distortion issue was not exclusive to the power amplifier stage.

In response to this, we undertook modifications by adjusting the value of the emitter degeneration resistor to bring the transistor within its linear range, thereby causing a clipped output. Subsequently, we fine-tuned the input resistance to attain a precise sine wave output signal with minimal distortion.

Following these adjustments, Multisim simulations presented graphs illustrating the input signal (depicted in yellow) and the output signal (depicted in red), providing visual insights into the effects of the parameter changes.

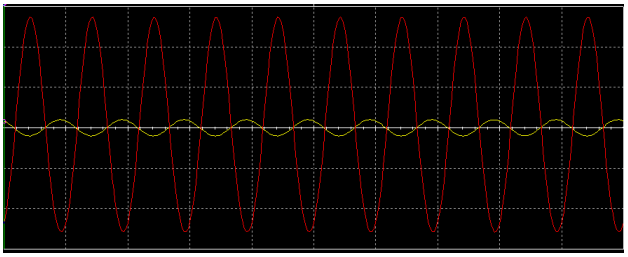


Figure 10: Multisim Result

Simulation Results

With load (8 ohm)

- Input Current (pk to pk) : (0.39 A)
- Input Voltage (pk to pk) : 0.1 V
- Output Voltage (pk to pk) : 1.556 V

Bandwidth The frequency response provides valuable information that can be used to determine bandwidth. This is referred to as the frequency range with a good gain. The range of frequencies for which the gain is more than $\frac{1}{\sqrt{2}}$ or the range of frequen cies for which the gain is more significant than -3 dB compared to the mid-frequency can be used to define bandwidth. The figure shows the bandwidth and frequency response.

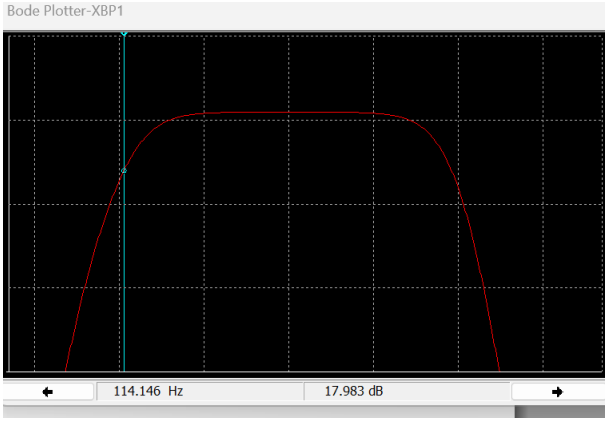


Figure 11: Bode Plot Simulation

6.2. Breadboard Implementation

Following the simulation, we translated the proposed design onto a breadboard. In this phase, we encountered minor distortions in the output, attributing them to the internal resistance of wires and the breadboard. Adjustments to the resistor values were made to alleviate these distortions and achieve the anticipated waveform.

Moreover, issues related to ground instability arose, prompting the introduction of a capacitor between the ground and the power line to address and resolve the problem.

To effectively manage thermal power, various techniques were employed. High-power rated resistors, specifically 2W and 5W for emitter followers and class AB amplifiers, were incorporated. Power transistors were strategically connected to heat sinks to efficiently disperse generated heat. Additionally, a considerable separation distance was maintained between high-power components to enhance ventilation and reduce surrounding warmth.

Component	Quantity
BC547 Transistor TIP31C Transistor TIP32C Transistor	1 2 2
2.2kΩ Resistors 10k ΩResistors 	3 1 1
220 ΩResistors 56 ΩResistors 1.2kΩ Resistors 68Ω 2W Power Resistors 2.2Ω 5W Power Resistors	1 1 2 2
1 F Capacitors 4.7 F Capacitors 100 F Capacitors 1 mF Capacitors	1 1 2 1
Heat sinks	4
Connectors	3

6.3. Measurements

Subsequently, we progressed to design the Printed Circuit Board (PCB) and conducted a comprehensive series of tests to assess its performance. Specifically, we transmitted various sinusoidal signals within the frequency range of 20 kHz to 100 kHz to identify potential output distortions. Following this, we performed experiments to measure the device parameters of the high-frequency amplifier, including input and output impedance, open-loop gain, closed-loop gain, and bandwidth, with a reference signal frequency of 20 kHz.

- **Input Impedance:**

Initially, the multimeter measured the current drawn from the source. After obtaining the current value, the input impedance was calculated by dividing the input voltage by it. The prototype circuit's input impedance value was determined to be 1.48 kΩ.

- **Output Impedance:**

The input of the high-frequency amplifier was short-circuited, and a multimeter measured the voltage across the output. The output impedance value was then calculated by dividing the measured voltage by the current flowing through the output, resulting in an output impedance measurement of 8.32 Ω for the prototype circuit.

- **Open Loop Gain:**

The open-loop gain, defined as the voltage gain without the load (speaker), was determined by connecting the input and output terminals to the oscilloscope. The ratio of input and output peak-to-peak voltage values was used to calculate the voltage gain. The obtained open loop gain for the prototype circuit was 24.3 (or 13.85 dB) for 50 kHz.

- **Closed Loop Gain:**

After connecting the speaker (with eight ohms impedance), the output peak-to-peak voltage was measured. Using the input peak-to-peak voltage, the closed-loop gain was determined. The closed loop gain for the prototype circuit was measured at 23.8(or 13.76 dB) for 50 kHz).

- **Bandwidth:**

The oscilloscope was utilized to determine the amplifier's bandwidth. Initial measurements were taken at a frequency of 20 kHz, and subsequent measurements were made at 10 kHz increments. The frequency producing an output voltage equal to the output at 330 kHz marked the bandwidth limit.

Bandwidth = (330-20) kHz = 310 kHz

7. Conclusion and future works

Given the nature of this high-frequency amplifier, there remains a slight possibility of output distortions. To further mitigate potential noise, an alternative could be the utilization of a constant current differential amplifier that employs transistors instead of a voltage amplifier.

Additionally, while the TIP 31 and TIP 32 power amplifier stage provides a relatively lower gain, there is an opportunity to enhance power gain by incorporating complementary symmetry power transistors with a Darlington pair. This approach would yield a higher-current output. However, the implementation of transistors with Darlington pairs is not pursued in this instance due to cost considerations.

8. Contribution of Group Members

Name	**Contribution**
Gamage S.B.P. (210178D)	PCB and Soldering
Mihiranga N.G.D. (210387D)	Initial prototype, Simulation, Overall project report
Morawakgoda M.K.I.G. (210391J)	Initial calculations, Data sheet preparation, Overall project report
Sirimanna N.T.W. (210610H)	Enclosure Design

Acknowledgment

The project's success hinged on various elements, and among them was the guidance and support received from numerous individuals involved in the project. Additionally, our appreciation goes out to everyone who played a role, no matter how small, in contributing to the accomplishment of this endeavor.

References

[1] DISCRETE SEMICONDUCTORS “2N2222; 2N2222A”. In : (1997).

[2]DISCRETE SEMICONDUCTORS ‘’BC107;BC1058;BC109’’. In : (1997)

[3]Mihai Albulet. RF power amplifiers. Vol. 2. SciTech Publishing , 2001

[4]Rosalfonso Bortoni , Rui Seara , et al.’’On the design and efficiency of class A, B, AB, G & H audio power ampifier output stages”. In: Journal of The Audio engineering Society 50.7/8 (2002), pp. 547 563.

[5]Paul Tobin. ‘’Operational Amplifier Characteristics”. In : PSpice for Circuit Theory and Electronic Devices. Springer,2007 pp.127 154

Appendix I -Data Sheet

Features

- Input Signal - Sinusoid with 0.1 V peak to peak Amplitude
- Supply Voltage - 12 V

Applications

- High frequency amplifier(for single tone sinusoid) which can drive a load impedance of 8 Ω.

Description

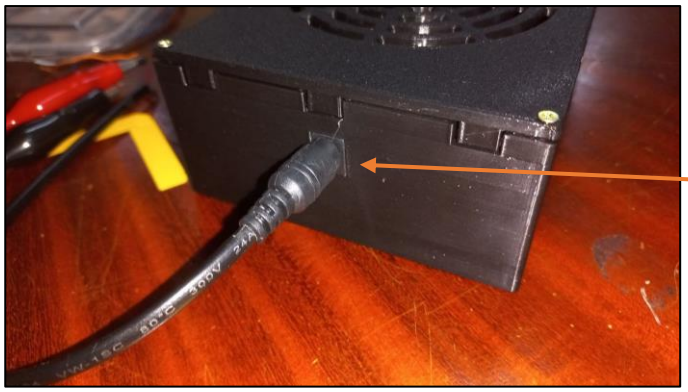
- Low noise output
- AB class solid state Amplifier

Electrical Characteristics

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
BW	Bandwidth	$R_L = 8\Omega$	20		330	kHz
A_{vo}	Open loop voltage gain	$R_L = \infty$		13.85		dB
A_v	Closed loop voltage gain	$R_L = 8\Omega$		13.76		dB
R_{in}	Input Impedance	$R_L = \infty$		1.48		kΩ
R_{out}	Output Impendence	$V_s = 0$		8.32		Ω
P_{out}	Output Power	$R_L = 8\Omega$	0.225	0.25	0.33	W
T_o	Operation Temperature	$R_L = 8\Omega$	25		32	^{o}C

Pinning


Quantum Synlab
On/Off switch
Signal Output
Signal Input


Power Input

Appendix II -Figures

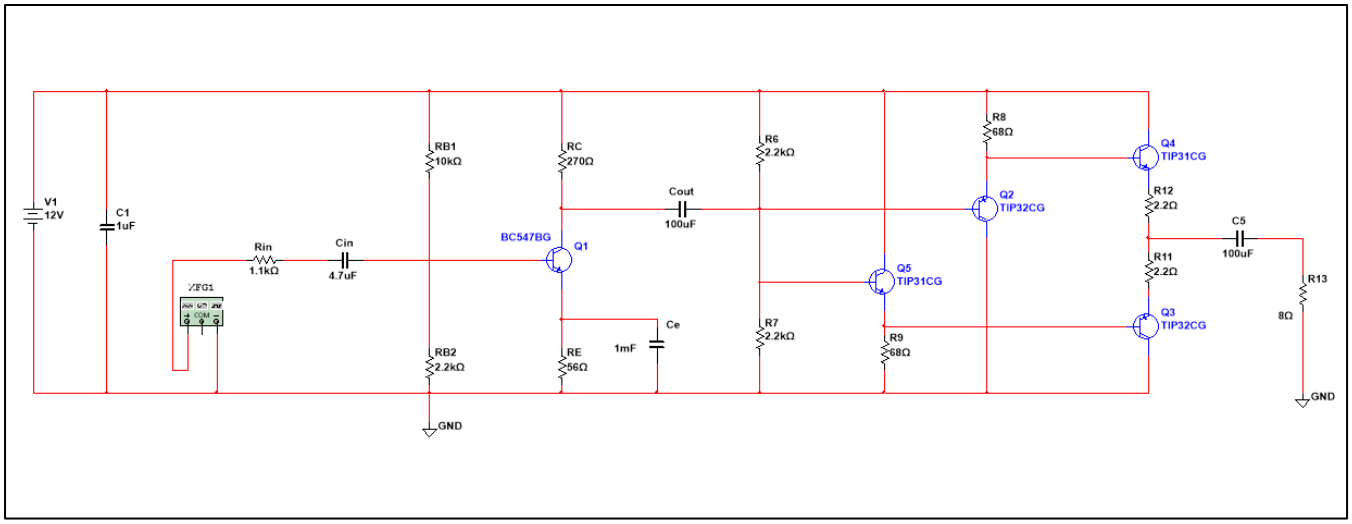


Figure 12: Circuit Diagram

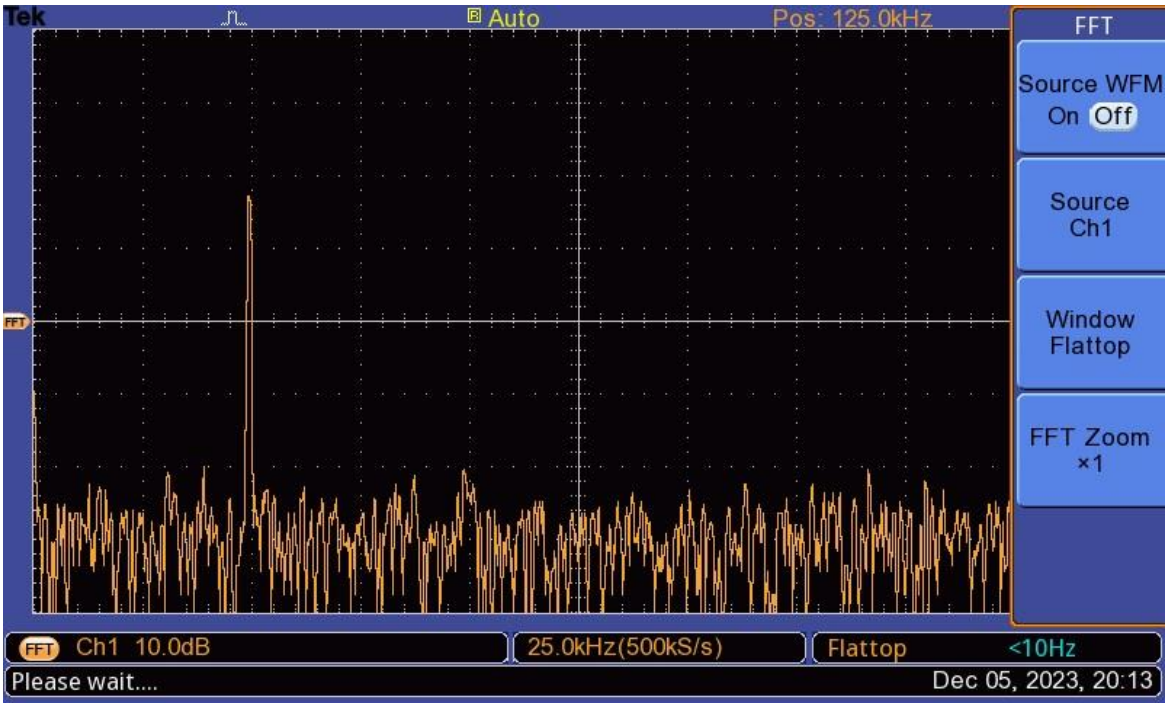
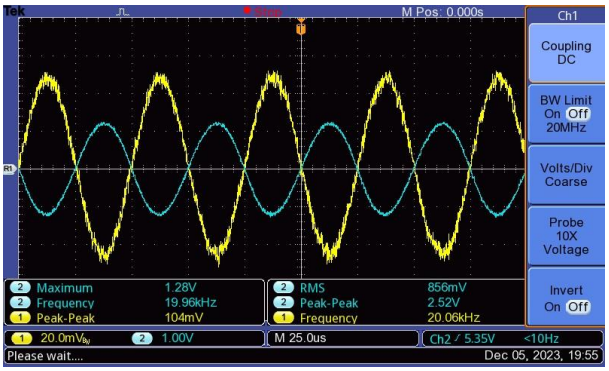
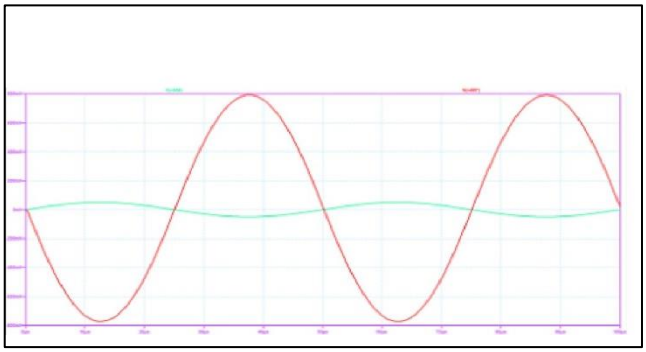
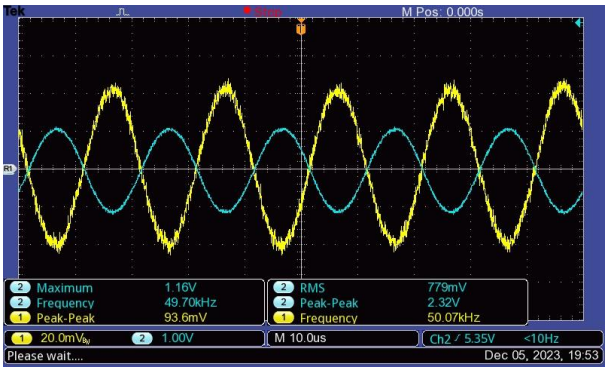


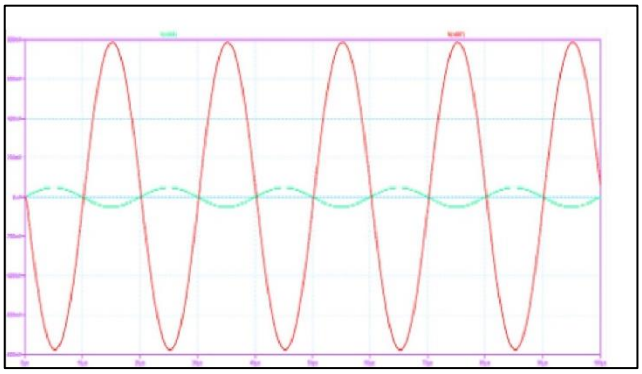
Figure 13: FFT plot



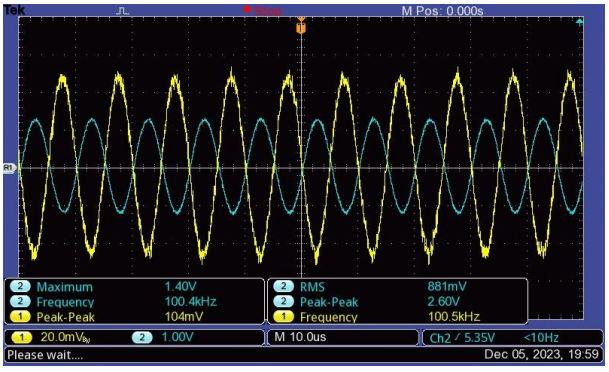


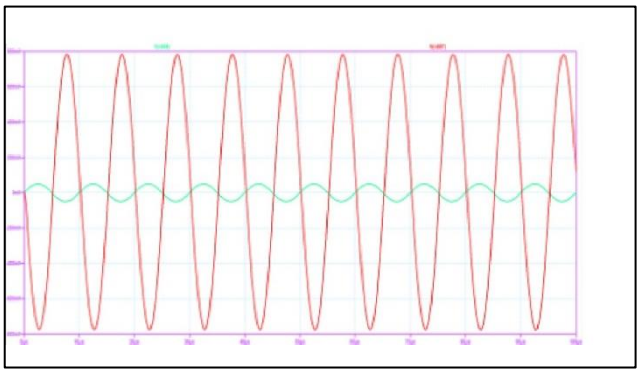
b)For 20kHz





b)For 50kHz





c)For 100kHz