

FINAL YEAR PROJECT

Final Project Report

Home Automation Using Power Line Communication



K.N.S.C. Kiriwaththuduwa

BSC-EE-2016-01-0091

Undergraduate, Sri Lanka Technological Campus

B.Sc. (Hons) in Electronics and Power Systems Engineering

A.M Harshana Miyuranga

BSC-EE-2016-01-0097

Undergraduate, Sri Lanka Technological Campus

B.Sc. (Hons) in Electronics and Power Systems Engineering

Dr. Udes Oruthota

Project Supervisor

Ms. Hinduja Durairaj

Project Co-Supervisor

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K.N.S.C. Kiriwaththuduwa

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The Final Project Report was submitted in partial fulfilment of the requirements for the

Degree of Bachelor of Science of Engineering

Supervised by

Dr. Udes Oruthota

Ms. Hinduja Durairaj (Co-supervisor)



School of Engineering

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Declaration

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K.N.S.C Kiriwaththuduwa

The above candidate has carried out final year project for the Bachelor of Science (Hons.) degree dissertation under my supervision.

.....

Date:

Dr. Udes Oruthota

.....

Date:

Ms. Hinduja Durairaj

Abstract

Home automation is a novel approach that is widespread through the advancement of the technology. It is also a costly approach provided that most of the components used in the systems are on upper cost margins. Their applications are based on network connections and require internet access for each component to be controlled. Homes which have the Wi-Fi facility cannot give the coverage to the entire premises and thus, it is not cost effective. Therefore, a power line communication scheme can be developed for home automation using existing electrical installations of a home. This will bear a low cost by using the existing wiring system and the walls are not damaged to use extra cable installations. No separate wires are needed for communication purposes, as the power lines themselves carry power as well as communication signals.

Power line communication has the benefit of reducing power and data loss since, power lines are well insulated to provide only negligible leakage between conductors and ground even in adverse weather conditions. Therefore, this will be better for home automation than existing systems. It is also possible to make the system more secure by using better encryption methods than the existing systems.

In this project, we developed a device, where a bit pattern is sent through the power line using a transmitter. When the receiver which is connected to anywhere in the power line identifies the relevant bit pattern, it energizes the relay and allows to get power from the plug base at the receiver. This method was developed to be controlled manually and also using a mobile application.

In the future our objective is to develop this product up to the industrial level so that it can contribute to the electronic industry in Sri Lanka.

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1 Introduction

Power line communications (PLC) reuse existing infrastructures (i.e. power lines) whose primary purpose is the delivery of AC (50 Hz or 60 Hz) or DC electric power, for the purpose of data communications. Hence, compared to the electric power ‘signal’, PLC uses high-frequency signals with frequency components starting from a few hundred Hz up to a few hundred MHz. The plurality of frequency bands used for PLC is related to different applications supported by PLC and their data-rate requirements, the specifics of grid topologies over which PLC is applied, as well as the ability of PLC technology to deal with the harsh communication environment. Before elaborating on this further, we first briefly review the terminology that has been used to describe PLC. [1]

The PLC designates a technology that uses the medium and low voltage electrical network to provide telecommunication services. Although, since its first applications when the frequency range started at a low level, PLC is today more commonly used for high-frequency applications, also known as broadband power line (BPL). [2]

The electrical network has been used for a long time by producers and distributors of electrical power for the purpose of network monitoring and remote control at low speed.

Nowadays, an electricity producer or distributor cannot ignore standardization. It is interesting to note that the deployment of electrical networks, their interconnection, and the ever-increasing number of electrical appliances have resulted in the emergence of the first network standardization bodies such as the IEC (International Electrotechnical Commission). [1]

1.1 PLC Technologies:

The principle behind the PLC technique is not one that has emerged recently. In 1838, Englishman Edward Davy proposed a solution allowing remote measurements to be taken of battery levels of sites far from the telegraph system between London and Liverpool. In 1897, he submitted the first patent (British Patent No. 24833) for a technique for the remote measurement of electrical network meters communicating over electrical wiring.

In 1950, the first PLC systems, known as Ripple Control, were designed and then deployed over medium- and low-voltage electrical networks. The carrier frequency was then between 100 Hz and 1 kHz. It was necessary to establish single-directional communications via control signals for the remote switching on and off of public lights or for tariff changes. The first industrial systems named Pulsadis appeared in France in 1960. The power involved was approximately a hundred kilovoltamperes (kVA).

Then the first CENELEC band PLC systems appeared, extending from 3 to 148.5 kHz, and allowing bidirectional communications over the LV (low voltage) electrical network, for instance, for meter readings (remote meter readings) as well as for a great number of applications relating to the home automation field (intruder alarm, fire detection, gas leak detection, and so forth). Much less power needed to be injected, since the power was reduced to levels of approximately a hundred milliwatts. [3]

The expression “power line carriers,” usually abbreviated to PLC, appeared at the end of World War II in 1945. By that time, many telephone and electrical lines had been destroyed and there were more infrastructure electrical lines than telephone lines. For communication purposes, systems were designed for data transmission over high or medium voltage wiring by imitating remote meter readings already carried out on the electrical lines.

Figure 1 illustrates the changes in the PLC technologies classified by speed since the beginning of the 1990s. [1]

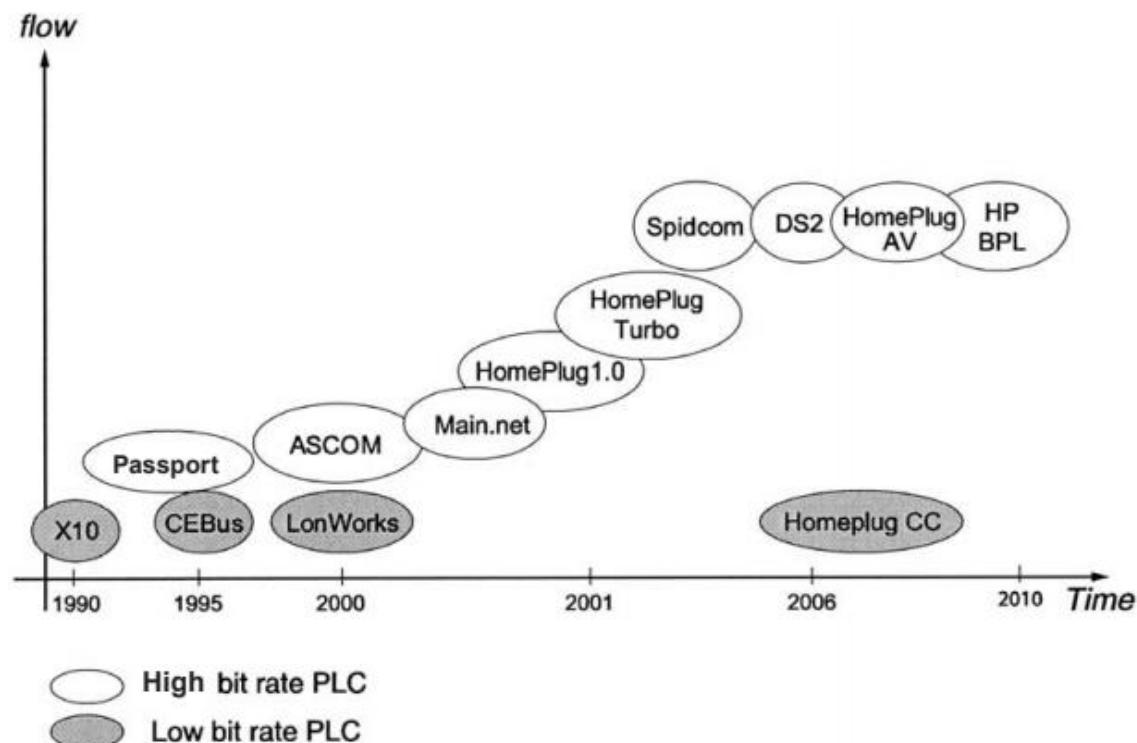


Figure 1: Low and High speed PLC Technologies

2 Project Overview

2.1 Details of the overall project and the solution.

Span of the project was divided into two stages. As per plan the initial stage was to make a prototype that can send a signal through the domestic power line and receive it. In the end, the prototype was successful. An online connection and a basic mobile application were implemented as an additional improvement. All the basics that needed to be clarified in the first stage are now clarified and all set to move to the final stage.

2.1.1 First Stage

In the end of the first stage, Signal transmitter was designed to get a command from a basic mobile application and real-time database of firebase through Wi-Fi and generate a signal that has a frequency of 470 kHz. That signal can be inserted through a wall socket and it transmits that signal throughout the domestic wiring.

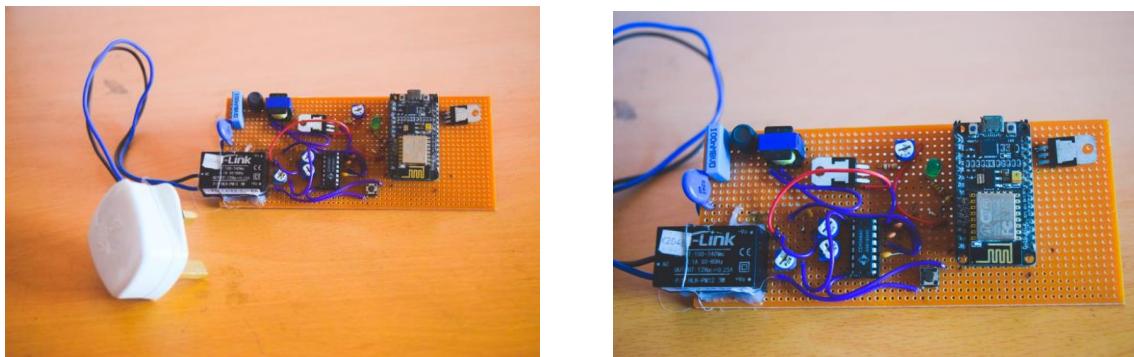


Figure 2: Designed Signal Transmitter at First Stage

Signal receiver was designed to get an input through wall socket and identify the 470 kHz signal that has been transmitted throughout the domestic wiring by the transmitter. When the Signal is given by the transmitter, the receiver identifies it as “1” and powers up the LED in it and otherwise it identifies as “0”.

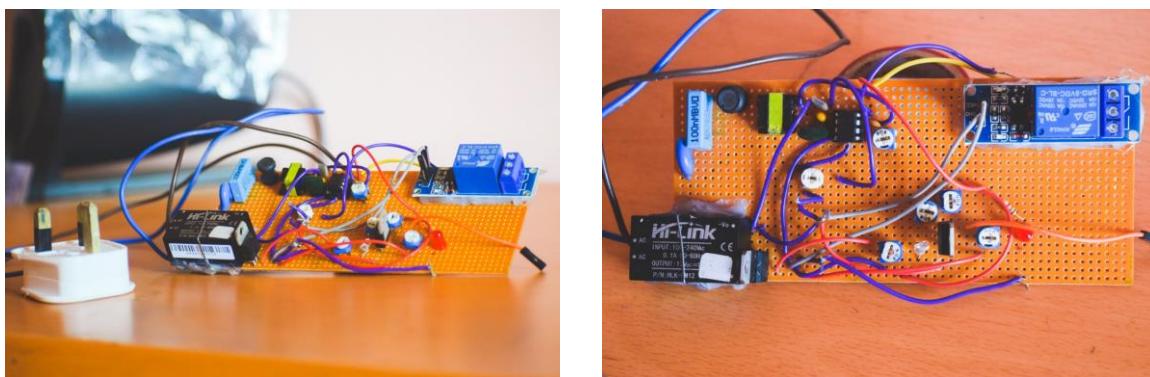


Figure 3: Designed Signal Receiver at First Stage

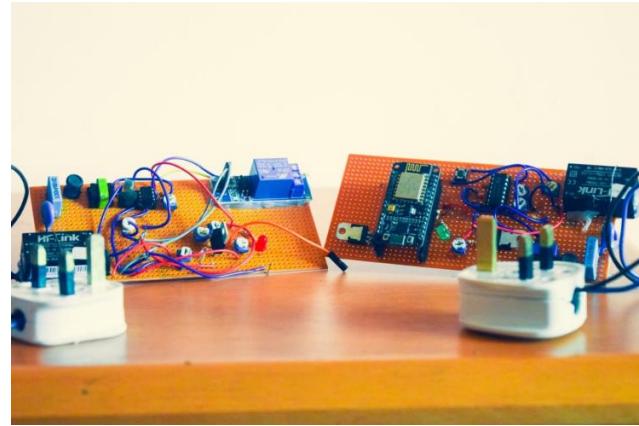


Figure 4: Designed Signal Transmitter and Signal Receiver at First Stage

2.1.2 Final Stage

In the final stage, Signal transmitter was designed to get a command from a mobile application and real-time database of Firebase through Wi-Fi and generate a message that was modulated to signal that has a frequency of 120 kHz. That signal can be inserted through a wall socket and it transmits this signal throughout the domestic wiring.

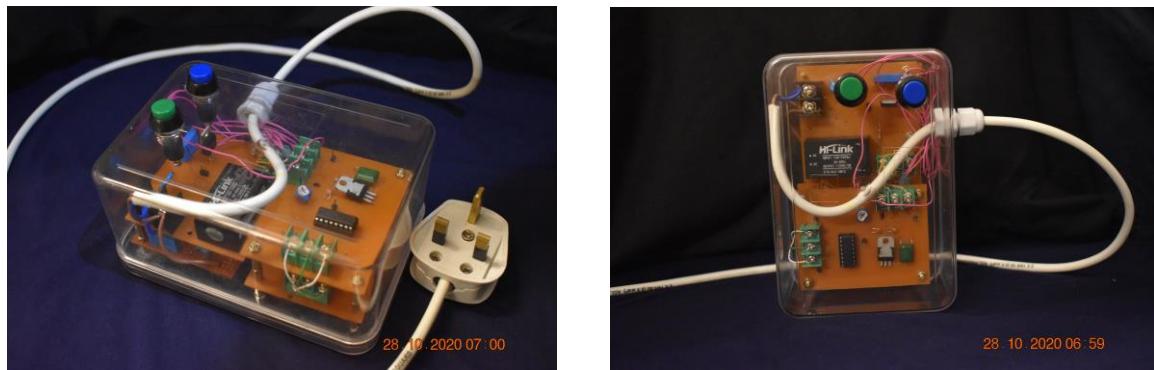


Figure 5: Designed Signal Transmitter at Final Stage

Signal receiver was designed to get an input through wall socket and identify the 120 kHz modulated signal that has been transmitted throughout the domestic wiring by the transmitter. Then it demodulates the signal and identifies the message and powers relay that allows to get power from the power outlet of the device.

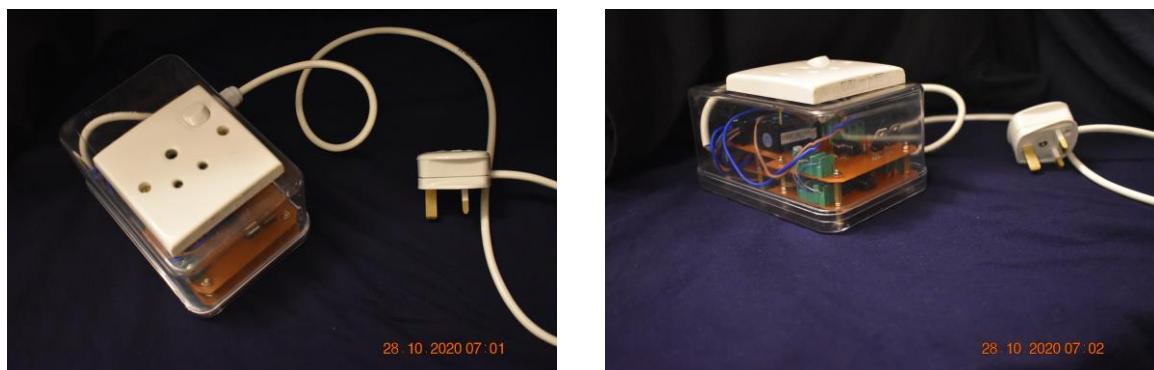


Figure 6 : Designed Signal Receiver at Final Stage



Figure 7: Designed Signal Transmitter and Signal Receiver at Final Stage

2.1.3 Future Implementation

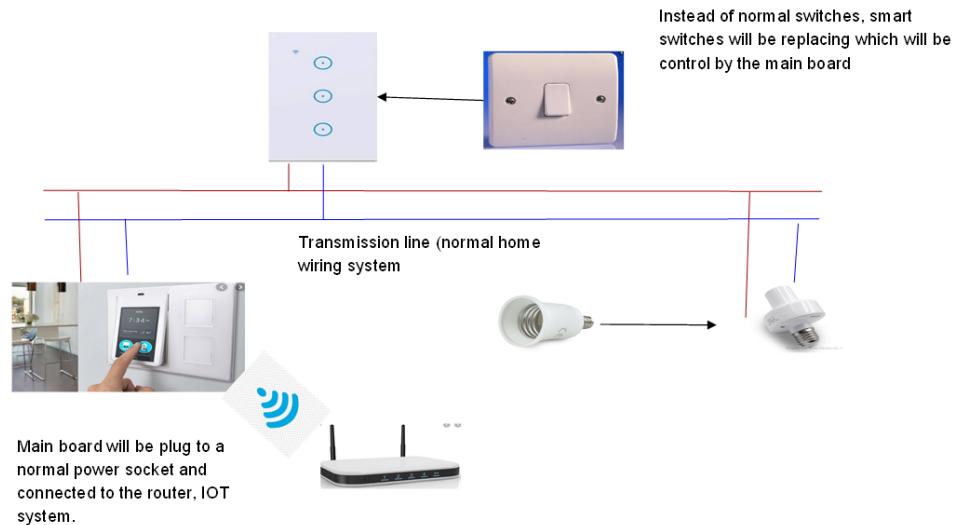


Figure 8: Expected Future Product

In the Future, Signal transmitter will be converted to a main board that can be connected to firebase and will have the ability to be controlled through a mobile applications and PC online software.

Signal receiver will be converted to a smart switch that can control the power supply through it.

Altogether the final product will be able to control any device in a domestic system from any corner in the world without having a micro controller for each and every device that need to be controlled.

2.2 Decision making process.

2.2.1 Test 1: Superimposing an Analog and Digital signals to the Low voltage AC signal.

According to the SC 205 standard a product, is to prepare harmonized international standard systems using the low voltage electric lines or the building wiring as a transmission medium and the frequency greater than 3 kHz up to 30 MHz.

Equipment:

- Signal Generator
- Oscilloscope
- Wiring Board
- Multimeter

Theory:

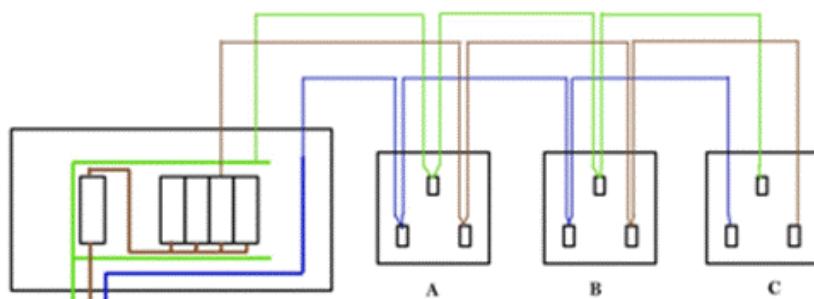


Figure 9: Radial Circuit

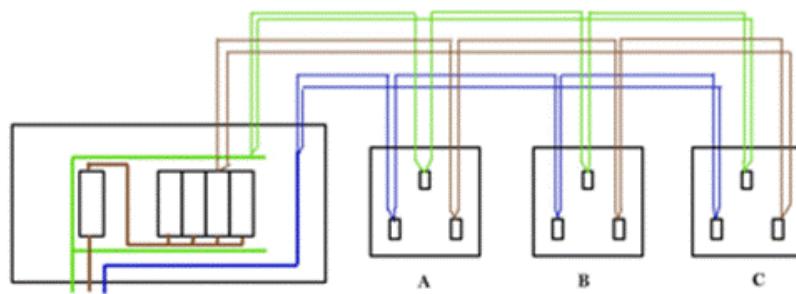


Figure 10: Ring Circuit

Procedure:

1. Wiring board was switched off.
2. Connectivity Radial Circuit (RAC) and Ring Circuit (RIC) was checked using multimeter.
3. AC signal of 1Vpp and 1kHz was inserted to a socket B of RAC and RIC using the signal generator.
4. Output from socket A and C of RAC and RIC were observed using oscilloscope.
5. Square signal of 1Vpp and 1kHz was inserted to socket B of RAC and RIC using the signal generator.
6. Output from socket A and C of RAC and RIC were observed using oscilloscope.
7. Low voltage AC signal of 10Vpp and 50Hz was inputted from the main distribution board.
8. AC signal of 1Vpp and 1kHz was inserted to socket B of RAC and RIC using the signal generator.
9. Output from socket A and C of RAC and RIC were observed using oscilloscope.
10. Square signal of 1Vpp and 1kHz was inserted to socket B of RAC and RIC using the signal generator.

Observations:

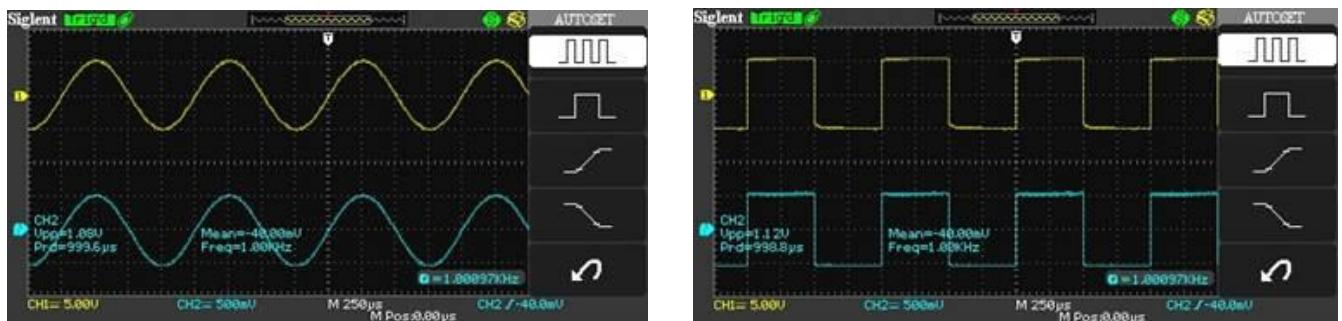


Figure 11: High frequency signal input

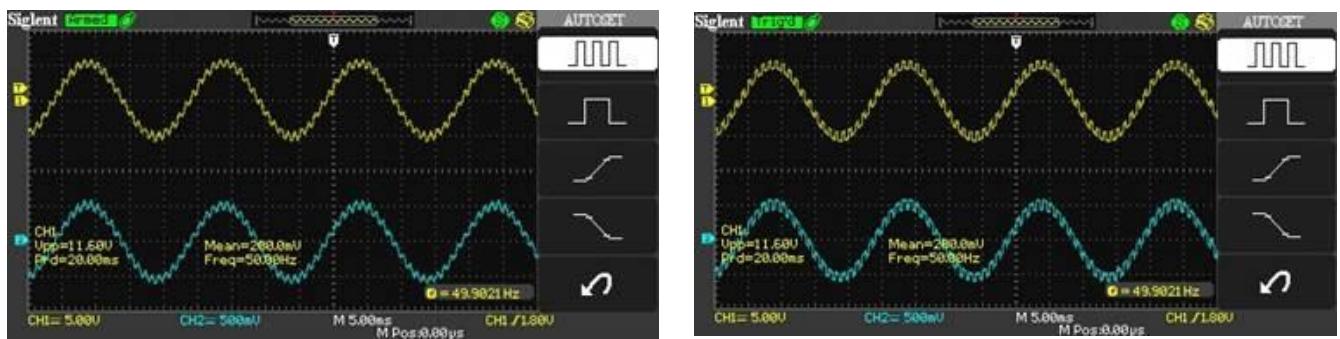


Figure 12: Signal output after superimposing the high frequency input signal

Discussion:

1. Irrespective of RIC or RAC the input from socket B can be taken as output from other sockets
2. When inputting a high frequency low voltage AC or square signal to the Low voltage AC signal it was superimposed and the shape was not affected.
3. High frequency low voltage carrier signal can be used to superimpose with a Low voltage AC signal and sent through housing wiring.

Conclusion:

1. A Coupling mechanism must be used to test with 230V 50Hz domestic power

2.2.2 Test 2: Superimposing Analog and Digital signals to the High voltage Domestic AC signal. (1kHz)

Equipment:

- Signal Generator
- Spectrum Analyzer
- Wiring Board
- 2 Transformers (230:12) as Couplers

Theory:

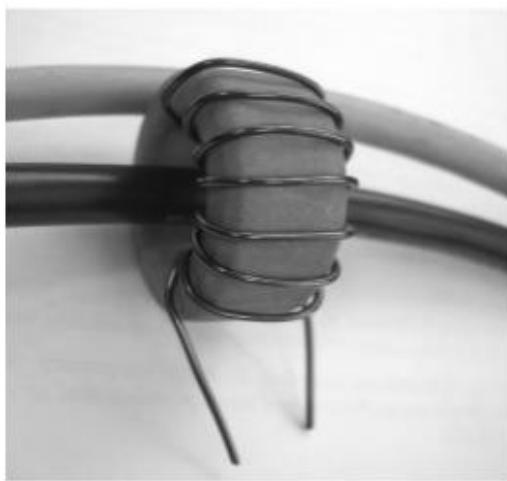
A PLC coupler may thus be defined as a device that allows a communication signal to be super imposed onto, and/or extracted from a power wave form, while also preventing the power waveform from entering the modem. Note that a transmitter-coupler would superimpose the communication signal onto the power waveform as noise, while a receiver-coupler would extract the communication signal from a power waveform (carrying the signal as noise).

PLC couplers may be broadly classified into two groups, namely inductive couplers and capacitive couplers.

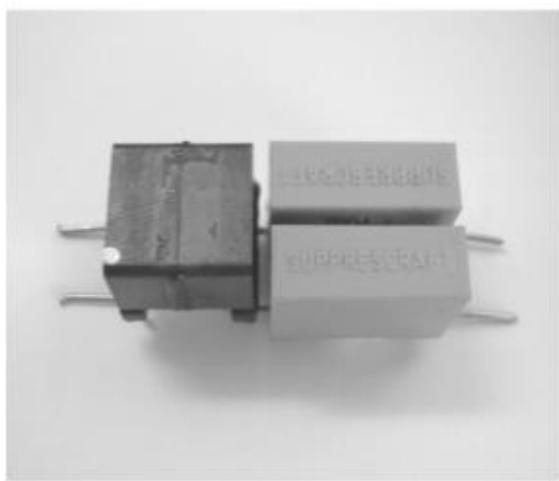
1. Inductive couplers
2. Capacitive couplers

Inductive couplers are electrically insulated from the power cables, and therefore no direct electrical connection is made.

Capacitive couplers, however, make up the bulk of power line couplers. This is especially true in Low Voltage (LV) applications where numerous transmitter and receiver nodes have to be implemented economically in order to compete against other network technologies such as wireless networks as well as cable networks. As the majority of LV PLC modems require dedicated Ac power for their DC power supplies, the direct electrical connection to the power grid is already a given. Therefore, the choice of a low-cost capacitive coupler, with a direct electrical connection to the power network, is obvious. These capacitive couplers may be as simple as a single series capacitor, or a simple passive L-C filter. However, the majority of capacitive PLC couplers do make use of an added coupling transformer for impedance adaptation and added protection. [2]



(a)



(b)

Figure 13: Types of Couplers

Figure 10 shows the typical couplers. (a) Inductive coupler with only two physical connections to the modem. However, that inductive couplers require a power cable (live or neutral) to be positioned through the center of some magnetic core, in order to complete the magnetic circuit for inductive coupling. (b) Capacitive coupler consisting of a transformer and two capacitors. All capacitive couplers have four terminals (two modem connections as well as two power line connections to live and neutral).

Therefore, capacitive transformers can be used.

A pulse transformer is a transformer that is optimized for transmitting rectangular electrical pulses (that is, pulses with fast rise and fall times and a relatively constant amplitude). Small versions called signal types are used in digital logic and telecommunications circuits, often for matching logic drivers to transmission lines. Medium-sized power versions are used in power-control circuits such as camera flash controllers. Larger power versions are used in the electrical power distribution industry to interface low-voltage control circuitry to the high-voltage gates of power semiconductors. Special high voltage pulse transformers are also used to generate high power pulses for radar, particle accelerators, or other high energy pulsed power applications. [2]

To minimize distortion of the pulse shape, a pulse transformer needs to have low values of leakage inductance and distributed capacitance, and a high open-circuit inductance. In power-type pulse transformers, a low coupling capacitance (between the primary and secondary) is important to protect the circuitry on the primary side from high-powered transients created by the load. For the same reason, high insulation resistance and high breakdown voltage are required. A good transient response is necessary to maintain the rectangular pulse shape at the secondary, because a pulse with slow edges would create switching losses in the power semiconductors.

The product of the peak pulse voltage and the duration of the pulse (or more accurately, the voltage-time integral) is often used to characterize pulse transformers. Generally speaking, the larger this product, the larger and more expensive the transformer.

Pulse transformers by definition have a duty cycle of less than 0.5, whatever energy stored in the coil during the pulse must be "dumped" out before the pulse is fired again.

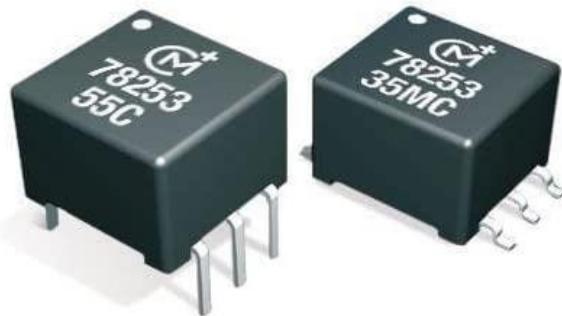


Figure 14: Pulse transformers

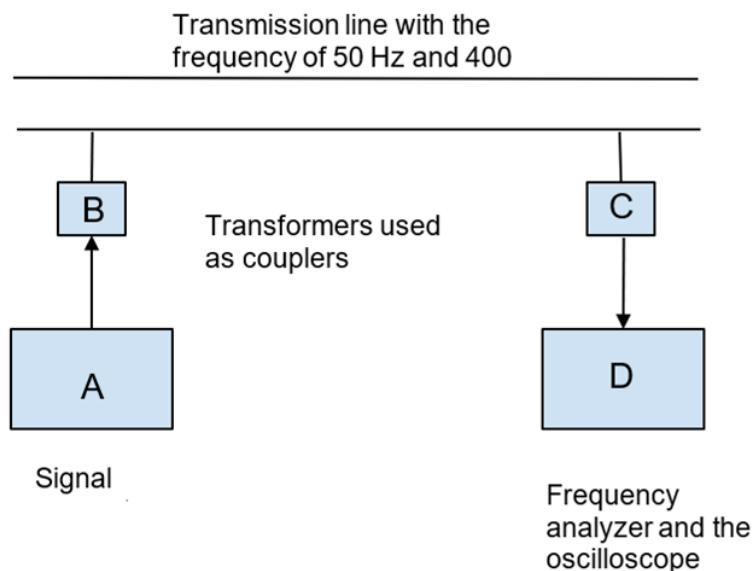


Figure 15: Test Setting

Procedure:

1. All equipment was set according to the test setting
2. AC signal of 20V Vpp and 1kHz was inserted to socket through step-down transformer B
3. Output from the socket through step-down transformer C was observed using oscilloscope and spectrum analyzer.
4. Square signal of 20V Vpp and 1kHz was inserted to socket through step-down transformer B
5. Output from the socket through step-down transformer C was observed using oscilloscope and spectrum analyzer.

Observations:

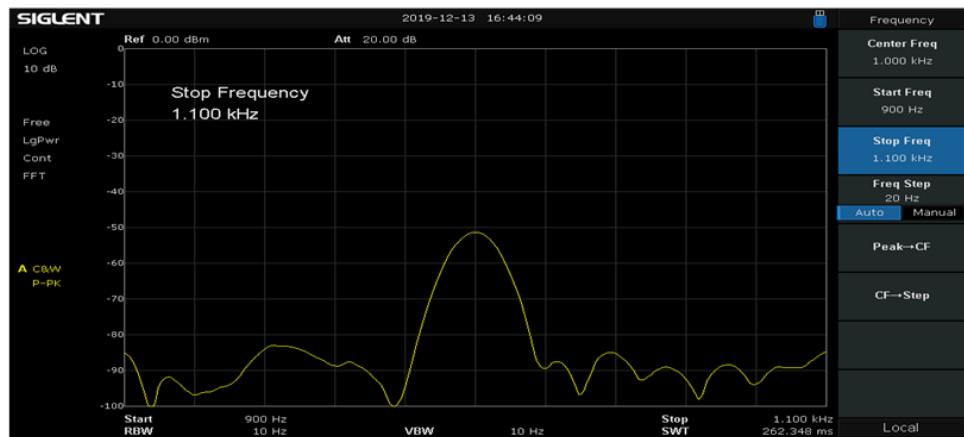


Figure 16: Output from Socket C of AC and Square Signal of 20V Vpp and 1 kHz without Domestic Power Signal

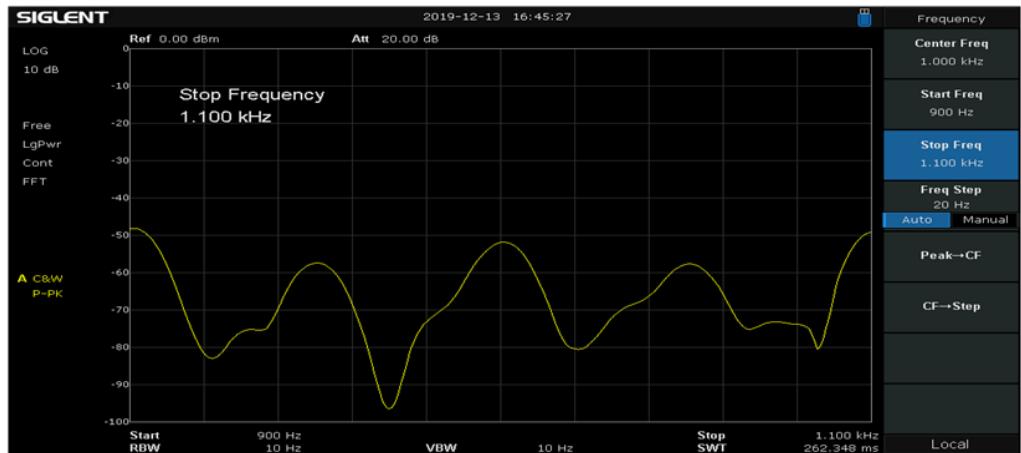


Figure 17: Output from Socket C of AC and Square Signal of 20V Vpp and 1kHz without Domestic Power Signal (Range, 900Hz-1100Hz)

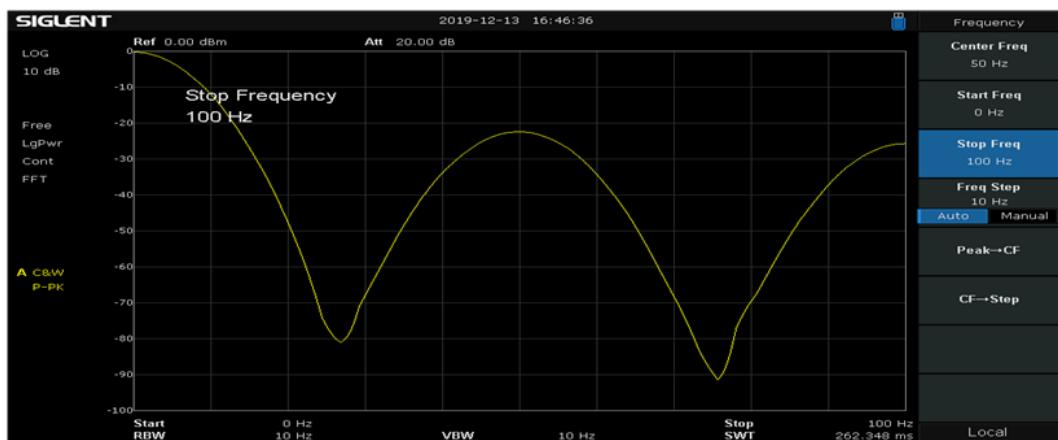


Figure 18: Output from Socket C of AC and Square Signal of 20V Vpp and 1 kHz without Domestic Power Signal (Range, 0Hz-100Hz)

Discussion:

1. The AC and square signal cannot be seen with direct connection from transformer
2. When inputting a high frequency low voltage AC or square signal to the high voltage AC high frequency signal doesn't appear in the end.
3. As a power transformer couldn't pass high frequency, RF transformers were selected. In Sri Lanka market RF transformers couldn't be found.
4. For project most appropriate one can be the pulse transformer

Conclusion:

1. Filter must be used to filter out the 50Hz signal from the signal.
2. Must check for higher frequencies.
3. Study on Pulse Transformers must be done.
4. Required RF transformers were unplugged from the phone charges.

2.2.3 Test 3: Superimposing Analog signal to the High voltage Domestic AC signal. (2.5 kHz)

Equipment:

- Signal Generator
- Spectrum Analyzer
- Wiring Board
- 2 Transformers (230:12)

Theory:

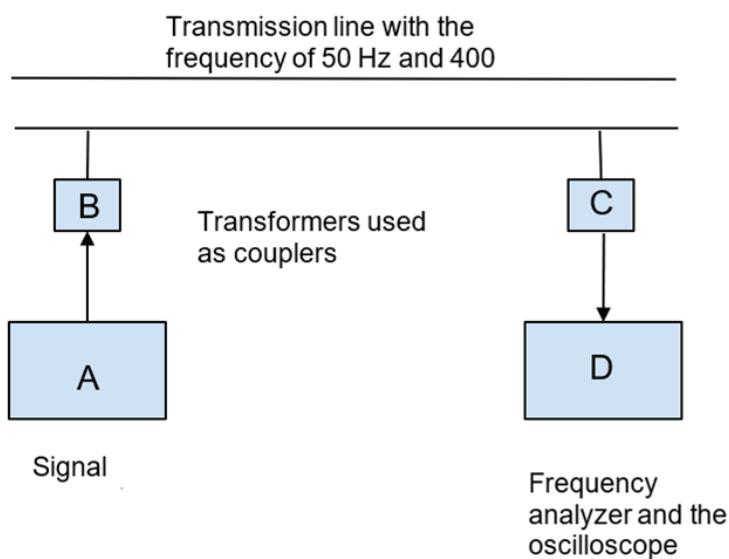


Figure 19: Test Setting

Procedure:

1. All equipment was set according to the figure 19
2. Only the domestic 230V supply was given through the transformer and output from C was observed from spectrum analyzer
3. Only the AC 10V Vpp 2.5kHz was given by signal generator and output from C was observed from spectrum analyzer
4. Both signals were given and output from C was observed from spectrum analyzer

Observations:

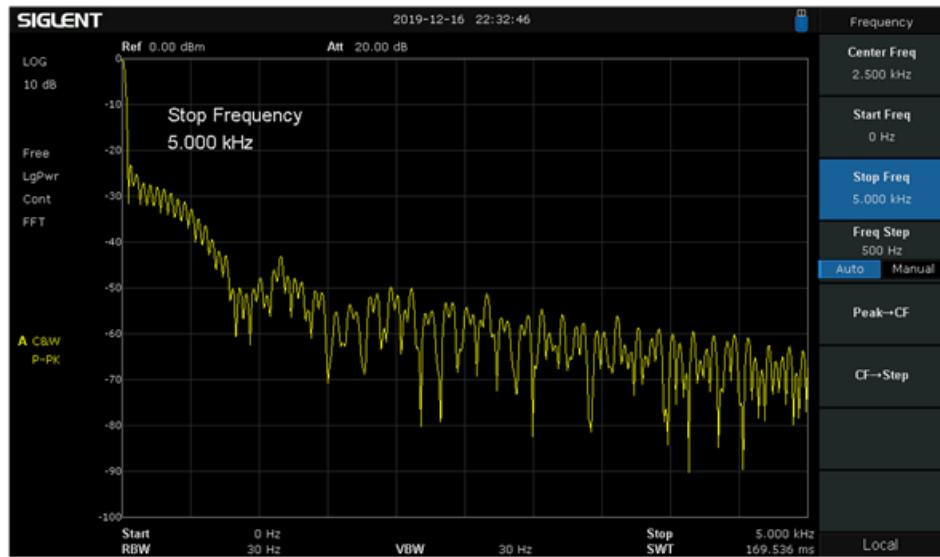


Figure 20: Output from C of only with 230V Domestic Power Signal

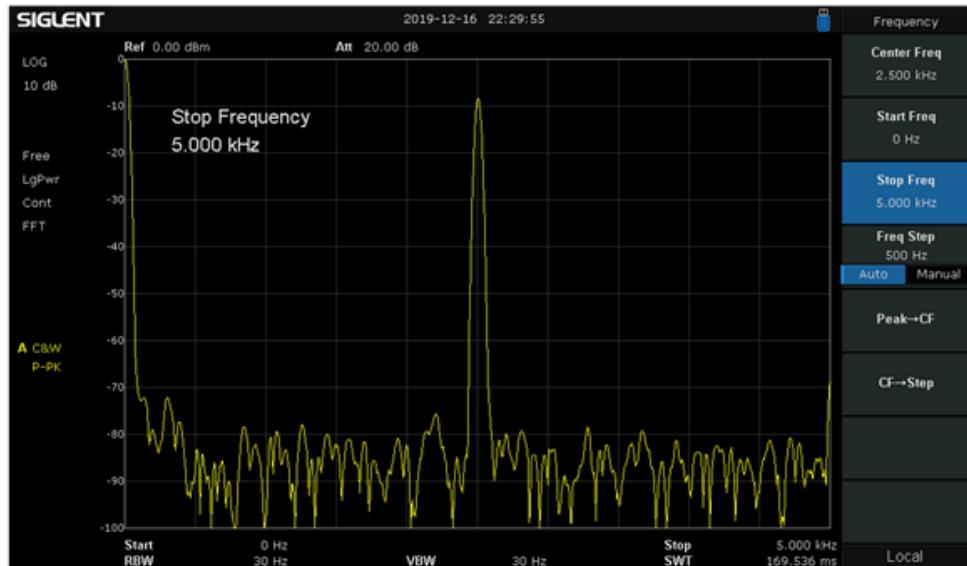


Figure 21: Output C of only with 10V Vpp 2.5kHz AC Signal

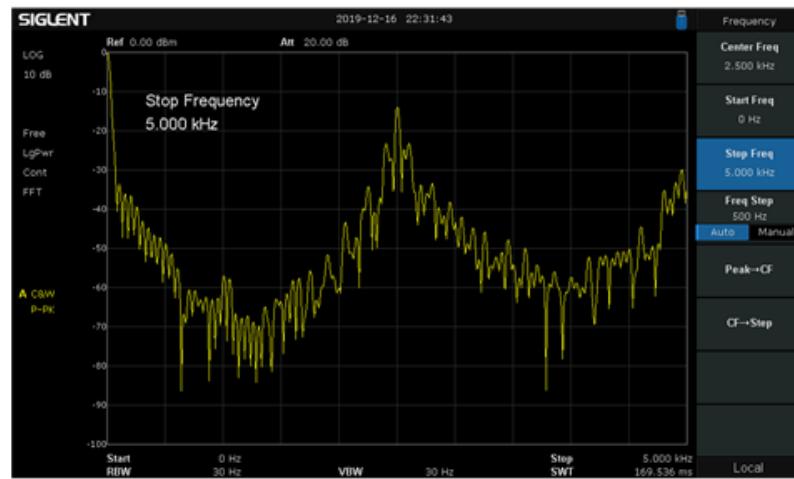


Figure 22: Output from C when the first input is the High Frequency AC signal

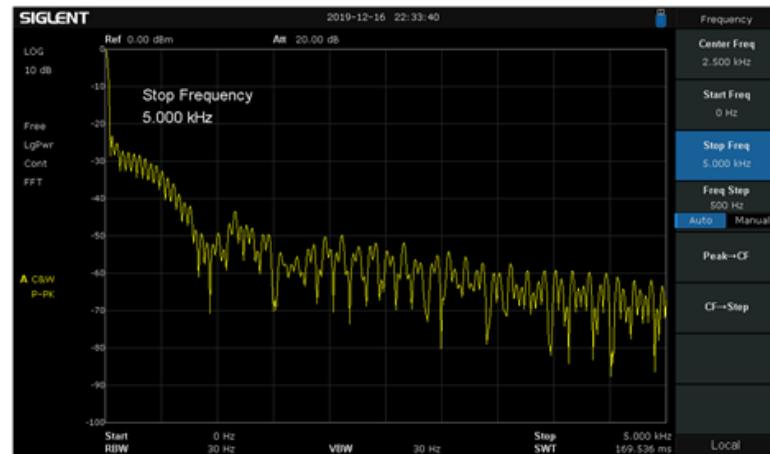


Figure 23: Output from C When the first Input is 230 V Domestic Signal

Discussion:

1. Both signals can be seen from output C when the first input is the high frequency AC signal
2. Both signals cannot be seen from output C when the first Input is 230V 50Hz domestic signal

Conclusion:

1. Solution must be found for the switching problem
2. Filter must be used to filter out the 50Hz signal from the signal
3. Must check for higher frequencies.

2.2.4 Test 4: Superimposing Analog signal to the High voltage Domestic AC signal. (300k Hz)

Equipment:

- Signal Generator
- Spectrum Analyzer
- Wiring Board
- 2 Transformers (230:12)

Theory:

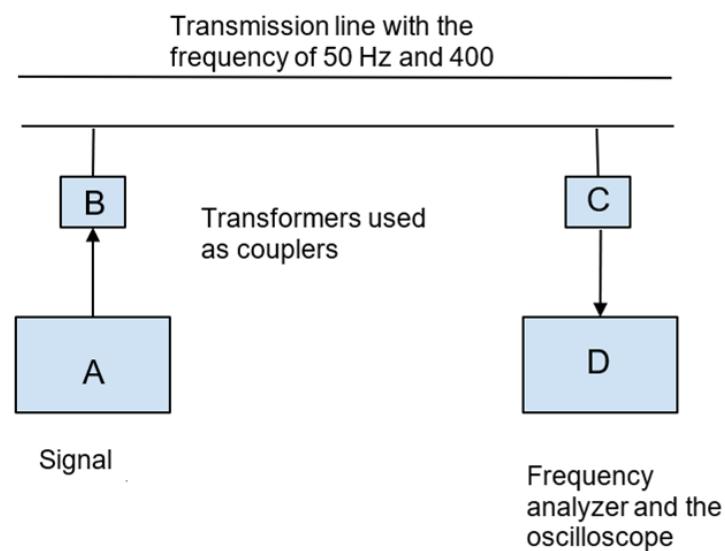


Figure 24: Test Setting

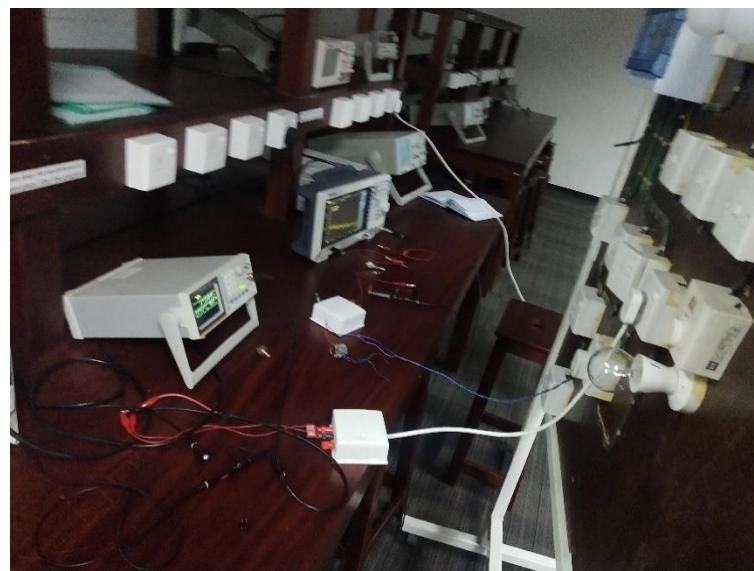


Figure 25: Equipment Arrangement

Procedure:

1. All equipment were set according to the figure 25 given above
 2. AC signal of 20V Vpp and 300kHz was inserted to socket through step-down transformer B
 3. Output from the socket through step-down transformer C was observed using oscilloscope and spectrum analyzer.
 4. Square signal of 20V Vpp and 300kHz was inserted to socket through step-down transformer B
 5. Output from the socket through step-down transformer C was observed using oscilloscope and spectrum analyzer.

Observations:

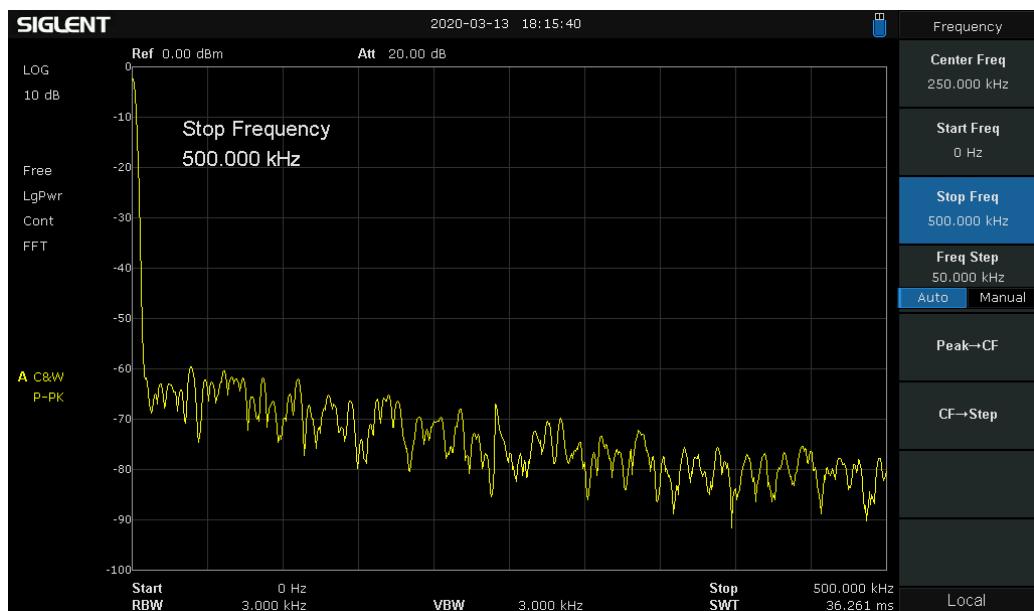


Figure 26: Output from the Socket through Step-down Transformer C without 300 kHz Signal

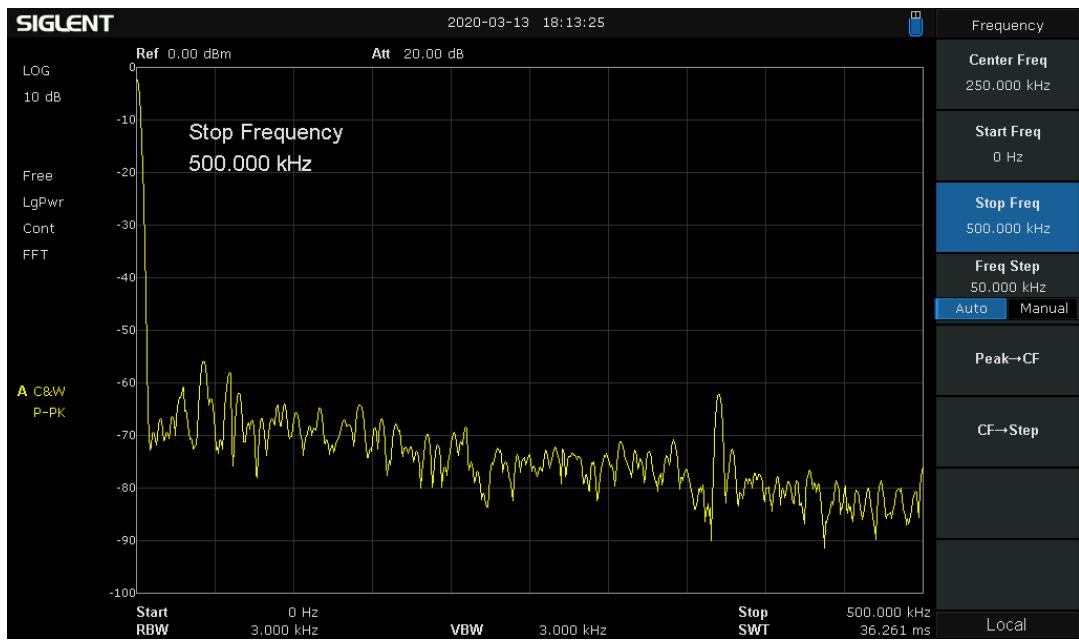


Figure 27: Output from the Socket through Step-down Transformer C with 300 kHz Signal

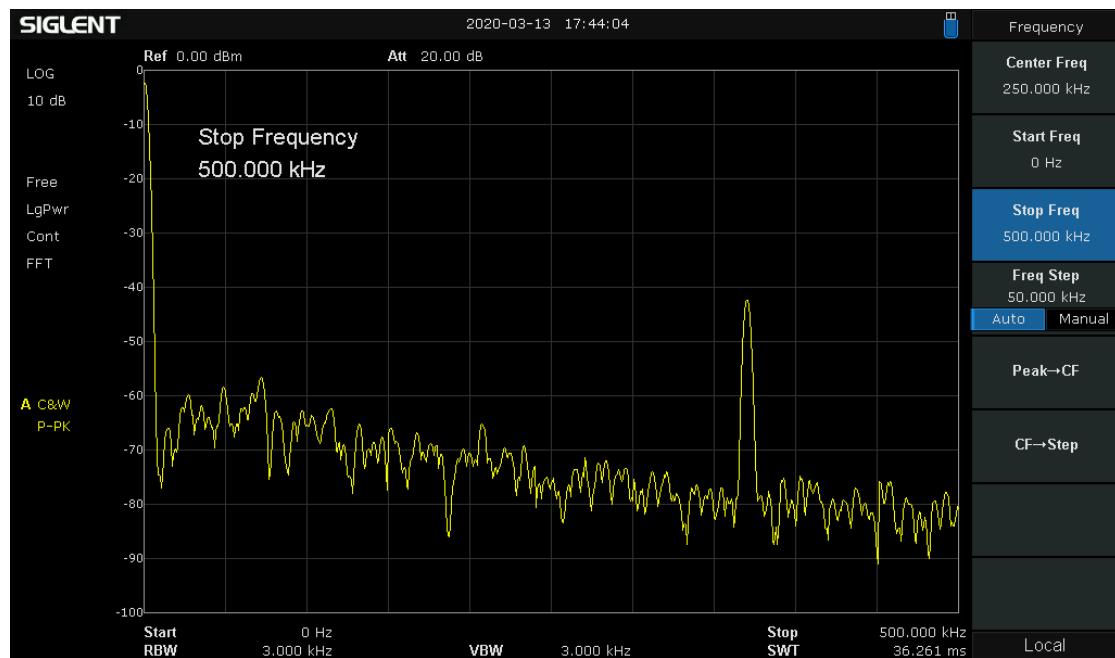


Figure 28: Output from the Socket through Step-down Transformer C with 300 kHz Signal and without Domestic signal

Discussion:

1. Both Signals can be seen from output C irrespective of what signal was inputted first.
2. Gain of the 300 kHz was affected from 50Hz domestic signal.

Conclusion:

1. 20V, Vpp and 300kHz Signal can be seen from the output even when the domestic power was applied
2. Filter must be used to filter out the 50Hz signal from the signal because the gain of the 20V, Vpp and 300kHz signal was very low

2.2.5 Test 5: Filtering the 50Hz

Equipment:

- Signal Generator
- Spectrum Analyzer
- Wiring Board
- 1 Transformers (230:12)
- Capacitors (2 nF and 100 nF)
- Inductors (56 uH)

Software:

- OrCAD Capture CIS - Lite

Theory:

The ability to selectively attenuate different frequencies or frequency components of a signal. Filtering forms the basis of most coupling and decoupling circuits. Decoupling filters are typically used for network conditioning whereas coupling filters feed the communication signal to and from the power line.

Filtering may include the filtering of noise, filtering to improve phase distortion and filtering to prevent incoming and outgoing EMI.

Proper filter design is,

1. Essential for minimum signal attenuation when coupling to the power line
2. Can help improve signal to-noise ratios.

A periodic waveform can be thought of as a unique mixture of sinusoids, each with a certain frequency and amplitude, that form one superimposed signal. Every individual sub sinusoid of a signal is changed by the filtering process, depending on its frequency [4]. This change is twofold: amplitude is attenuated by a certain factor, and phase angle is shifted to a certain degree. After the filtering process, the resultant waveform is once again the sum of the individual sub sinusoids. Thus, the filtered wave form is now composed to a lesser degree of some frequency (sinusoidal) components because they have been

attenuated or filtered to a certain degree. As each sub sinusoid is typically phase-shifted by a different angle, the filtered wave form shows not only phase delay but also phase distortion, a side-effect.

Single and paired capacitors are used extensively in PLC to couple the communication signal to the power line while ‘blocking’ the low frequency (LF) power signal. This application is well known in transistor circuit theory, as a series capacitor is typically used to disconnect or block DC biasing voltages but pass small-signal AC voltages. This is possible due to the frequency-dependent impedance of an ideal capacitor (valid for a specific frequency sine wave):

$$Z_C = 1/j\omega C = (1/2\pi f C) > -90^\circ$$

Equation 1: Capacitive impedance

It is obvious that any capacitor’s impedance will tend to infinity at DC ($f = 0\text{Hz}$), blocking any DC component of a signal. At low frequencies, such as power line frequencies, its impedance is high enough to revert almost 100% of the signal to lower impedance paths of the power line (current-divider rule). At the communication signal frequency, however, the coupling capacitor would be designed to have a low enough impedance to admit a large portion of the communication signal, making it available to the receiver. [4]

If a PLC system uses a sinusoidal carrier signal, say of 500 kHz superimposed on a 50 Hz sinusoidal power waveform, the following conclusions can be made for a $1\text{ }\mu\text{F}$ series capacitor: the capacitor can be modeled as two parallel impedances, one parallel path for low (power line) frequencies and another for high (communication) frequencies.

The LF path has an impedance magnitude of $3.18\text{ k}\Omega$ whereas the HF path has an impedance magnitude of only 0.318 (inversely proportional to frequency). Both the HF and LF path impedances have the same phase angle, however (-90°).

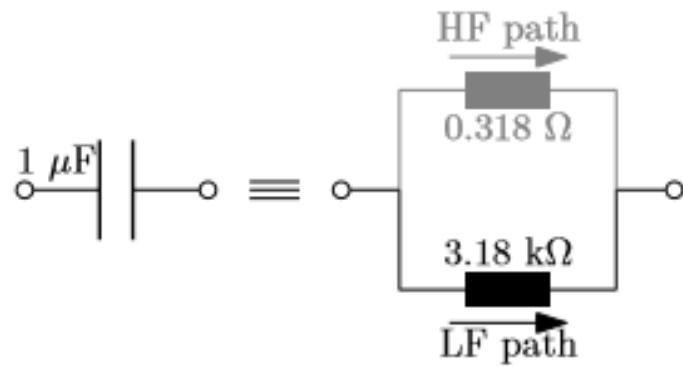


Figure 29: Equivalent circuit for capacitive filter

Designing of band pass filter was important to cut off the most high frequency which are added as noise from the power switching and telecommunication devices.

Inductors function complementarily to capacitors: HF signals (or harmonics) are blocked and LF signals (or harmonics) passed, the reason being that an ideal inductor has a unique impedance for each sub sinusoid of a waveform, proportional to the sub sinusoid's frequency

$$ZL = j\omega L = 2\pi f L + 90^\circ$$

Equation 2: Inductive impedance

In a power line network, any series inductor would impede the HF communication signal to a certain degree, from flowing through that specific path. Thus, unnecessary loss of transmitted power can be prevented by ‘blocking’ off branches of the network that will not be utilized for PLC. If a $1 \mu\text{H}$ series-inductor is considered with the same PLC scheme as discussed above (50 Hz waveform with 500 kHz carrier), it can be modeled as a 3.14 k impedance for HFs

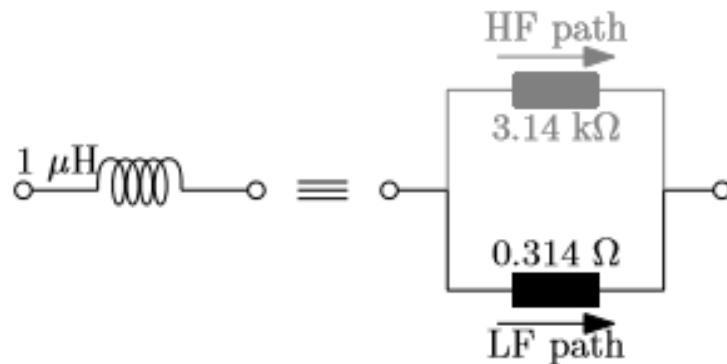


Figure 30: Equivalent for Inductive filter

As an example, for capacitor,

The HF-LF model is used further to illustrate the filtering operation of a $1 \mu\text{F}$ capacitor terminating into a 50-load resistor. The voltage-divider rule can be used to obtain the voltage transfer function of the HF path as,

$$V_{\text{OUT}} / V_{\text{IN}} = 50 < 0^\circ / (50 < 0^\circ + 0.318 < -90^\circ) \approx 1 < 0.364^\circ$$

And

$$V_{\text{OUT}} / V_{\text{IN}} = 50 < 0^\circ / (50 < 0^\circ + 3.18 \times 10^3 < -90^\circ) \approx 0.0157 < 89.1^\circ$$

Equation 3: $V_{\text{out}}/V_{\text{in}}$

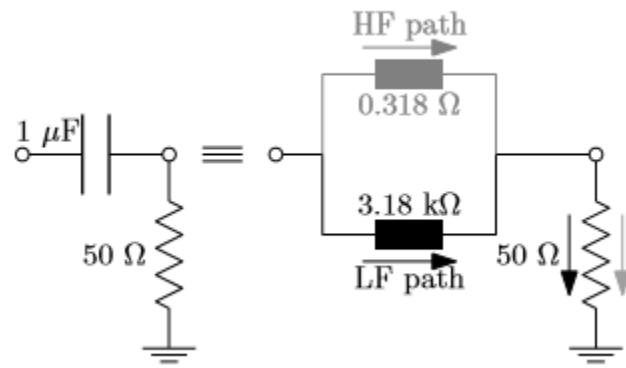


Figure 31 : Equivalent circuit for filter as a voltage divider

For the inductor it was same as the above. Only the change is it passes the LF and cutoff HF. (More Vout for LF and lower Vout for HF).

Design a band pass filter -

In the simple shunt capacitor filter circuit explained above, concluded that the capacitor will reduce the ripple voltage, but causes the diode current to increase. This large current may damage the diode and will further cause heating problem and decrease the efficiency of the filter. On the other hand, a simple series inductor reduces both the peak and effective values of the output current and output voltage. Then if combine both the filter (L and C), a new filter called the L-C filter can be designed which will have a good efficiency, with restricted diode current and enough ripple removal factor. The voltage stabilizing action of shunt capacitor and the current smoothing action of series inductor filter can be combined to form a perfect practical filter circuit. [2]

L-C filters can be of two types: Choke Input L-section Filter and L-C Capacitor input filter

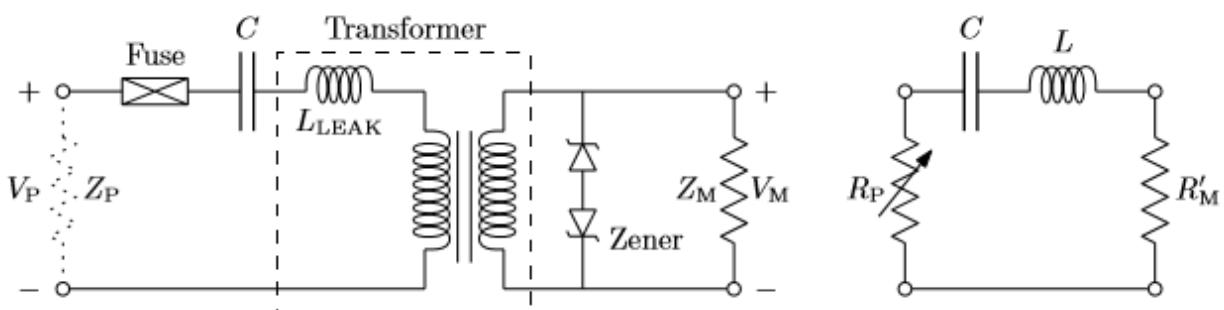


Figure 32: RCL filter design

Frequency specifications,

For the frequency range ≈ 90 kHz to ≈ 150 kHz. Thus, 90 kHz would be the worst-case frequency for core considerations and 150 kHz would be the frequency where copper losses would be a maximum.

Impedance levels,

The coupler will still be designed to function at a minimum power line impedance level of 0.25 ohms without overheating. In this case, although currents are higher, power output will actually be reduced because of the impedance mismatch.

It is also assumed that a 50-ohm modem impedance needs to be adapted to the 1-ohm impedance of the power line. This can be done using a 1:7 transformer winding ratio, seen from the power line side. The 50-ohm modem impedance appears as $(1/7)^2 \times 50 \approx 1$ ohm on the power line side, whereas the 1 power line impedance appears as $(7/1)^2 \times 1 \approx 49$ ohm on the modem side. [2]

Maximum voltage level,

Thus, a maximum voltage of 122 dB μ V (which represents ≈ 1.26 VPEAK or 0.89 VRMS) can be injected into the power line network and this represents a voltage of 8.81VPEAK or 6.23VRMS on the modem side of the coupling transformer.

Maximum current level,

In order to calculate the maximum transformer current levels, a minimum power line impedance of 0.25 is assumed. This gives an estimated power throughput of 3.17 W and maximum currents of 3.56 ARMS and 0.51 ARMS for the power line side and modem side, respectively.

An E20 core was chosen, manufactured from Mn-Zn ferrite material. [2]

Software Simulations using OrCAD Capture CIS - Lite,

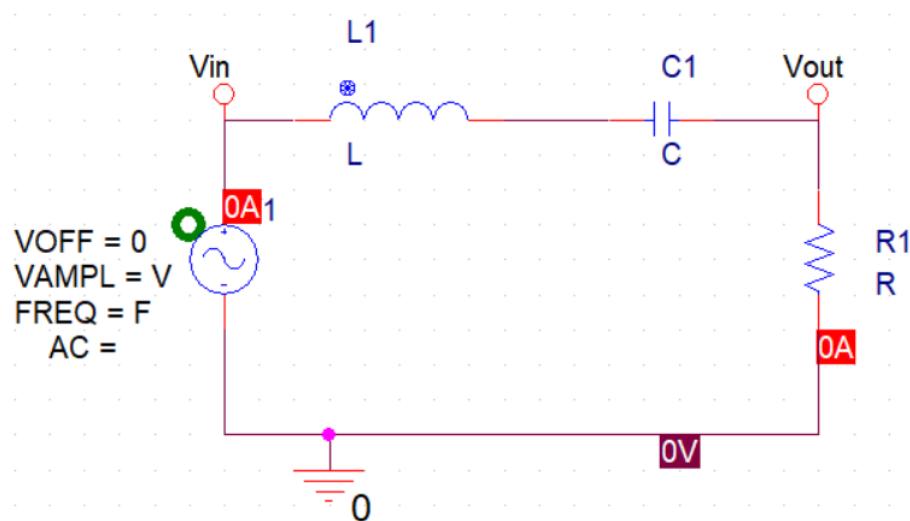


Figure 33: OrCAD Capture CIS - Lite, Schematic 1

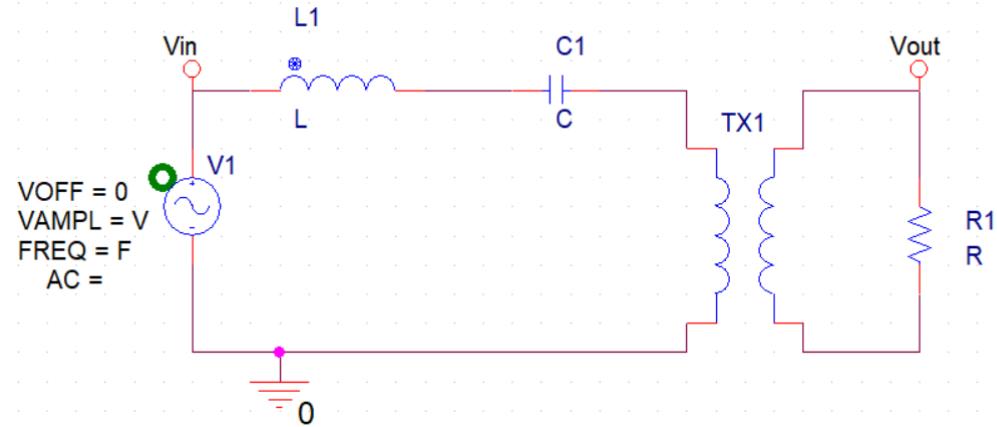


Figure 34: OrCAD Capture CIS - Lite, Schematic 2

Procedure:

1. C and L of OrCAD Capture CIS - Lite, schematic 1 were set to 100n and 47uH.
2. VAMPL and FREQ were set to 10V and 60Hz.
3. Time domain (Transient) was checked from Vin and Vout.
4. VAMPL and FREQ were set to 230V and 60Hz.
5. Time domain (Transient) was checked from Vin and Vout.
6. C and L of OrCAD Capture CIS - Lite, schematic 2 were set to 100n and 47uH.
7. VAMPL and FREQ were set to 230V and 60Hz.
8. Time domain (Transient) was checked from Vin and Vout.
9. Circuit was designed according to the OrCAD Capture CIS - Lite, Schematic 2.
10. Output was checked using the spectrum analyzer with the filter.
11. C was changed by inputting a series Capacitor of 2 nF output was checked using the spectrum analyzer with the filter.

Observations:

OrCAD Capture CIS - Lite Simulations

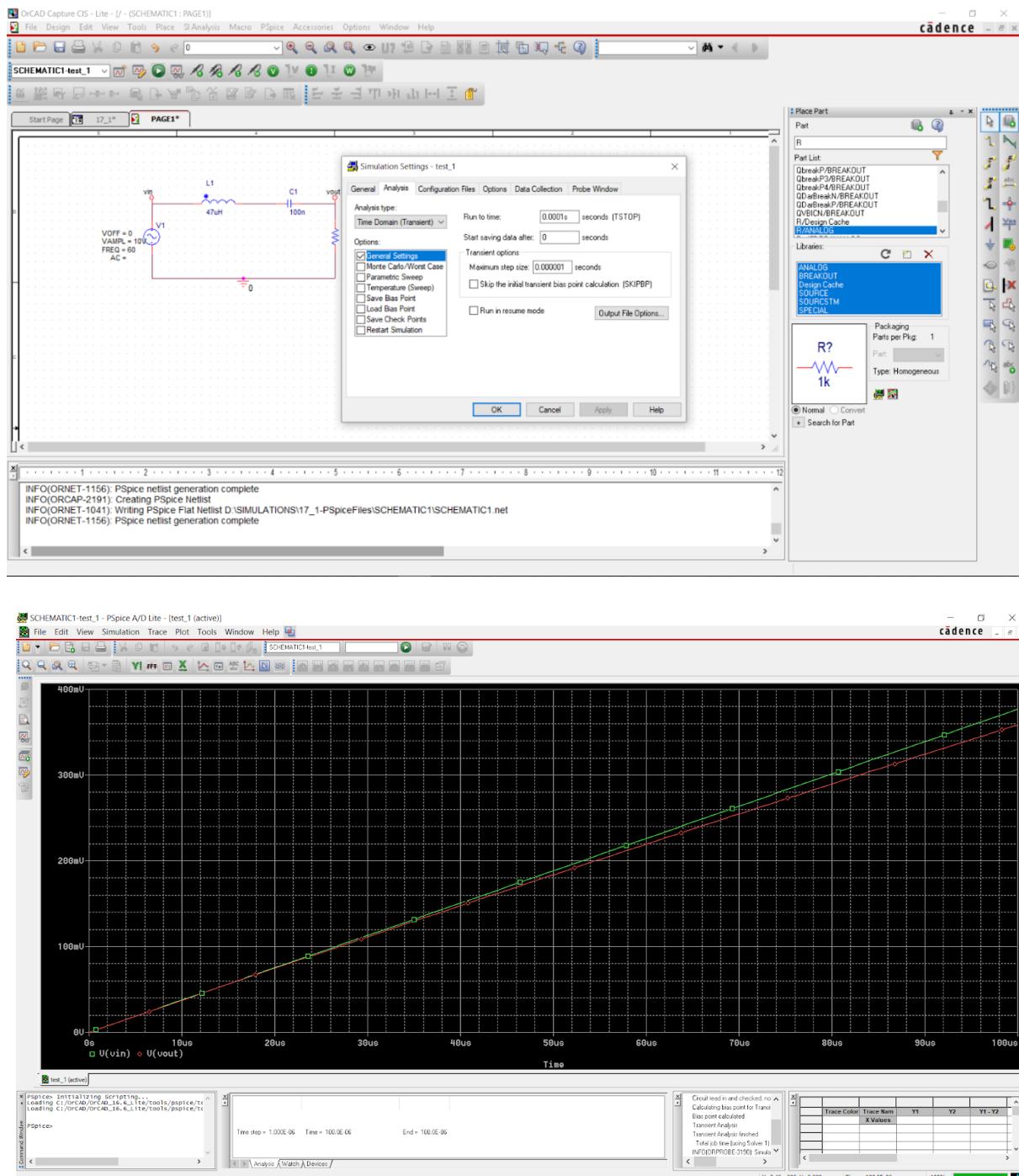


Figure 35: Schematic - 1 - 60 Hz 10V runtime 0.0001s

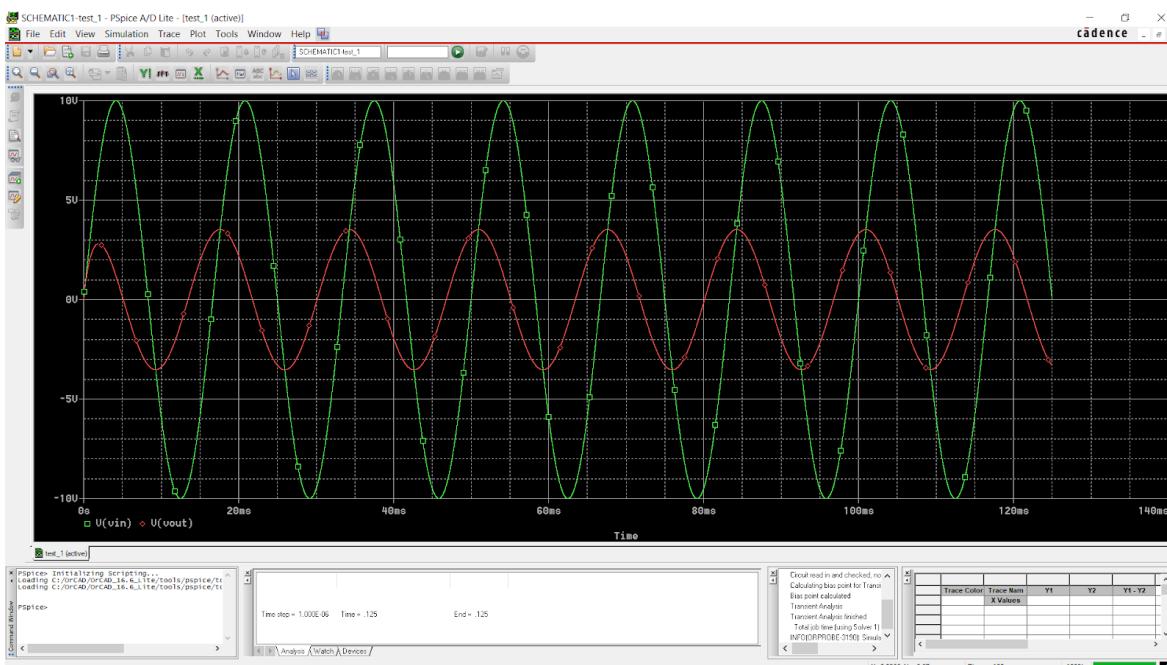
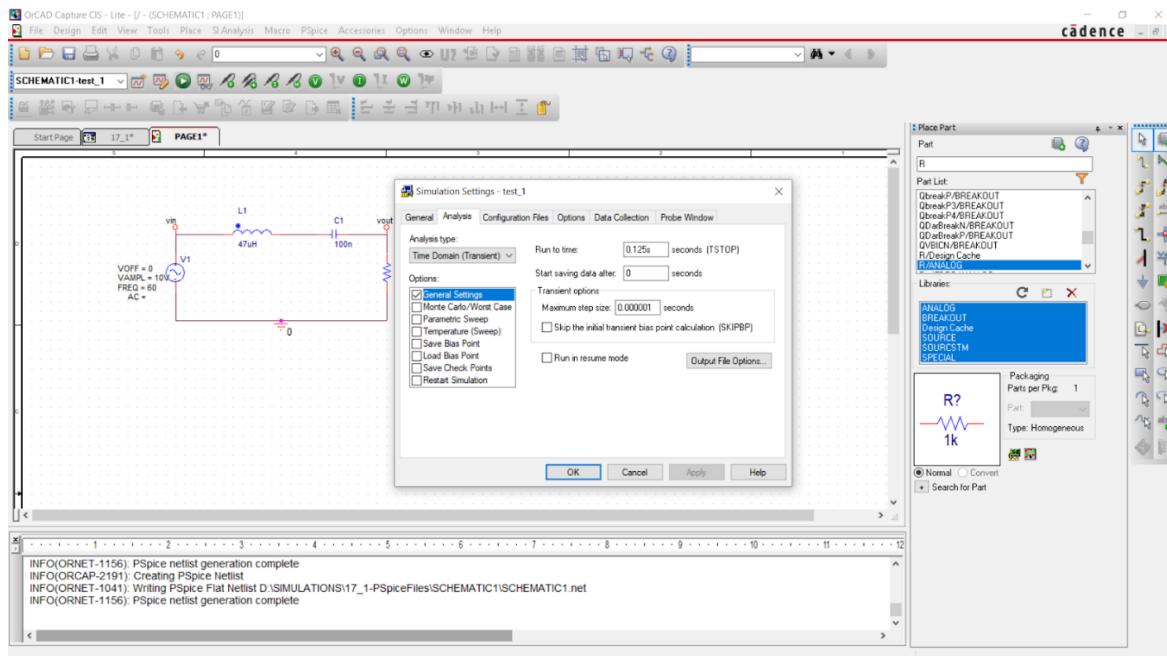


Figure 36: Schematic - 1 - 60 Hz 10V runtime 0.125s

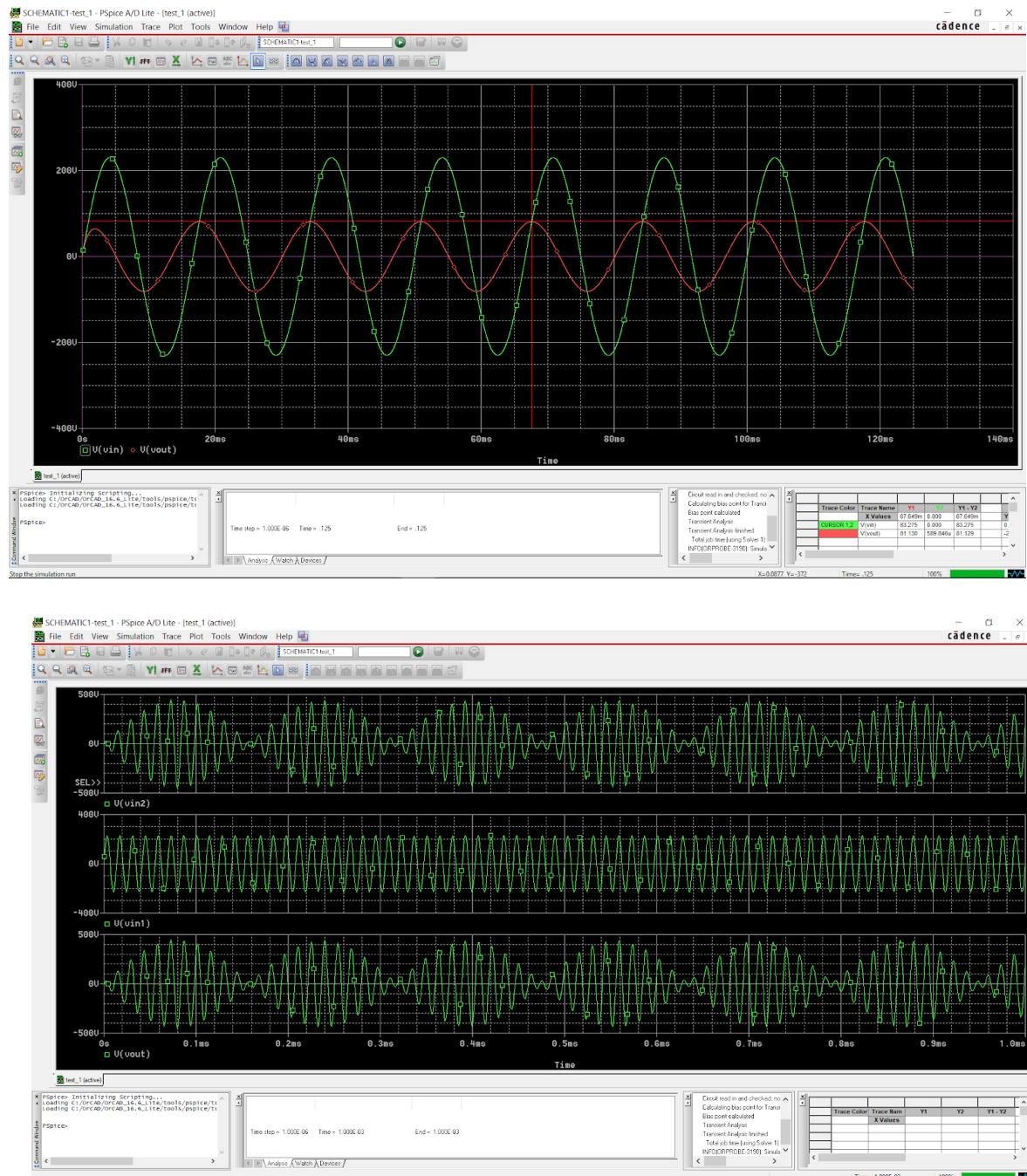


Figure 37: Schematic - 2 - 60 Hz 230V

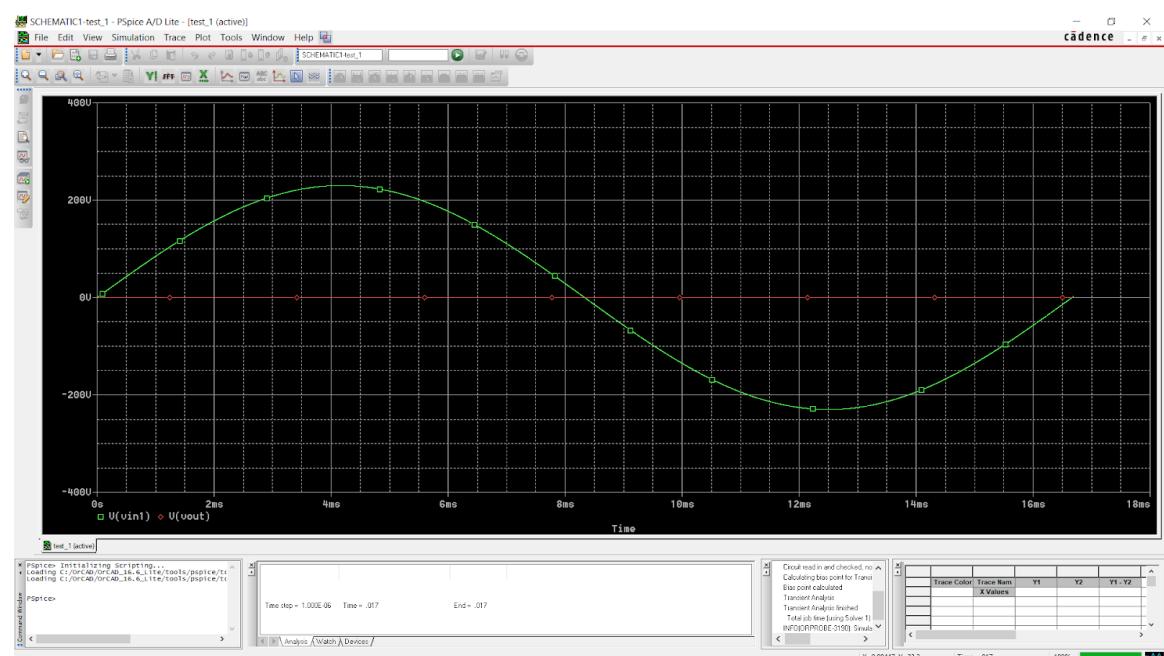
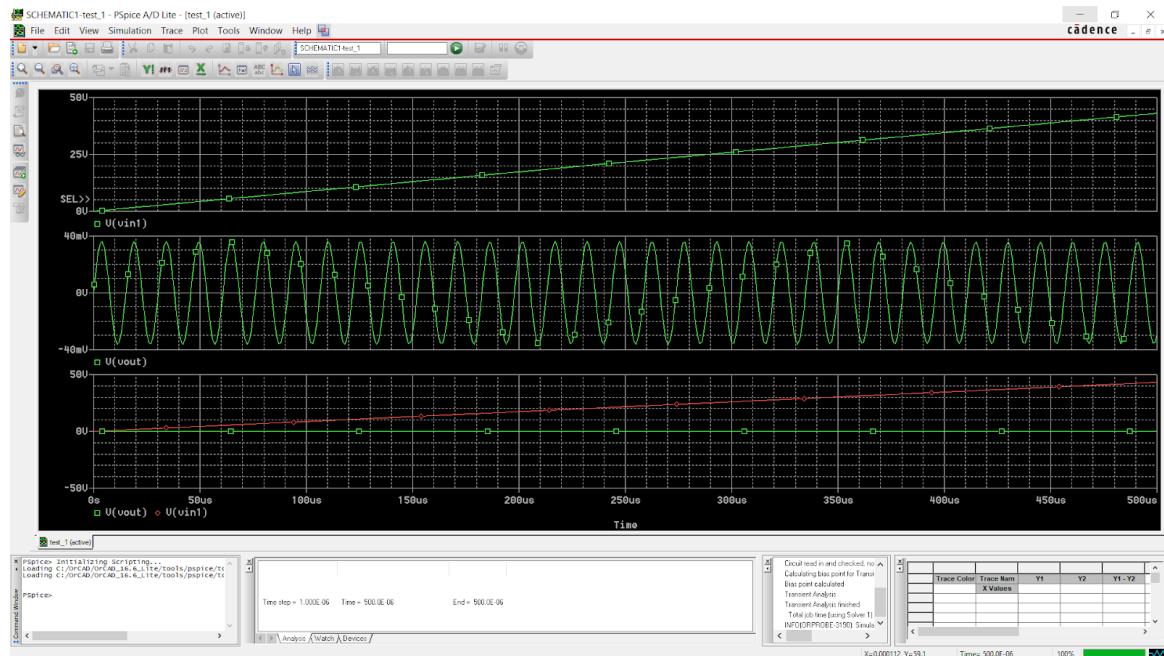


Figure 38: Schematic - 3 - 60 Hz 230V with transformer

Circuit output observations,



Figure 39: Equipment Arrangement

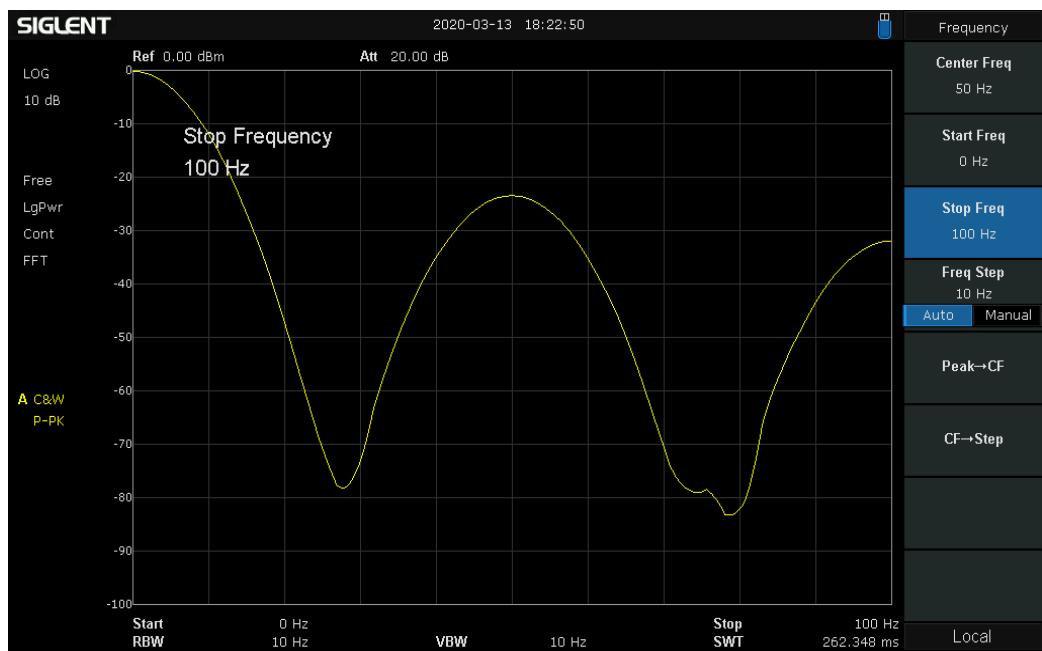


Figure 40: Output with planned Filter

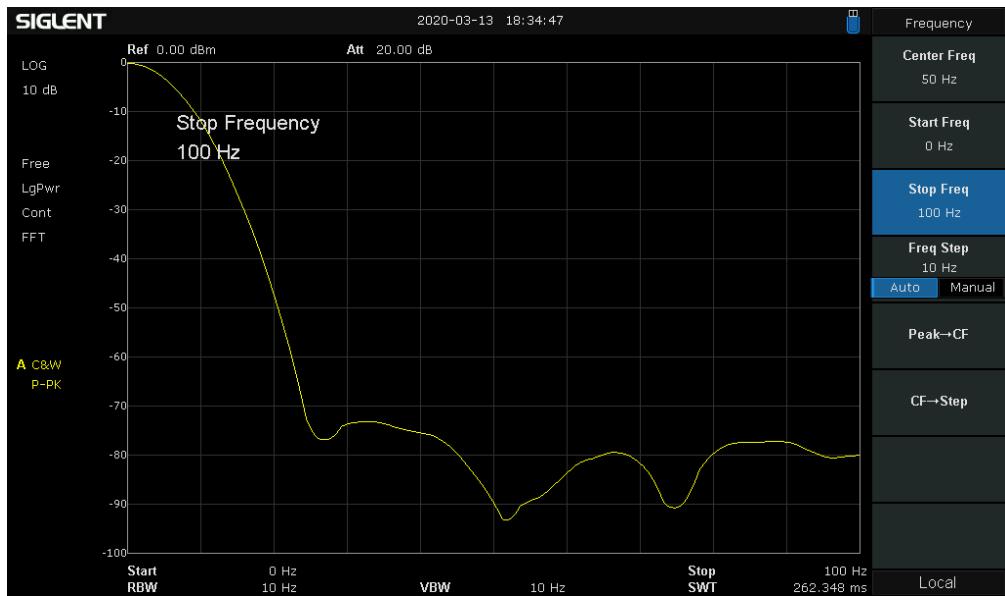


Figure 41: Output with changed C value in the Filter

Discussion:

1. According to the simulations it can be seen that a 230V 50Hz signal can be cut off using the filter.
2. Expected outcome of cutoff of 50Hz didn't come from the planned filter due to the inductance of the transformer. After the modification expected outcome can be taken.

Conclusion:

1. According to the Simulations the 50Hz Domestic signal can be cut off using the filter.
2. Expected outcome of cutoff of 50Hz didn't come from the planned filter due to the inductance of the transformer. After the modification expected outcome can be taken.
3. Modified C and L values were decided to be kept the same for the first step and the filter should be soldered.
4. Pulse transformer with 1:1 ratio must be checked and the C and L values must be calculated in the second step modifications.

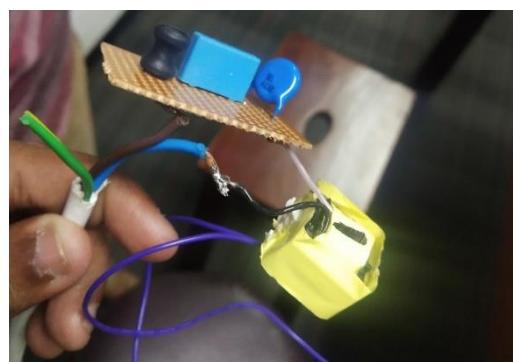


Figure 42: Filter Design

2.2.6 Test 6: Deciding the Optimum Transmission Frequency for Stage 1

Equipment:

- Signal Generator
- Spectrum Analyzer
- Wiring Board
- Transformers (230:12)
- Designed filter
- CD4046
- Capacitors 102
- Converter hilink-5m05
- Dot board
- Variable resistors 20K, 50K

Theory:

For Western Europe, regulations concerning PLC are described in the EN50065 standard, entitled 'Signaling on low-voltage electrical installations in the frequency range 3 kHz to 148.5 kHz.' In this EN-paper, the allowed frequency band and output voltage over power lines are indicated. According to EN 50065.1, the maximum allowed peak voltage for narrowband signals (i.e. a 20 dB bandwidth of less than 5 kHz in width) at 9 kHz equals 5 V, exponentially decreasing to 1 V at 95 kHz and for broadband transmitters (i.e. a 20 dB bandwidth of more than 5 kHz in width) equals 5 V=134 dB (μ V). Roughly speaking, the bandwidth for communication is about 86 kHz and the maximum modulator output voltage is limited to 5 V. These regulations determine to a large extent the development of PLC in Western Europe. [5]

From the restrictions in power and frequency, one can conclude that a simple and robust communication system, taking the mentioned regulations in to consideration, is preferable. In addition, the channel conditions are very often not known at the receiver and sophisticated demodulator features cannot be used effectively. One of the robust modulation schemes is the Spread-Frequency Shift Keying(S-FSK) scheme as introduced by Schaub. Other schemes are Binary Phase Shift Keying (BPSK) or differential BPSK. In addition to the robustness in communications, these simple schemes can also be designed to comply with the local regulations, such as CENELEC, FCC, KN60, etc. Of course, the type of application plays a dominant role. For instance, a meter-reading or load-control system can operate at low data rates, needing a reliable communication channel during a fraction of the time. For these systems often a feedback channel is available, making error detection schemes combined with message repetition very attractive. [6]

Frequency-shift keying (FSK) is a method of transmitting digital signals. The 2 binary states, logic 0 (low) and 1(high), are each represented by an analog waveform. Logic 0 is represented by a wave at a specific frequency, and logic 1 is represented by a wave at a different frequency. A modem converts the binary data from a computer to FSK for transmission over telephone lines, cables, optical fiber, or wireless media. The modem also converts incoming FSK signals to digital low and high states, which the computer can "understand".

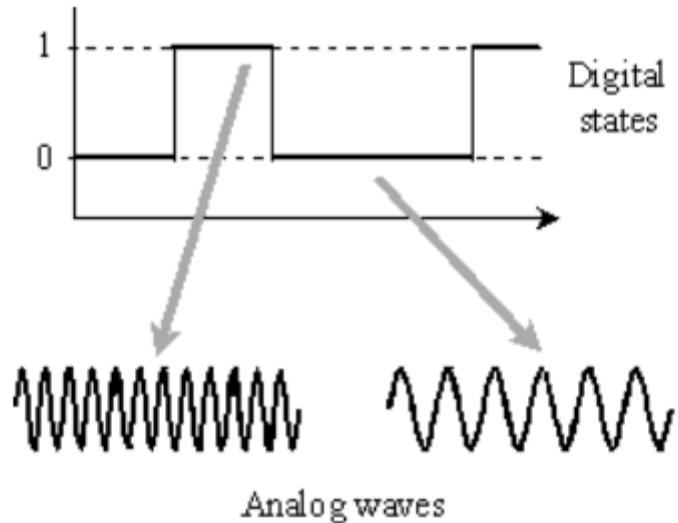


Figure 43: FSK in transmitting digital signal

In narrowband PLC, performance is strongly influenced by signal attenuation, noise disturbances and interference. Attenuation starts with the coupling circuit. Losses due to mismatch of the network impedance to the coupling circuits can lead to an attenuation of 10 dB or more in Signal-to-Noise Ratio (SNR). For reasons of simplicity, assume that coupling losses do not occur. If they do, a correction on the signal input power must be incorporated. Can consider a maximum channel input power (CENELEC) or an average input power, as for Orthogonal Frequency Division Multiplexing (OFDM) modulation. The signal attenuation in the lower frequency band is assumed to be slowly time-varying. The low transmission frequencies (<500 kHz) do not cause standing wave sand thus narrow band fades are unlikely to appear. Signal attenuation due to the network loads can be of the order of 40 to 100 dB per kilometer. The main parameter determining the actual level of signal attenuation is the **number of loads connected to the main line**. As long as loads are evenly distributed over the main line, the relation between signal attenuation and distance can be considered to be approximately exponential. For the power line channel, the received average signal power can be modeled as a function of the distance between transmitter and receiver. [6]

From extensive measurements it follows that the received signal power at distance d (in meters), $S_{re}(d)$ from the transmitter can be approximately written as ,

$$S_{re}(d)=S10^{-kd} \quad [W]$$

Equation 4: Received signal power at distance

Where S is the transmitted power and κ is a constant that expresses the attenuation. A ‘good’ channel has an attenuation of 40dB/km, i.e. $\kappa =0.004$. For a ‘bad’ channel, might have an attenuation of 100 dB/km and thus $\kappa =0.01$. In practical schemes, reliable communication is possible up to a distance of 500 m. Many measurements have been performed to determine the characteristics of the power line channel for frequencies up to 500 kHz; e.g., to the proceedings of the various International Symposia on Power Line Communications(ISPLC) and its Applications.

The average noise power level ranges from -90 dB (W/Hz) at 9 kHz to -125 dB (W/Hz) at 95 kHz. It is worth mentioning that, since noise as well as wanted signals are subject to attenuation, noise sources close to the receiver will have the greatest effect on the received noise structure, particularly when the network attenuation is large. The background noise is assumed to have a PSD on average equal to

$$N_f = 10^{(\gamma - 4.10^{-5}f)} \quad [\text{W/Hz}].$$

Equation 5: PSD on average

The constant γ changes slowly in time and can be estimated from measurements. γ has in approximation a Gaussian distribution with an average $\mu = -8.6$ and standard deviation $\sigma = 0.5$. [7]

Using the data on signal attenuation and background noise, can estimate the distance that can be reached with a reasonable detection error probability of say 10^{-5} .

Table 1: The distance calculated with constant noise PSD N_f .

N_f	Attenuation	
	100 dB/km	40 dB/km
10^{-10} W/Hz	600 m	1500 m
10^{-12} W/Hz	800 m	2000 m

Since the transmission and detection are binary, the transmission efficiency at a detection error rate of 10^{-5} is approximately 1 bit/channel symbol or 12.5 kbit/s.

Generation of signal,

IC waveforms generators (function generators) and IC waveform synthesizers provide several different waveforms or functions at the desired frequency. An IC waveforms synthesizer can generate different waveforms like sine, square, ramp, and triangle. There are many different types of IC waveforms synthesizers. Examples include IC function generators, an IC waveform generator, arbitrary waveform generator, signal generator, and a sweep function generator. [8]

An IC function generator is a versatile device that delivers a choice of different waveforms like sine, square, or triangle.

The different waves can be obtained by selecting the appropriate code of the select pins which is present at the output. An IC waveform generator is an IC around which the waveform generator circuit is build. A waveform generator is available as a bench top instrument, portable, or PC based module. An

arbitrary waveform generator can recreate any waveform at a wide range of amplitudes. A signal generator is used to generate a waveform, signal, testing, and aligning all receivers and transmitters, and also for producing alternating current of desired frequency and amplitude. A sweep function generator generates different waveforms that may be required to measure the frequency response of amplifiers and filters. Other IC waveforms synthesizers are commonly available. [8]

IC found,

1. IC18036
2. XR 2206
3. AD9835 chip
4. CD4046

From the above CD4046 was appropriate for the design because,

1. It could be found in Sri Lanka.
2. It has easier and clear structure.
3. Want to generate 12 Vpp square signal. Without more amplification components could to generate 12 Vpp signal.
4. Can get stable signal output and yet the necessity is to generate 2 signals from different frequencies, a simple structure is used.

The CD4046BC micropower phase-locked loop (PLL) consists of a low power, linear, voltage-controlled oscillator (VCO), a source follower, a Zener diode, and two-phase comparators. The two-phase comparators have a common signal input and a common comparator input. The signal input can be directly coupled for a large voltage signal, or capacitively coupled to the self-biasing amplifier at the signal input for a small voltage signal. [8]

Phase comparator I, an exclusive OR gate, provides a digital error signal (phase comp. I Out) and maintains 90° phase shifts at the VCO center frequency.

Between signal input and comparator input (**both at 50% duty cycle**), it may lock onto the signal input frequencies that are close to harmonics of the VCO center frequency.

Phase comparator II is an edge-controlled digital memory network. It provides a digital error signal (phase comp. II Out) and lock-in signal (phase pulses) to indicate a locked condition and maintains a 0° phase shift between signal input and comparator input.

The linear voltage-controlled oscillator (VCO) produces an output signal (VCO Out) whose frequency is determined by the voltage at the VCOIN input, and the capacitor and resistors connected to pin C1A, C1B, R1 and R2. The source follower output of the VCOIN (demodulator out) is used with an external resistor of 10 kΩ or more.

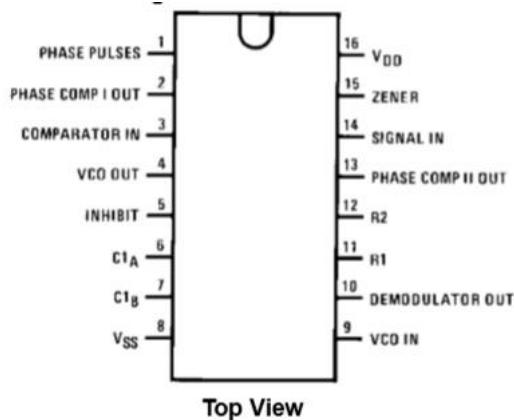


Figure 44: Pin assignment of CD4046

The INHIBIT input, when high, disables the VCO and source follower to minimize standby power consumption. The Zener diode is provided for power supply regulation, if necessary.

Features

1. Wide supply voltage range: 3.0V to 18V
2. Low dynamic power consumption: 70 μ W (typ.) at $f_0 = 10$ kHz, $VDD = 5V$
3. VCO frequency: 1.3 MHz (typ.) at $VDD = 10V$
4. Low frequency drift: 0.06%/°C at $VDD = 10V$ with temperature
5. High VCO linearity: 1% (typ.)

Applications

1. FM demodulator and modulator.
2. Frequency synthesis and multiplication.
3. Frequency discrimination.
4. Data synchronization and conditioning.
5. Voltage-to-frequency conversion.
6. Tone decoding.
7. **FSK modulation.**
8. Motor speed control

Block diagram,

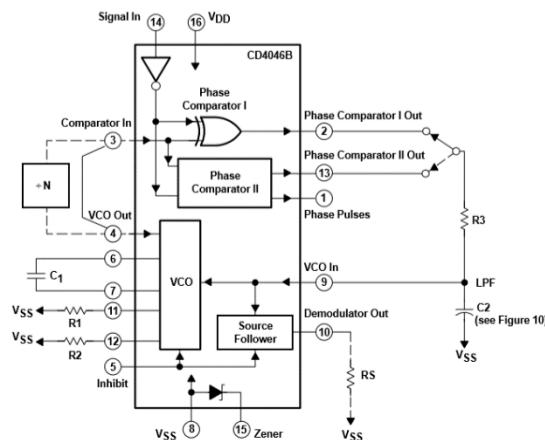


Figure 45: Block diagram

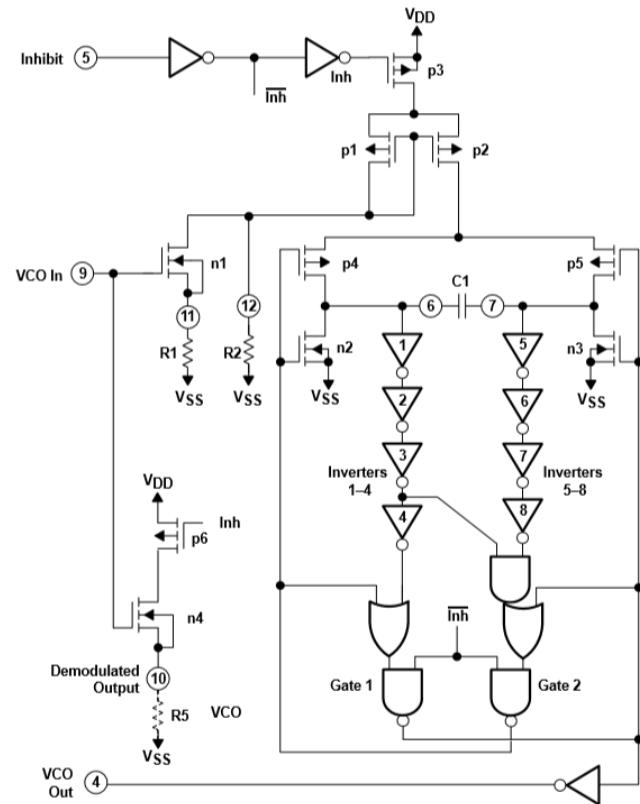


Figure 46: CD4046 VCO section schematic

Table 2: Maximum and recommended rating conditions of CD4046 operation

	Absolute Maximum ratings	Recommended operation conditions
DC Supply Voltage (VDD)	-0.5 to +18 VDC	3 to 15 VDC
Input Voltage (VIN)	-0.5 to VDD +0.5 VDC	0 to VDD VDC
Storage Temperature Range (TS)	-65°C to +150°C	-40°C to +85°C
Power Dissipation (PD) Dual-In-Line small outline	700 mW 500 mW	
Lead Temperature (TL) (Soldering, 10 seconds)	260 °C	

Voltage -controlled oscillator (VCO),

The VCO circuit shown in Figure 44 operates as follows; when the inhibit input is low, p3 is turned full on, effectively connecting the sources of p1 and p2 to VDD, and gates 1 and 2 are permitted to function as NOR-gate flip-flops. n1 and external resistor R1 form a source-follower configuration.

As long as the resistance of R1 is at least an order of magnitude greater than the on resistance of n1 (greater than $10\text{ k}\Omega$), current through R1 is linearly dependent on the VCO input voltage. This current flows through p1, which, together with p2, forms a current-mirror network. External resistor R2 adds an additional constant current through p1; this current offset the VCO operating frequency for VCO input signals of 0 volts. [8]

In the current-mirror network, the current of p2 is effectively equal to the current through p1, independent of the drain voltage at p2. (This condition is true, provided p2 is maintained in saturation. In the circuit in Figure 8, p2 is saturated under all possible operating conditions and modes.)

The set/reset flip-flop composed of gates 1 and 2 turns on either p4 and n3 or p5 and n2. One side of external capacitor C1 is, therefore, held at ground, while the other side is charged by the constant current supplied by p2. As soon as C1 charges to the point at which the transfer point of inverters 1 or 5 is reached, the flip-flop changes state. [8]

The charged side of the capacitor now is pulled to ground. The other side of the capacitor goes negative and discharges rapidly through the drain diode of the off-n device. Subsequently, a new half cycle starts. Because inverters 1 and 5 have the same transfer points, the VCO has a 50% duty cycle. Inverters 1–4 and 5–8 serve several purposes:

- Shape the slow-input ramp from capacitor C1 to a fast waveform at the flip-flop input stage
- Maintain low power dissipation through the use of high-impedance devices at inverters 1 and 5 (slow-input waveforms)
- Provide four inverter delays before removal of the set/reset flip-flop triggering pulse to ensure proper switching action

In order not to load the LPF, a source-follower output of the VCO input voltage is provided (demodulated output). If this output is used, a load resistor (R_s) of $10\text{ k}\Omega$, or more, should be connected from this terminal to ground. If unused, this terminal should be left open. A logic 0 on the inhibit input enables the VCO and the source follower, while a logic 1 turns off the VCO and source follower to minimize standby power consumption. [8]

Circuit diagram was as follow,

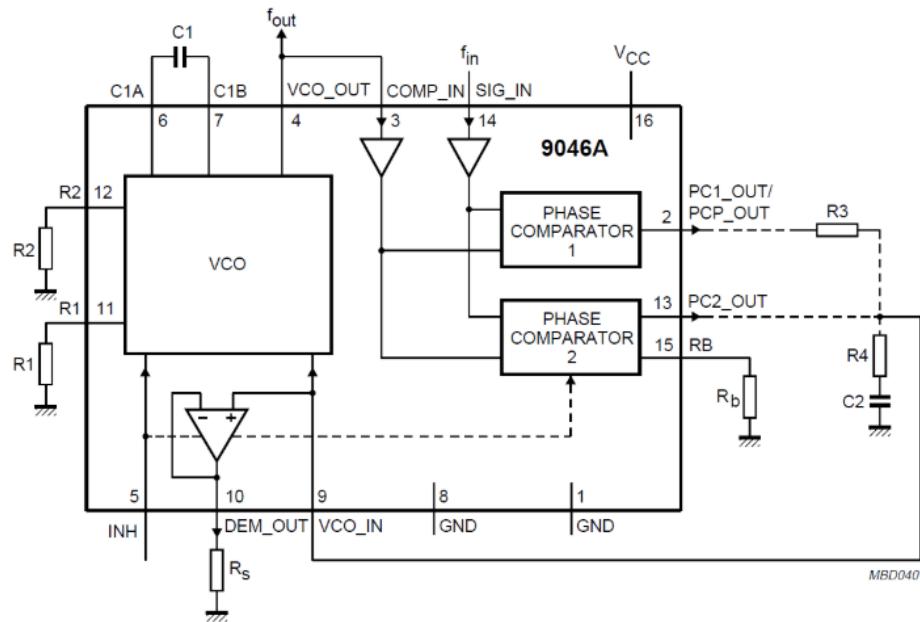


Figure 47: Block diagram of CD4046

Calculation must be done for the proposed frequency according to the following equation,

$$f_c \approx \pm \left(\frac{1}{2\pi} \right) \left(\frac{2\pi f_1}{R_3 C_2} \right) = \pm 0.4 \text{ kHz}$$

Equation 6; Frequency Calculation

As can be seen from the previous tests for the first stage modulation and coding aspects for narrowband (low speed) transmission in the frequency bands up to 500 kHz has to be considered.

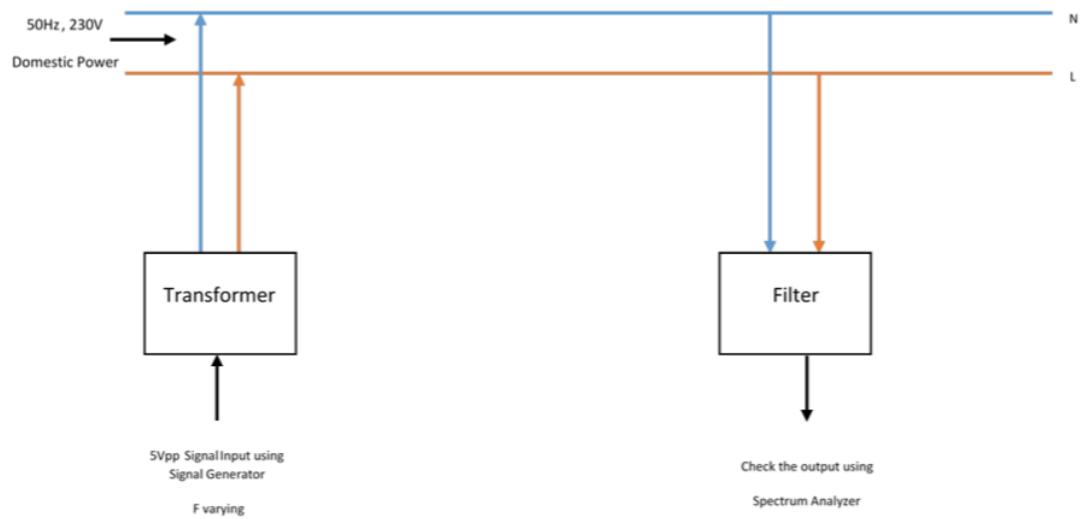


Figure 48: Test arraignment

Procedure:

1. Circuit arraignment was set accordingly.
2. 5Vpp input signal was given using the signal generator through the transformer varying the frequency.
3. Frequency was set to 100 kHz, 300 kHz and 500 kHz and the output from filter was observed using the spectrum analyzer.
4. Input signal frequency was varied to find the frequency that gives the maximum gain.

Calculations:

Calculation can be done using an online frequency calculator. [9]

The screenshot shows an online calculator interface for frequency calculations. The calculator has a light blue header with a calculator icon. The input fields are on the left, and the results are on the right. The results are color-coded in orange for the first two, black for the next two, and orange for the last two.

R1 [kΩ]	10.451	3 kΩ < R1 < 300 kΩ
R2 [kΩ]	10.2	3 kΩ < R2 < 300 kΩ
C1 [pF]	2000	40 pF < C
FREQ.MIN [kHz]	494.885	$V_{TUN} = 1.1 \text{ V}$
FREQ.TYP [kHz]	617.781	$V_{TUN} = 2.5 \text{ V}$
FREQ.MAX [kHz]	800.164	$V_{TUN} = 3.9 \text{ V}$
K_{VCO}	109.028	kHz/V

CALCULATE

Figure 49: calculating the center frequency by above link

Observations:

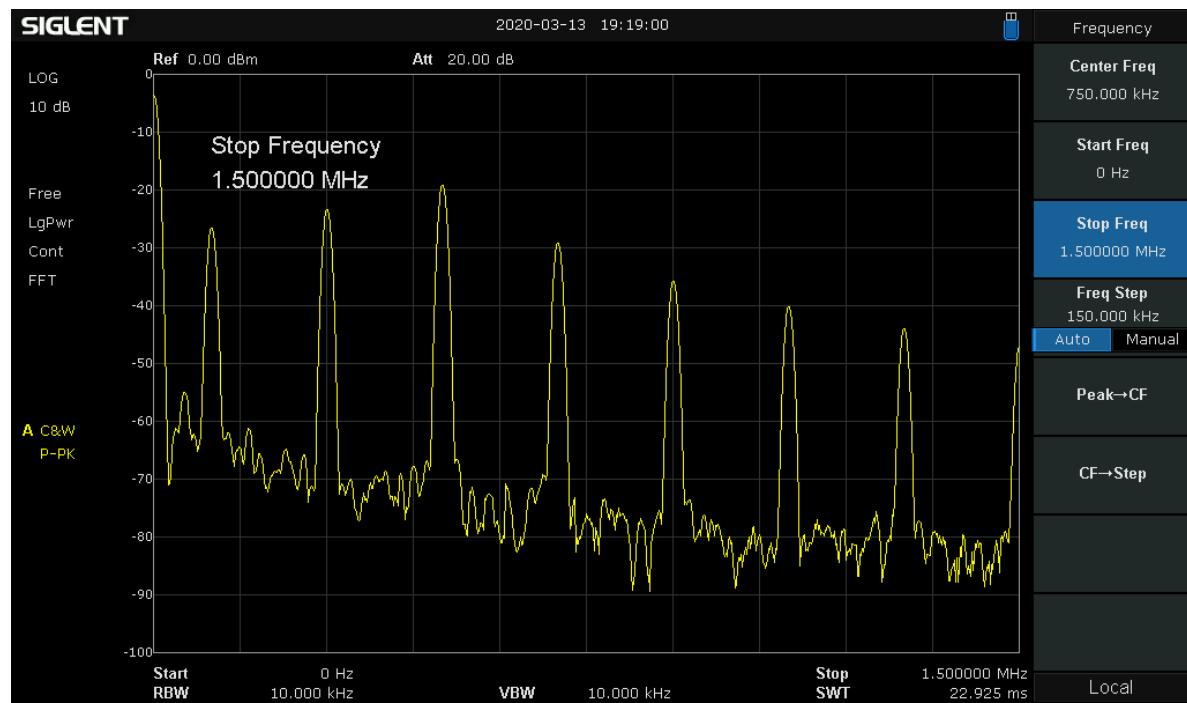


Figure 50: Output from filter for 100 kHz

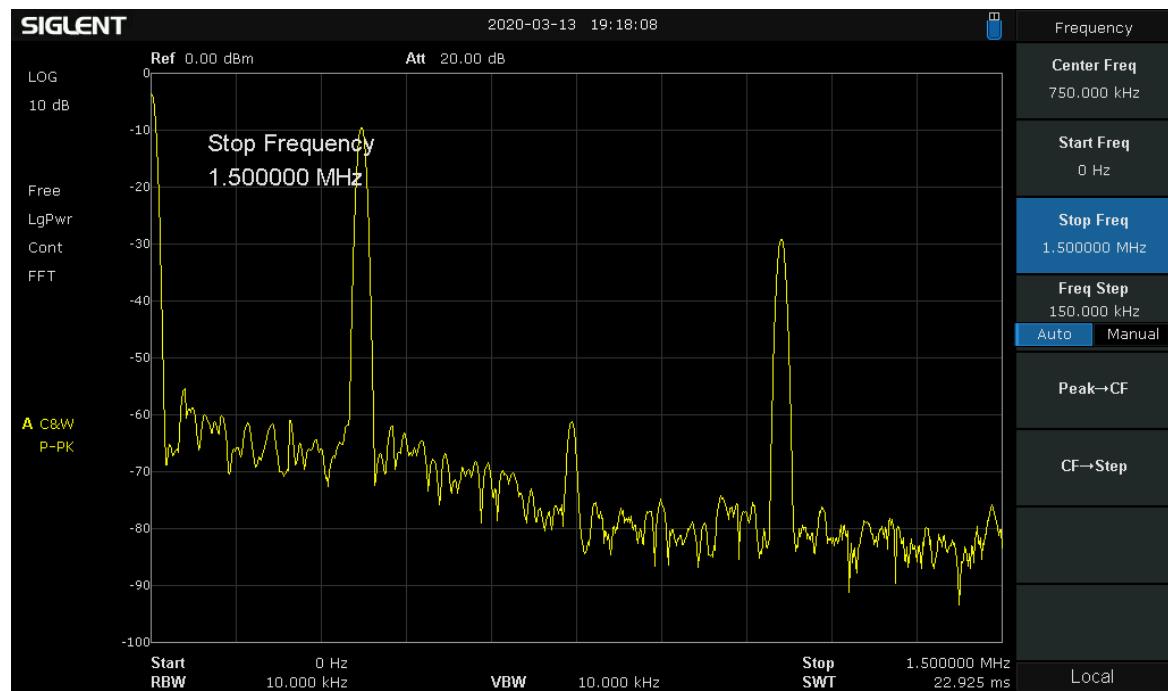


Figure 51: Output from filter for 300 kHz

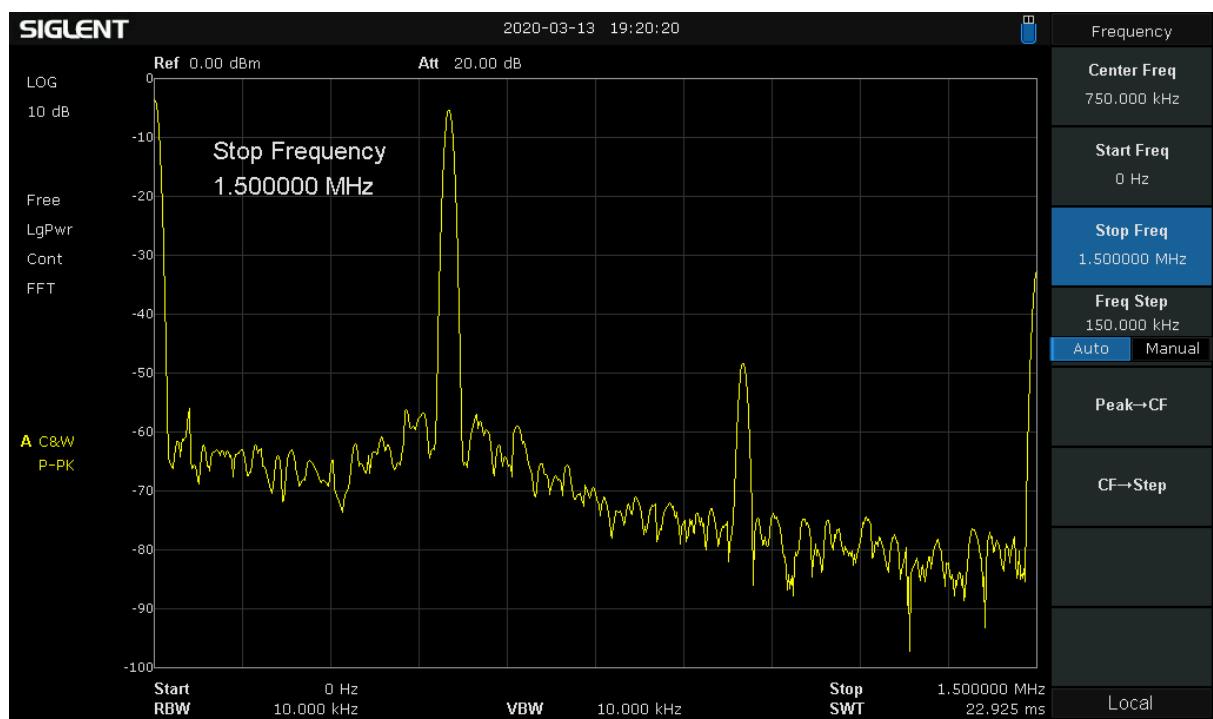


Figure 52: Output from filter for 500 kHz

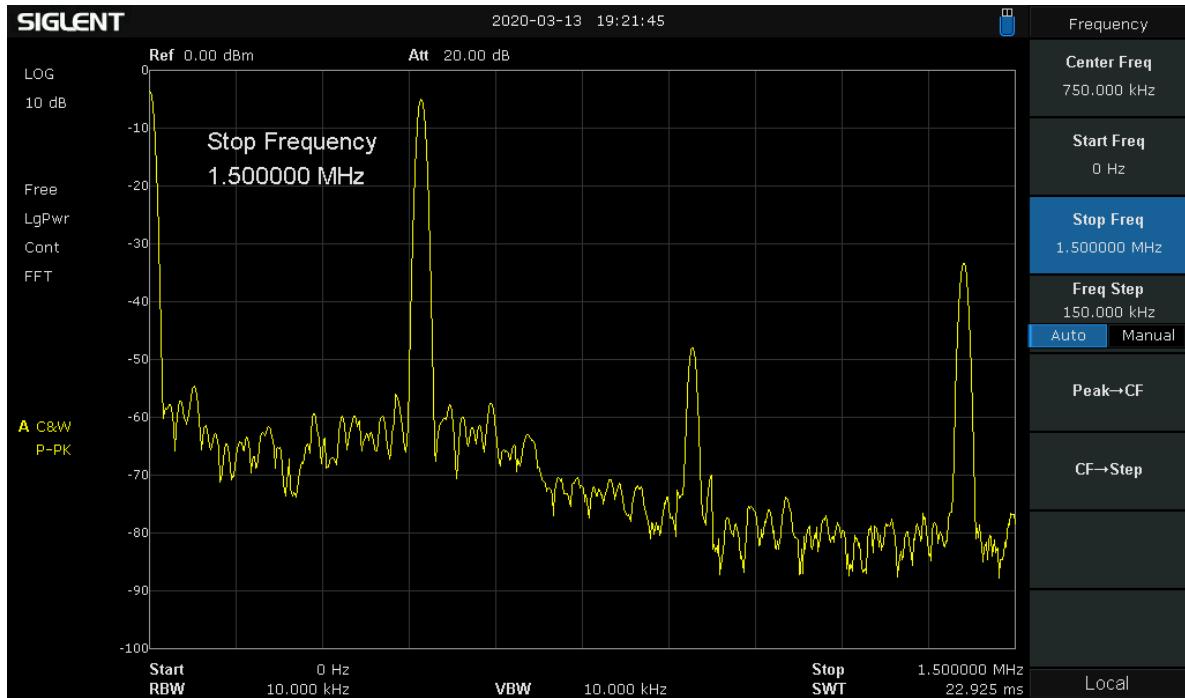


Figure 53: Output from filter for 470 kHz - Max Gain

Discussion:

1. Irrespective of the regulations range of 300 kHz – 500 kHz must be used for the Stage 1 due to the components that can be found.
2. The optimum frequency to send in the range of 300 kHz – 500 kHz can be found as 470 kHz.
3. When using the Signal Generator harmonics of the input signal can be seen in the output.
4. A Supply Voltage of 5 V is assumed. Changes affects the Frequencies

Conclusion:

1. A Supply Voltage can be set to 5 V.
2. For R1, R2, Rs 50K ohm resistors can be used in order to change the frequency accordingly to 470kHz
3. The circuit should be design as schematic below.
4. Further study on harmonics must be done and clarify whether the IC CD4046 generates harmonics when used as the input.

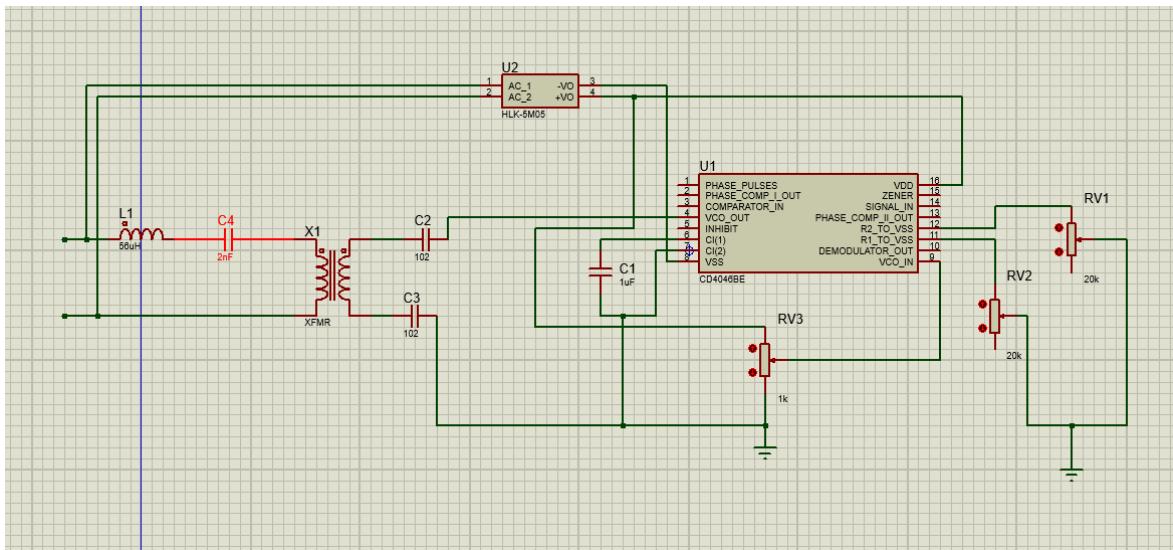


Figure 54: Circuit Schematic for the signal transmitter

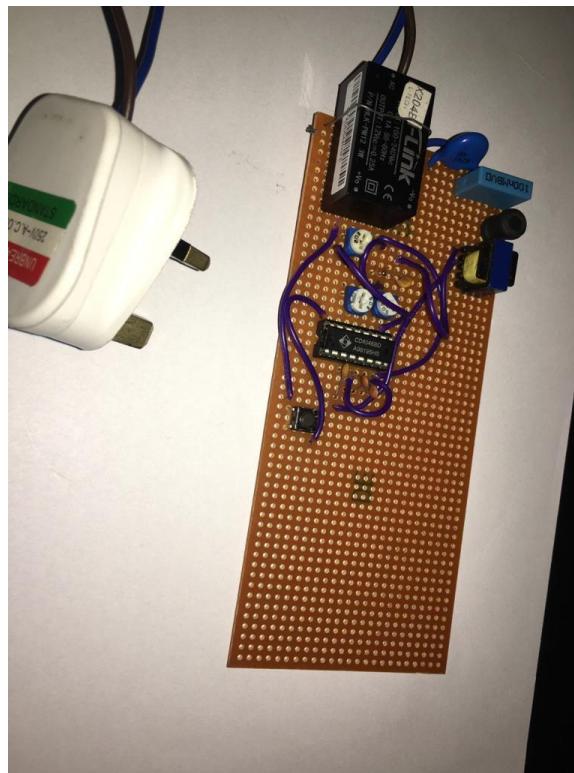


Figure 55: Designed Signal Transmitter circuit

2.2.7 Test 7: Taking measures for voltage drop

Equipment:

- Designed signal transmitter circuit
- TIP120 Transistor [10]
- Spectrum Analyzer

Theory:

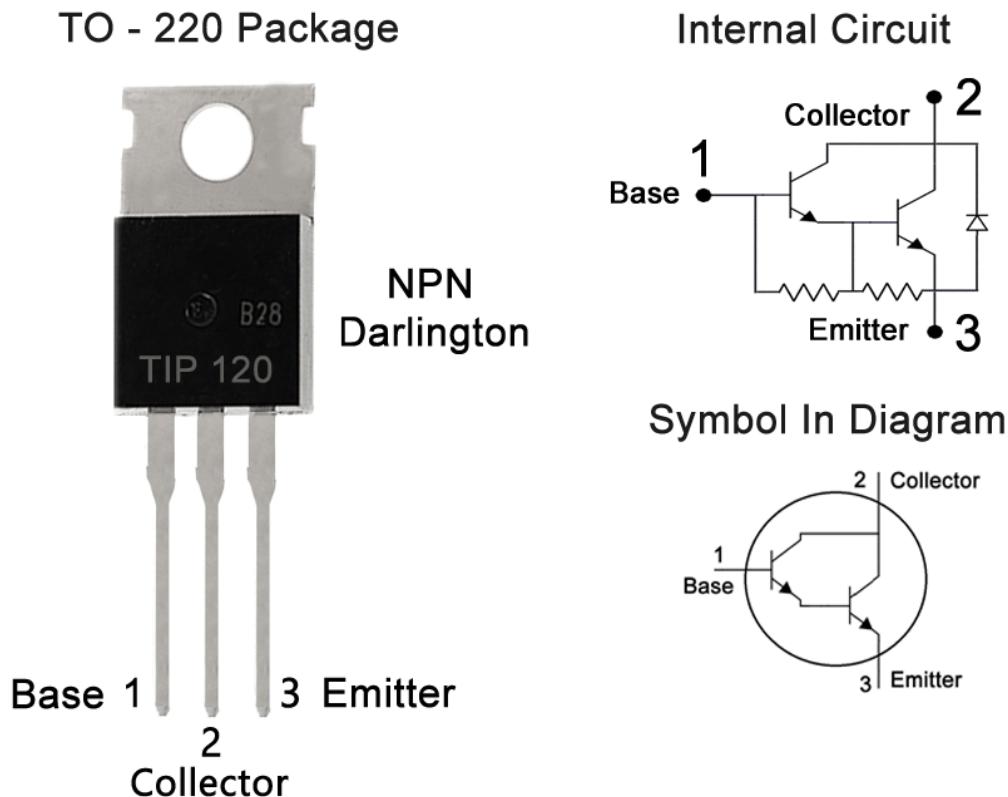


Figure 56: TIP120 Transistor Pin out

Symbol	Parameter	Ratings	Units
V_{CBO}	Collector-Base Voltage : TIP120 : TIP121 : TIP122	60 80 100	V
V_{CEO}	Collector-Emitter Voltage : TIP120 : TIP121 : TIP122	60 80 100	V
V_{EBO}	Emitter-Base Voltage	5	V
I_C	Collector Current (DC)	5	A
I_{CP}	Collector Current (Pulse)	8	A
I_B	Base Current (DC)	120	mA
P_C	Collector Dissipation ($T_a=25^\circ\text{C}$) Collector Dissipation ($T_C=25^\circ\text{C}$)	2 65	W
T_J	Junction Temperature	150	$^\circ\text{C}$
T_{STG}	Storage Temperature	- 65 ~ 150	$^\circ\text{C}$

Figure 57: Absolute maximum ratings of TIP120

Procedure:

1. TIP120 Transistor was included to the Signal Transmitter circuit.
2. Output from the Signal Transmitter IC was checked using the spectrum analyzer.
3. Output from the Signal Transmitter Circuit before the Filter was checked using the spectrum analyzer.
4. Output from the Signal Transmitter Circuit after the Filter was checked using the spectrum analyzer.

Discussion:

1. As a result of the attenuation receiver could to detect the exact signal as the gain about is same as the noise. So, the phase detector couldn't to select the relevant frequency.
2. So, it was a need in transmitter side to transmit a high gain signal. So increased the value of V_{pp}. Selection of CD4046 as it able to get 15 V_{pp} square wave signal. But here get only 12 V as the converter turns 230 V to 12 V.
3. To the working process of the filter added before the transformer coupler, couldn't add a resistor parallel to the circuit. It may cause the half process of filtering. Later planned to add an appropriate resistor.
4. Micro controller has switch 12 V supply by 5V output. Use of a transistor TIP120 done this switching purpose.

Observations:

1. Voltage of output of the signal generator is lower than 5V_{pp} and this is not enough to give a good Gain at the receiver end.

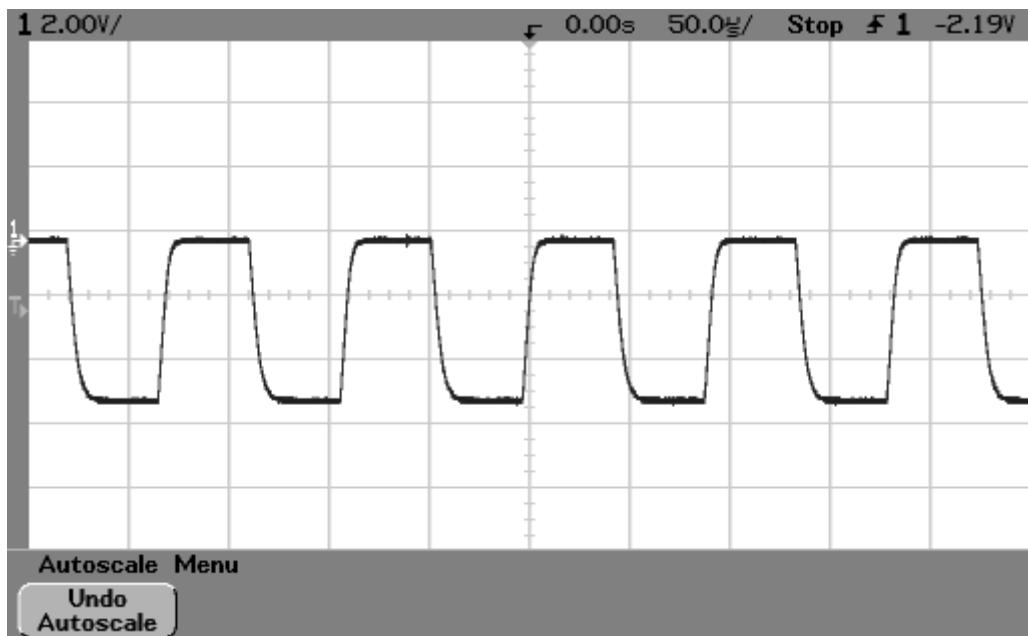


Figure 58: Output from the Signal generator IC CD4046

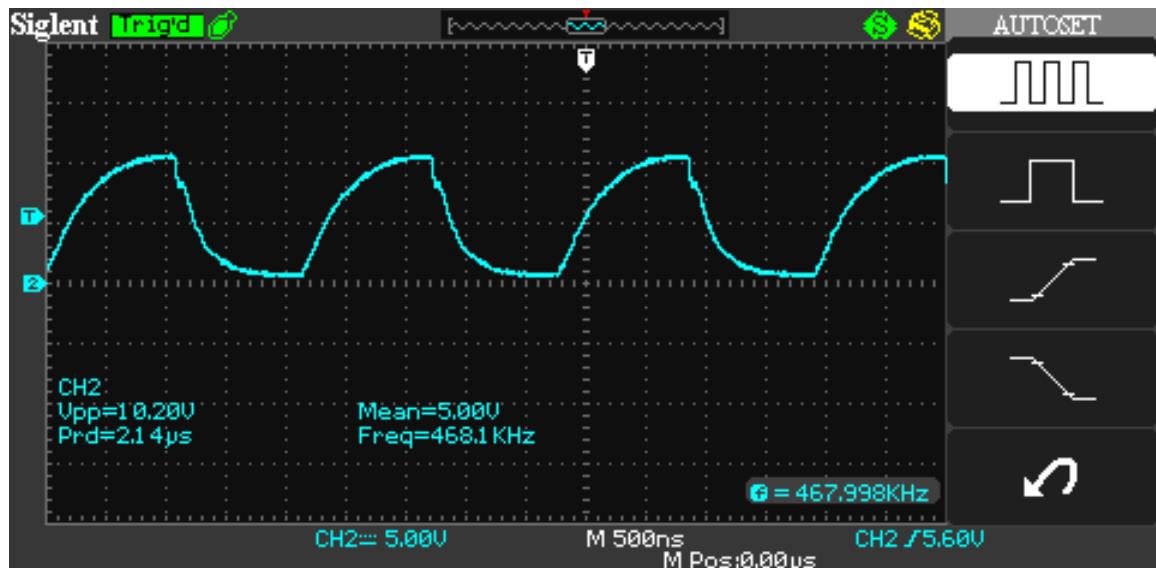


Figure 59: Output from the Signal Transmitter Circuit before the Filter

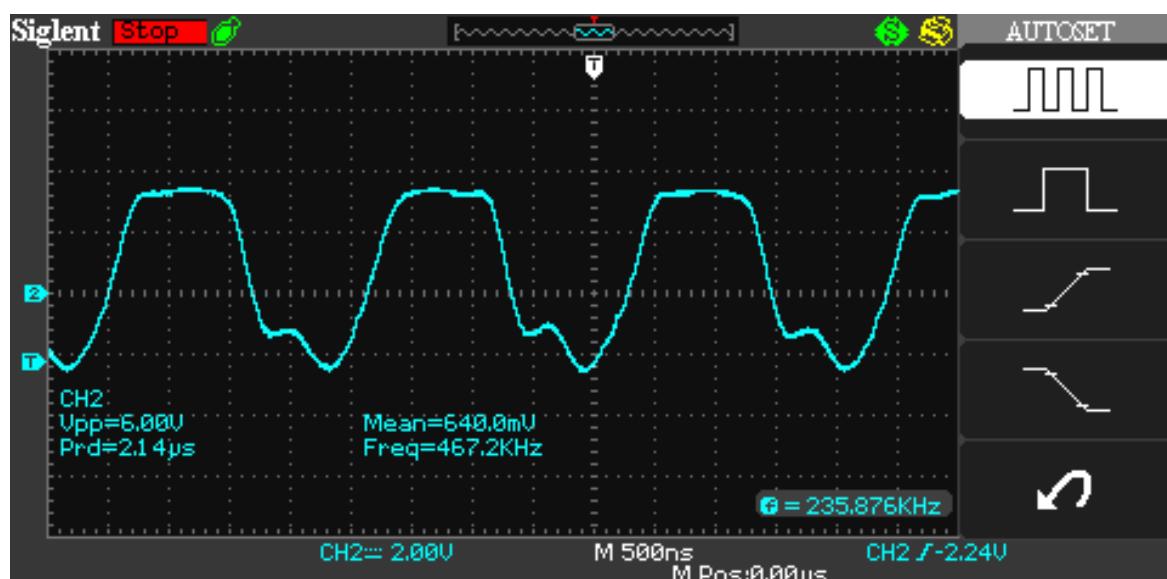


Figure 60: Output from the Signal Transmitter Circuit after the Filter

Conclusion:

1. Addition 12v must be done instead of 5v for that TIP120 can be used.
2. Capacitors C1 and C2 in the below schematic in figure 56 to be placed to remove the DC off set from the transmission line. Direct connection causes the destruction of IC.

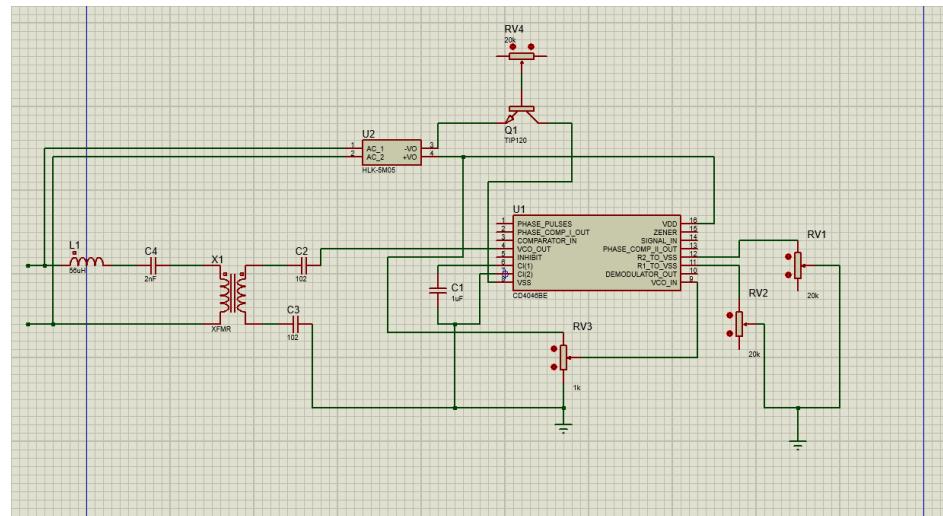


Figure 61: Designed signal generator circuit schematic with TIP120

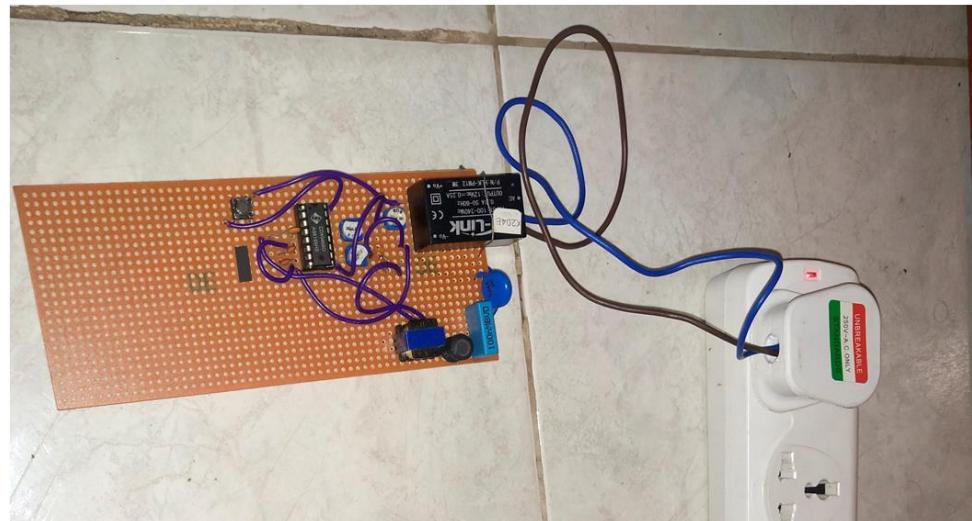


Figure 62: Designed signal generator circuit with TIP120

2.2.8 Test 8: Receiver Designing

Equipment:

- Designed Filter
- Capacitors 102
- Converter hilink-5m05
- IC – LM567
- Dot board
- Variable resistors 20K, 50K

Theory:

Signal transmitted from transmitter should identify by the receiver side to get the bit pattern.

Major concern in the receiver side is the attenuation amount of the signal. If the signal attenuation beyond the limit the receiver couldn't to identify the signal.

Considering gain of the received signal it should be above 30 dB level, if not receiver couldn't to filter the signal from noise.

One of the classical problems in information and communication theory is the determination of the maximum amount of reliable information that can be transmitted over an unreliable channel. This maximum amount is called the channel capacity.

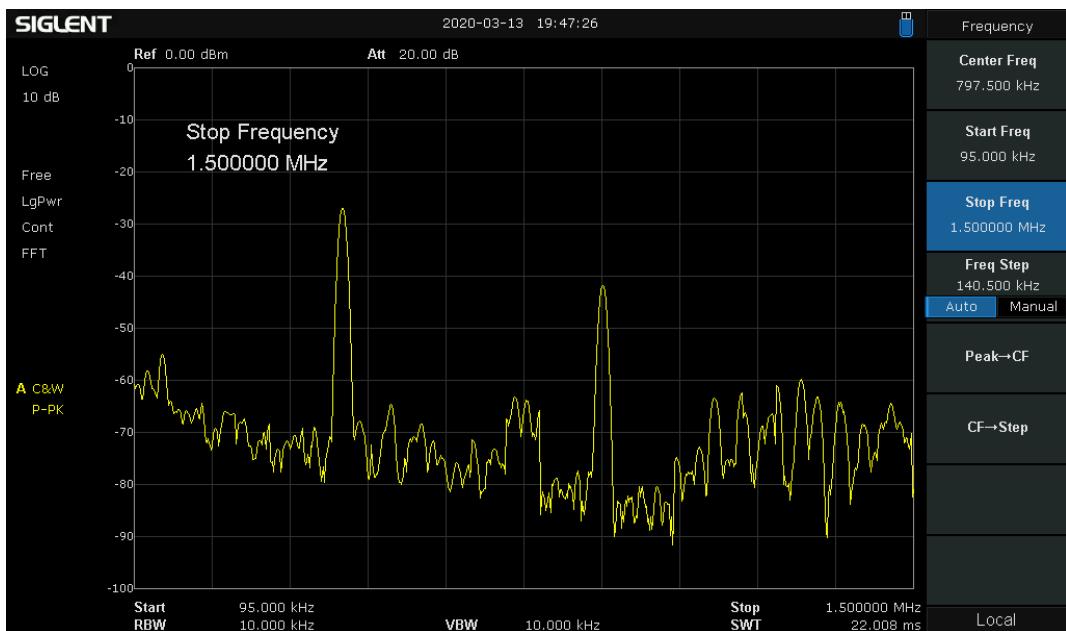


Figure 63: Various gains for different signals of Vpp

NE/SE 567 was used as the detection component of the signal. This IC is a tone decoder as well as this includes phase locked loop.

In Sri Lanka the component can be found easily, with low price and having a simple structure of design.

The NE/SE567 tone and frequency decoder is a highly stable phase-locked loop with synchronous AM lock detection and power output circuitry. **Its primary function is to drive a load whenever a sustained frequency within its detection band is present at the self-biased input.** The bandwidth center frequency and output delay are independently determined by means of four external components. [11]

Features,

1. Wide frequency range (.01Hz to 500kHz).
2. High stability of center frequency.
3. Independently controllable bandwidth (up to 14%).
4. High out-band signal and noise rejection.
5. Logic-compatible output with 100mA current sinking capability.
6. Inherent immunity to false signals.
7. Frequency adjustment over a 20-to-1 range with an external resistor.
8. Military processing available.

Applications,

1. Touch-Tone decoding
2. Carrier current remote controls
3. Ultrasonic controls (Remote TV, etc.)
4. Communications paging
5. Frequency monitoring and control
6. Wireless intercom
7. Precision oscillator

Pin configurations,

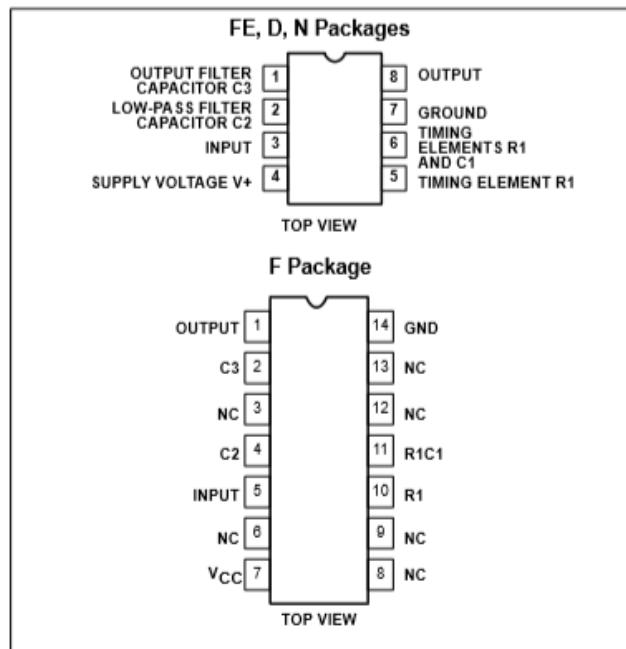


Figure 64: Pin configurations of LM567

There are 2 types. Here FE, D or N package IC was used.

Block diagram,

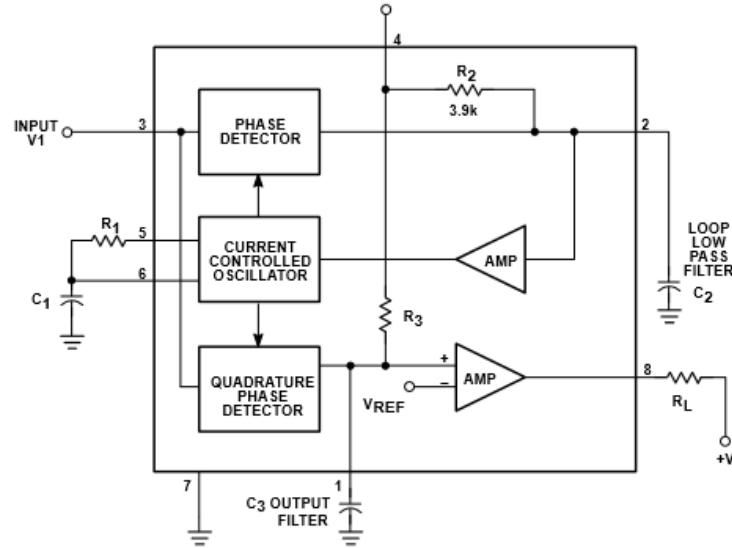


Figure 65: Block diagram of LM567

Design formula,

Phase-locked loop terminology center frequency (f_0)

The free-running frequency of the current controlled oscillator (CCO) in the absence of an input signal.

$$f_0 = \frac{1}{1.1R_1 C_1}$$

Equation 7: Design formula for center frequency

Detection Bandwidth (BW),

The frequency range, centered about f_0 , within which an input signal above the threshold voltage (typically 20mVRMS) will cause a logical zero state on the output. The detection bandwidth corresponds to the loop capture range.

Can introduce a bandwidth for the detection as the transmitted signal frequency will change in some small percentage. [11]

$$BW = 1070 \frac{V_I}{f_0 C_2} \text{ in \% of } f_0$$

$$V_I = 200 \text{ mV}_{\text{RMS}}$$

Where

V_I =Input voltage (V_{RMS})

C_2 =Low-pass filter capacitor (μF)

Equation 8: Detection Bandwidth

For the components refer the following Figure 62,

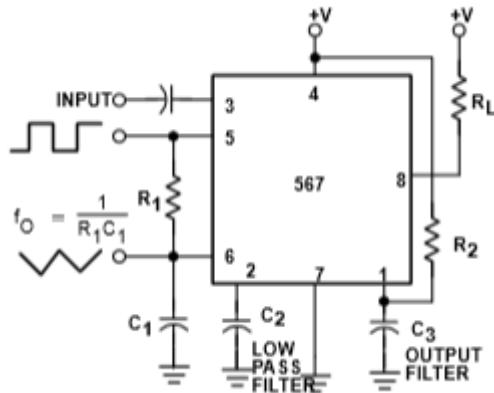


Figure 66: Component setup for 567

Lock Range,

The largest frequency range within which an input signal above the threshold voltage will hold a logical zero state on the output.

Detection Band Skew,

A measure of how well the detection band is centered about the center frequency, f_0 . The skew is defined as $(f_{MAX} + f_{MIN} - 2f_0) / 2f_0$ where f_{MAX} and f_{MIN} are the frequencies corresponding to the edges of the detection band. The skew can be reduced to zero if necessary by means of an optional centering adjustment. [11]

Operating Instructions,

Above figure shows a typical connection diagram for the 567. For most applications, the following three-step procedure will be sufficient for choosing the external components R1, C1, C2 and C3.

1. Select R1 and C1 for the desired center frequency. For best temperature stability, R1 should be between 2K and 20K ohm, and the combined temperature coefficient of the R1C1 product should have sufficient stability over the projected temperature range to meet the necessary requirements.
2. Select the low-pass capacitor, C2, by referring to the Bandwidth versus Input Signal Amplitude graph. If the input amplitude Variation is known, the appropriate value of $f_0 \cdot C2$ necessary to give the desired bandwidth may be found. Conversely, an area of operation may be selected on this graph and the input level and C2 may be adjusted accordingly. For example, constant bandwidth operation requires that input amplitude be above 200mVRMS. The bandwidth, as noted on the graph, is then controlled solely by the $f_0 \cdot C2$ product (f_0 (Hz), $C2$ (μ F)).
3. The value of C3 is generally non-critical. C3 sets the band edge of a low-pass filter which attenuates frequencies outside the detection band to eliminate spurious outputs. If C3 is too small, frequencies just outside the detection band will switch the output stage on and off at the beat frequency, or the output may pulse on and off during the turn-on transient. If C3 is too large, turn-on and turn-off of the output stage will be delayed until the voltage on C3 passes the threshold voltage. (Such delay may be desirable to avoid spurious outputs due to transient frequencies.) A typical minimum value for C3 is $2C2$.
4. Optional resistor R2 sets the threshold for the largest “no output” input voltage. A value of $130k\Omega$ is used to assure the tested limit of 10mVRMS min. This resistor can be referenced to ground for

increased sensitivity. The explanation can be found in the “optional controls” section which follows. [11]

Available Outputs,

The primary output is the uncommitted output transistor collector, Pin 8. When an in-band input signal is present, this transistor saturates; its collector voltage being less than 1.0 volt (typically 0.6V) at full output current (100mA). The voltage at Pin 2 is the phase detector output which is a linear function of frequency over the range of 0.95 to 1.05 f_0 with a slope of about 20mV per percent of frequency deviation. The average voltage at Pin 1 is, during lock, a function of the in-band input amplitude in accordance with the transfer characteristic given. Pin 5 is the controlled oscillator square wave output of magnitude $(+V - 2V_{BE}) \cong (+V - 1.4V)$ having a DC average of $+V/2$. A $1k\Omega$ load may be driven from pin 5. Pin 6 is an exponential triangle of $1V_{p-p}$ with an average DC level of $+V/2$. Only high impedance loads may be connected to pin 6 without affecting the CCO duty cycle or temperature stability.

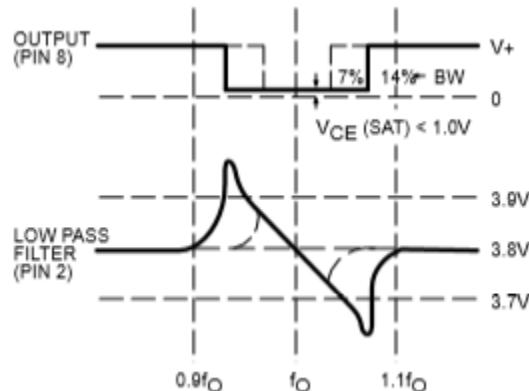


Figure 67: Typical output response

Operating precautions,

1. Operation in the high input level mode (above 200mV) will free the user from bandwidth variations due to changes in the in-band signal amplitude. The input stage is now limiting, however, so that out-band signals or high noise levels can cause an apparent bandwidth reduction as the in band signal is suppressed. Also, the limiting action will create in-band components from sub-harmonic signals, so the 567 becomes sensitive to signals at $f_0/3$, $f_0/5$, etc.
2. The 567 will lock onto signals near $(2n+1) f_0$, and will give an output for signals near $(4n+1) f_0$ where $n=0, 1, 2$, etc. Thus, signals at $5f_0$ and $9f_0$ can cause an unwanted output. If such signals are anticipated, they should be attenuated before reaching the 567 input.
3. Maximum immunity from noise and out-band signals is afforded in the low input level (below 200mVRMS) and reduced bandwidth operating mode. However, decreased loop damping causes the worst-case lock-up time to increase, as shown by the Greatest Number of Cycles before Output vs Bandwidth graph.
4. Due to the high switching speeds (20ns) associated with 567 operation, care should be taken in lead routing. Lead lengths should be kept to a minimum. The power supply should be adequately bypassed close to the 567 with a $0.01\mu F$ or greater capacitor; grounding paths should be carefully

chosen to avoid ground loops and unwanted voltage variations. Another factor which must be considered is the effect of load energization on the power supply. For example, an incandescent lamp typically draws 10 times rated current at turn-on. This can be somewhat greater when the output stage is made less sensitive, rejection of third harmonics or in-band harmonics (of lower frequency signals) is also improved. Cause supply voltage fluctuations which could, for example, shift the detection band of narrow-band systems sufficiently to cause momentary loss of lock. The result is a low-frequency oscillation into and out of lock. Such effects can be prevented by supplying heavy load currents from a separate supply or increasing the supply filter capacitor. [11]

Minimum speed of operation,

Lock-up time is related to the natural frequency of the loop. The lower it is, the longer becomes the turn-on transient. Thus, maximum operating speed is obtained when C2 is at a minimum. When the signal is first applied, the phase may be such as to initially drive the controlled oscillator away from the incoming frequency rather than toward it. Under this condition, which is of course unpredictable, the lock-up transient is at its worst and the theoretical minimum lock-up time is not achievable. Must simply wait for the transient to die out.

The following expressions give the values of C2 and C3 which allow highest operating speeds for various band center frequencies. The minimum rate at which digital information may be detected without information loss due to the turn-on transient or output chatter is about 10 cycles per bit, corresponding to an information transfer rate of $f_0/10$ baud.

Sensitivity adjustment,

When operated as a very narrow-band detector (less than 8 percent), both C2 and C3 are made quite large in order to improve noise and out-band signal rejection. This will inevitably slow the response time. If, however, the output stage is biased closer to the threshold level, the turn-on time can be improved. This is accomplished by drawing additional current to terminal 1. Under this condition, the 567 will also give an output for lower-level signals (10mV or lower).

By adding current to terminal 1, the output stage is biased further away from the threshold voltage. This is most useful when, to obtain maximum operating speed, C2 and C3 are made very small. Normally, frequencies just outside the detection band could cause false outputs under this condition. By desensitizing the output stage, the out-band beat notes do not feed through to the output stage.

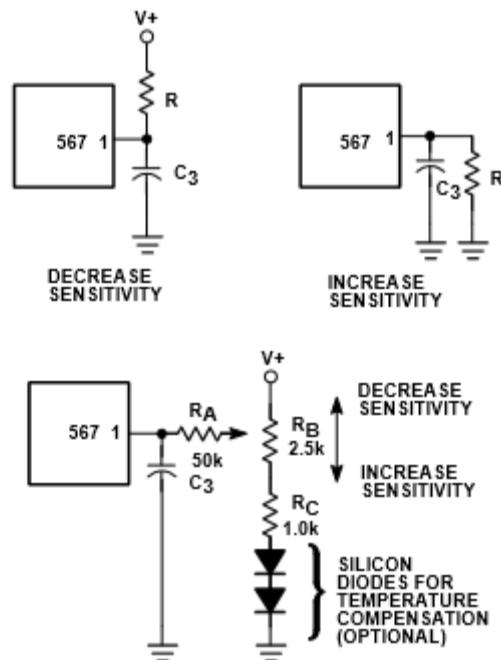


Figure 68: Sensitivity adjust

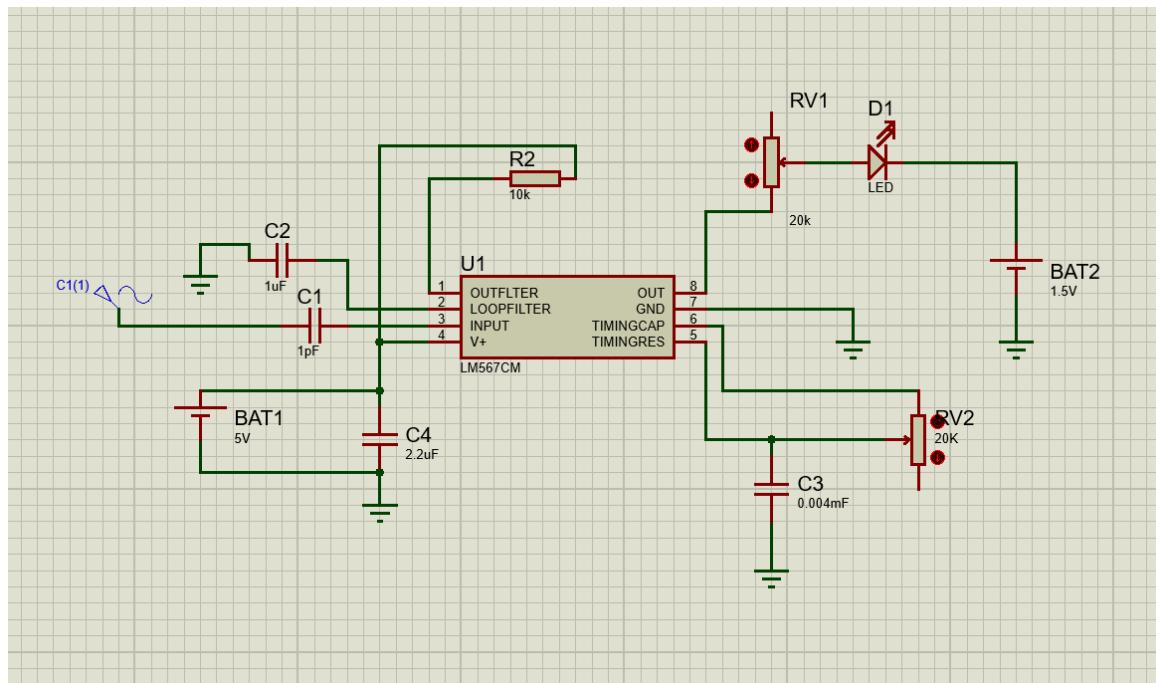


Figure 69: Designed schematic of the Signal receiver

Procedure:

1. IC – LM567 was set according to the data sheet.
 2. The variable resistors were set in the level of identification of the 470 kHz Signal.
 3. The illumination of the LED bulb was observed while sending the signal from the signal generator.
 4. The illumination of the LED bulb was observed while sending the signal from the designed signal transmitter.

Calculations:

Calculations were done using the online calculator. [12]

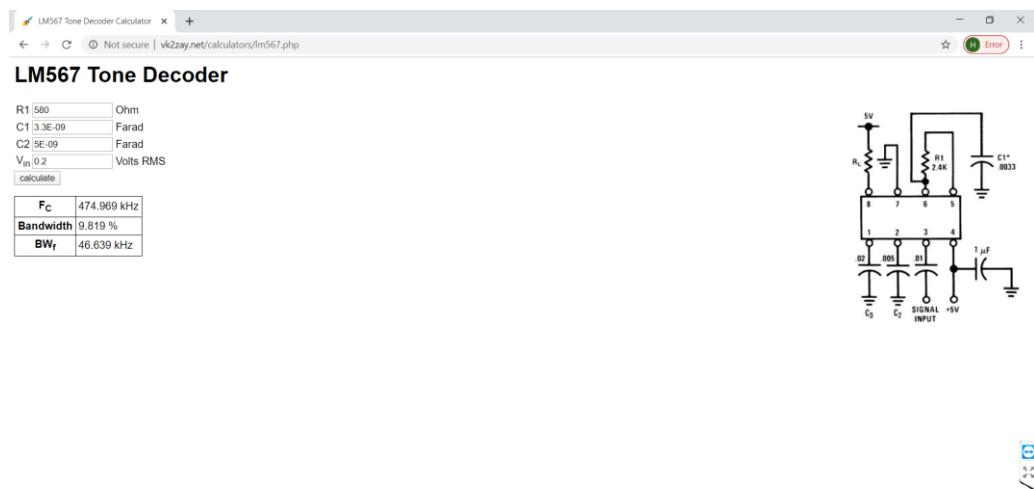


Figure 70: LM567 Online Calculator

Observations:

- ## 1. LED bulb is blinking in low illumination

Conclusion:

1. Addition 12v must be done between the LED instead of 5v for that TIP120 can be used.
 2. Calculated values of Capacitors and Resistors were decided to be set according to the schematic shown in figure 64.
 3. For Cutting off the 50Hz domestic power input, the designed filter was included to the circuit according to the schematic in Figure 67.

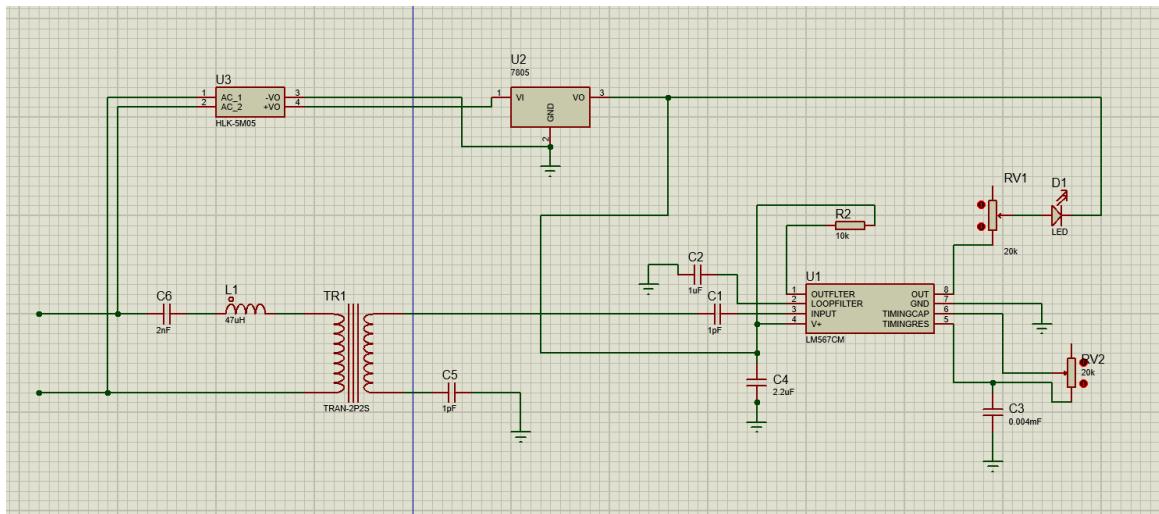


Figure 71: Designed schematic of the Signal receiver with the filter

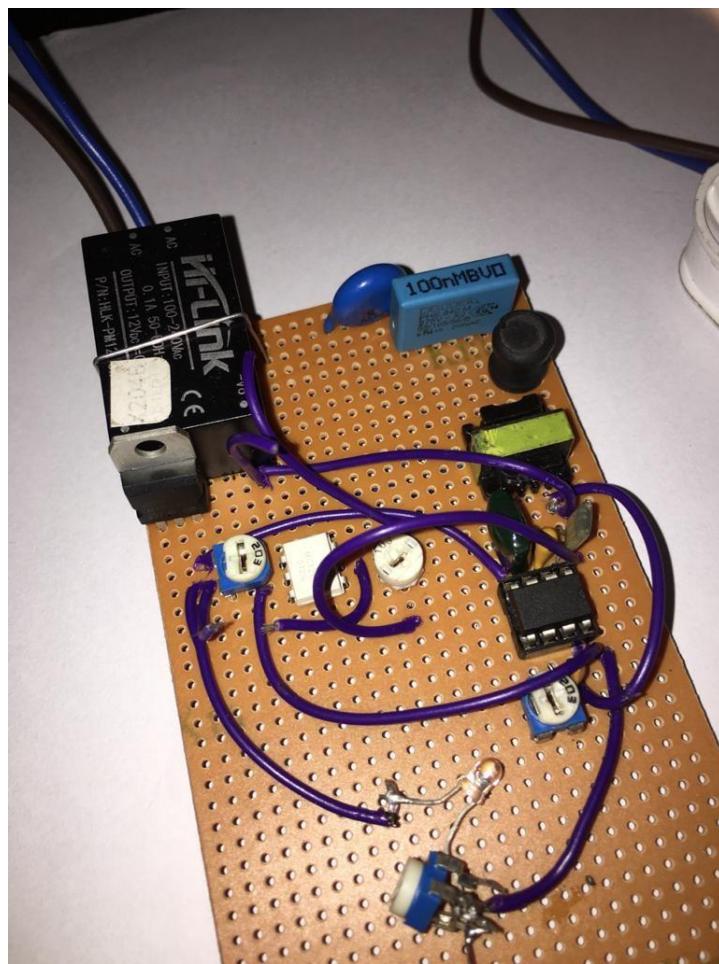


Figure 72: Designed signal Receiver circuit

4. For addition of 12v between the LED instead of 5v for that TIP120 can be included to the circuit according to the schematic below.

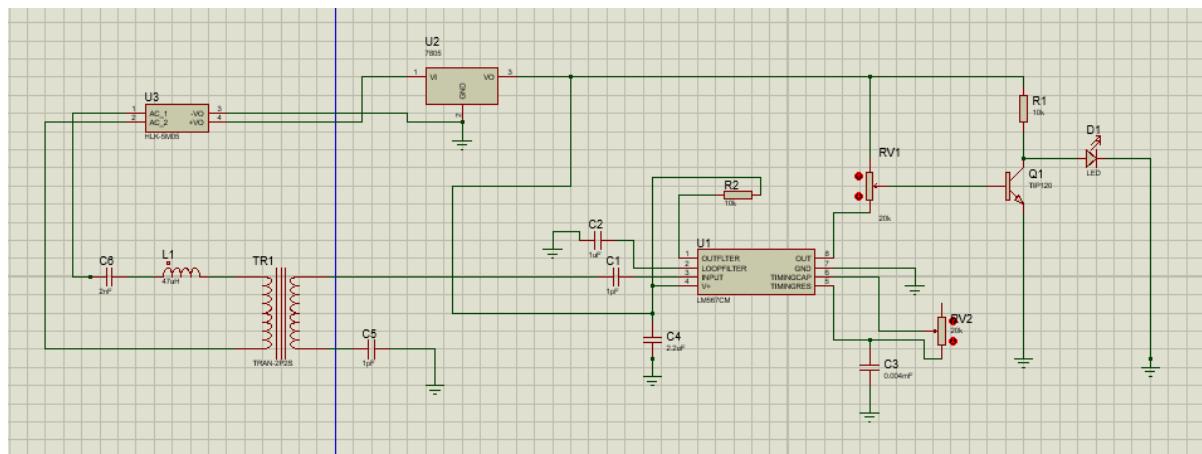


Figure 73: Designed schematic of the Signal receiver with TIP120



Figure 74: Designed signal Receiver circuit with TIP120

5. Study for IoT method of controlling must be done.

2.2.9 Test 9: Designing the IoT method

Equipment:

- ESP8266MOD Micro controller
- L7805 Regulator
- Designed signal transmitter circuit

Software:

- Arduino IDE
- Firebase
- Android Studio

Theory:

Micro controller,

A microcontroller is a compact integrated circuit designed to govern a specific operation in an embedded systems. A typical microcontroller includes a processor, memory and input/output (I/O) peripherals on a single chip.

Sometimes referred to as an embedded controller or microcontroller unit (MCU), microcontrollers are found in vehicles, robots, office machines, medical devices, mobile radio transceivers, vending machines and home appliances, among other devices. They are essentially simple miniature personal computers (PCs) designed to control small features of a larger component, without a complex front-end operating system (OS).

A microcontroller is embedded inside of a system to control a singular function in a device. It does this by interpreting data it receives from its I/O peripherals using its central processor. The temporary information that the microcontroller receives is stored in its data memory, where the processor accesses it and uses instructions stored in its program memory to decipher and apply the incoming data. It then uses its I/O peripherals to communicate and enact the appropriate action.

ESP8266MOD,

The ESP8266 Wi-Fi Module is a self-contained SOC with integrated TCP/IP protocol stack that can give any microcontroller access to your Wi-Fi network. The ESP8266 is capable of either hosting an application or offloading all Wi-Fi networking functions from another application processor. Each ESP8266 module comes pre-programmed with an AT command set firmware, meaning, you can simply hook this up to your Arduino device and get about as much Wi-Fi ability as a Wi-Fi Shield offers. The ESP8266 module is an extremely cost effective board with a huge, and ever growing, community.

This module has a powerful enough on-board processing and storage capability that allows it to be integrated with the sensors and other application specific devices through its GPIOs with minimal development up-front and minimal loading during runtime. Its high degree of on-chip integration allows for minimal external circuitry, including the front-end module, is designed to occupy minimal PCB area. The ESP8266 supports APSD for VoIP applications and Bluetooth co-existence interfaces, it contains a self-calibrated RF allowing it to work under all operating conditions, and requires no external RF parts.

Features:

1. Wi-Fi Direct (P2P), soft-AP
2. Integrated TCP/IP protocol stack
3. Integrated TR switch, balun, LNA, power amplifier and matching network
4. Integrated PLLs, regulators, DCXO and power management units
5. +19.5dBm output power in 802.11b mode
6. Power down leakage current of <10uA
7. Integrated low power 32-bit CPU could be used as application processor
8. SDIO 1.1 / 2.0, SPI, UART
9. STBC, 1x1 MIMO, 2x1 MIMO
10. Flash: 4M
11. A-MPDU & A-MSDU aggregation & 0.4ms guard interval
12. Wake up and transmit packets in < 2ms
13. Standby power consumption of < 1.0mW (DTIM3)

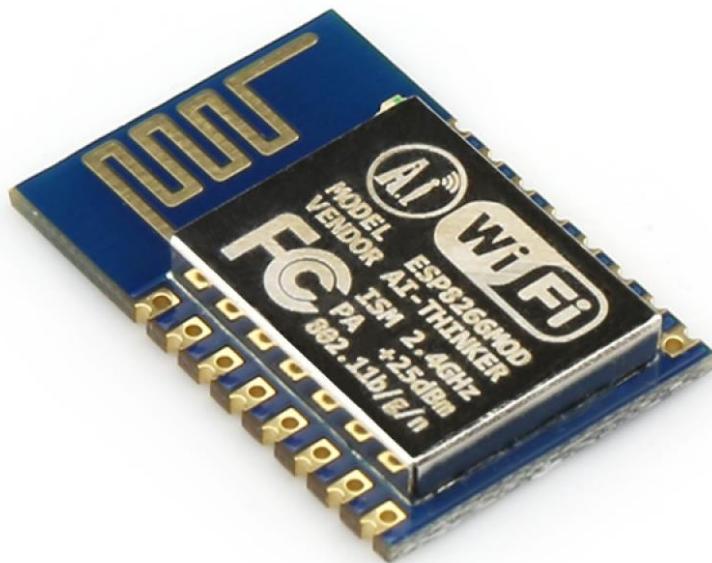


Figure 75: ESP8266MOD

Firebase, [13]

Firebase is a mobile and web application development platform developed by Firebase, Inc. in 2011, then acquired by Google in 2014. As of October 2018, the Firebase platform has 18 products, which are used by 1.5 million apps.

A project is a container for apps across iOS, Android and web. It supports sharing of features such as Database, Configuration and Notifications between your cross-platform apps.

You should add iOS, Android and web app variants to a single project. You can use multiple projects to support multiple environments, such as development, staging and production.

Free project quota per account is limited to a small number of projects (usually around 5-10). Paid plans quota per billing account increases substantially as long as your Cloud billing account is in good standing.

A project is a container for apps across iOS, Android and web. While there is no restriction on number of apps within a project, adding an app can create one or more underlying OAuth 2.0 client IDs. There is a limit of around 30 client IDs that can be created within a single project.

You should ensure that all apps within a project are platform variants of the same application from an end user perspective. For example, if you develop a white label application, each independently labelled app should have its own Firebase project.

Services of Firebase:

Analytics,

- Google Analytics,
Google analytics is a cost-free app measurement solution that provides insights on app usage and user engagement.

Develop,

- Firebase Cloud Messaging,
Formerly known as google cloud messaging (GCM), firebase cloud messaging (FCM) is a cross-platform solution for messages and notifications for Android, ISO and web applications, which as of 2016 can be used at no cost.
- Firebase Auth,
Firebase Auth is a service that can authenticate users using only client-side code. It supports social login, provider Facebook, GitHub, Twitter and Google (and google play games). Additionally, it includes a user management system whereby developers can enable user authentication with email and password login stored with Firebase.
- Firebase Realtime Database,
Firebase provides a real-time database and back-end as a service. The service provides application developers an API that allows application data to be synchronized across clients and stored on Firebase's cloud. The company provides client libraries that enable integration with Android, IOS, JavaScript, Java, Objective-C, Swift and Node.js applications. The database is also accessible through a REST API and bindings for several Java script framework such as Angular.Js, React, Ember.Js and Backbone.JS the REST API uses the server-sent events protocol, which is an API for creating HTTP connections for receiving push notifications from a server. Developers using the realtime database can secure their data by using the company's server-side-enforced security rules.
- Cloud Firestore,
On January 31, 2019, Cloud Firestore was officially brought out of beta, making it an official product of the Firebase lineup. It is the successor to Firebase's original databasing system, Realtime Database, and allows for nested documents and fields rather than the tree-view provided in the Real-time Database.
- Firebase Storage,
Firebase Storage provides secure file uploads and downloads for Firebase apps, regardless of network quality, to be used for storing images, audio, video, or other user-generated content. It is backed by Google cloud storage.

- **Firebase Hosting,**
Firebase Hosting is a static and dynamic web hosting services that launched on May 13, 2014. It supports hosting static files such as CSS, JavaScript, HTML and other files, as well as support through Cloud Functions. The service delivers files over a content delivery network (CDN) through HTTP layer(HTTPS) and secure socket layer encryption (SSL). Firebase partners with Fastly, a CDN, to provide the CDN backing Firebase Hosting. The company states that Firebase Hosting grew out of customer requests; developers were using Firebase for its real-time database but needed a place to host their content.
- **ML Kit,**
ML Kit is a mobile machine learning system for developers launched on May 8, 2018, in beta during the Google I/O 2018. ML Kit APIs feature a variety of features including optical character recognition, detecting faces, scanning barcodes, labelling images and recognizing landmarks. It is currently available for iOS or Android developers. You may also import your own TensorFlow Lite models, if the given APIs are not enough. The APIs can be used on-device or on-cloud.

Procedure:

1. ESP8266MOD Micro controller was connected to the designed signal transmitter circuit according to the Schematic below...
2. L7805 Regulator was connected and the micro controller was powered through it.
3. IOT device was designed to send a signal to the receiver.
4. As the real time database FIREBASE was chosen.
5. ESP8266 connect to the home router (Miyuranga) and it will connect with the FIREBASE.
6. Connection and authorization and the process was done with the Aduino code below (Appendix).
7. Simple real-time database for “LED1” was created using Firebase as the Figure 73 below.
8. A Basic Mobile Application was developed using Android Studio according to the Figure 74 and Figure 75

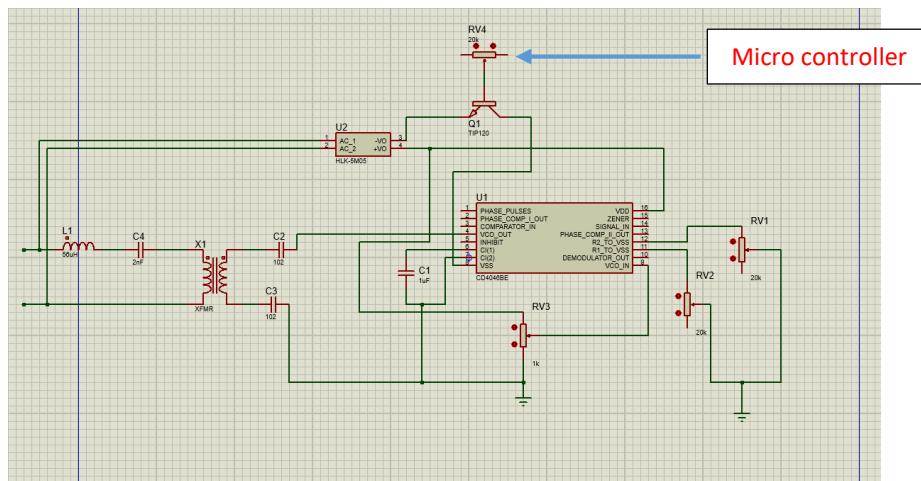


Figure 76: Schematic of the Designed signal transmitter circuit with Micro controller

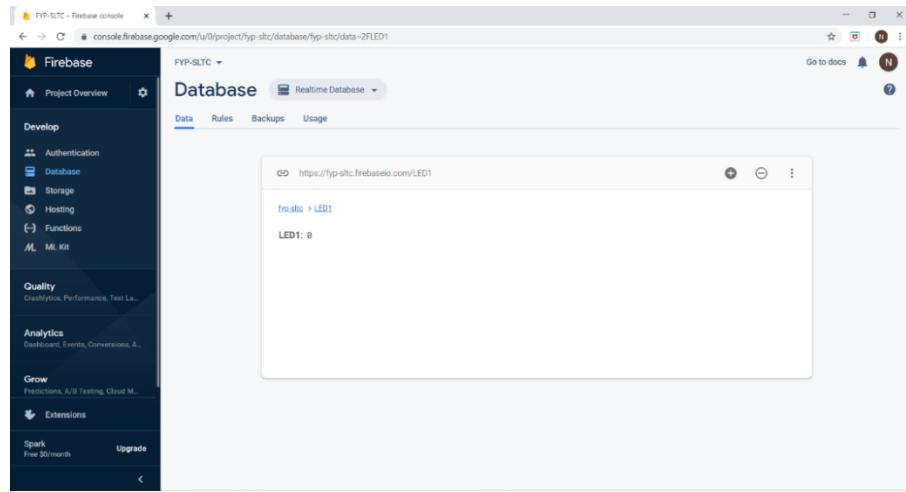


Figure 77: Created Real-time Database of Firebase console

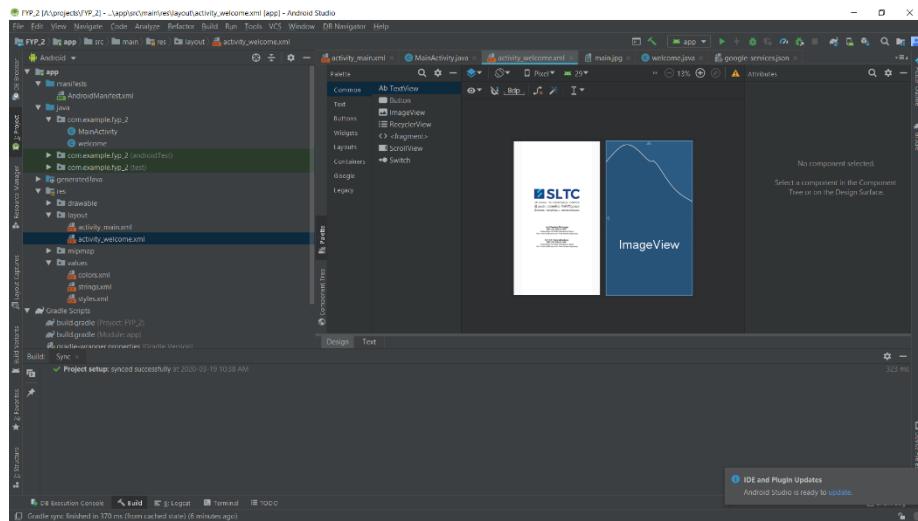


Figure 78: Welcome Form of the Basic Mobile Application

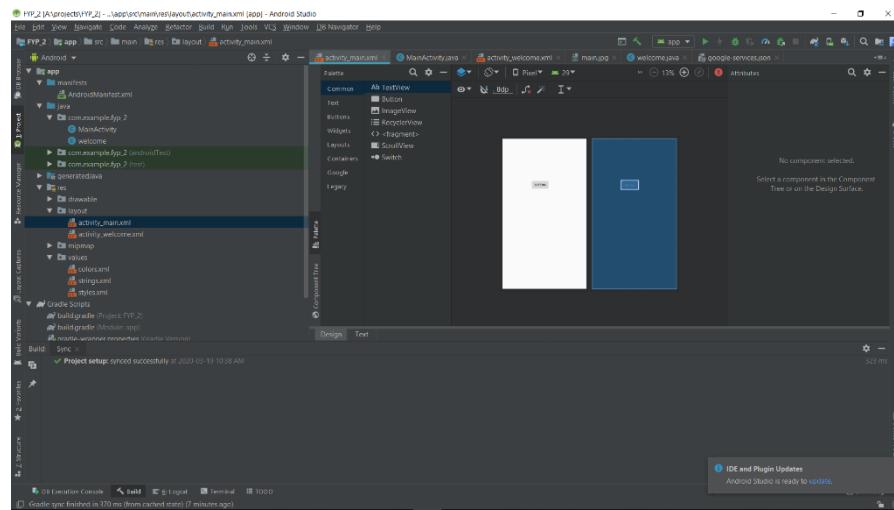


Figure 79: Main Activity Form of the Basic Mobile Application

Discussion:

1. Transmitting signal of 12V V_{pp} should be generated by CD4046, for that power supply should give of 12V to CD4046 by the micro controller. But the Microcontroller can only supply 5V output, for that TIP120 can be used to supply 12 V V_{cc} by a signal of 5V.
2. According to the Table in figure 52, V_{BE} maximum rating was 5V. B-C junction will forward bias with 5V which is given by the micro controller. Considering the V_{CE} rating value for TIP120 was 60 V. This will able to pass 12V for CD4046.

Conclusion:

1. Sending a pulse via a micro controller was successful.
2. In order to send data, this signal has to switch in around 16 MHz, high frequency switching capability of TIP120 and CD4046 must be tested.
3. Transmitting signal attenuation must be checked.

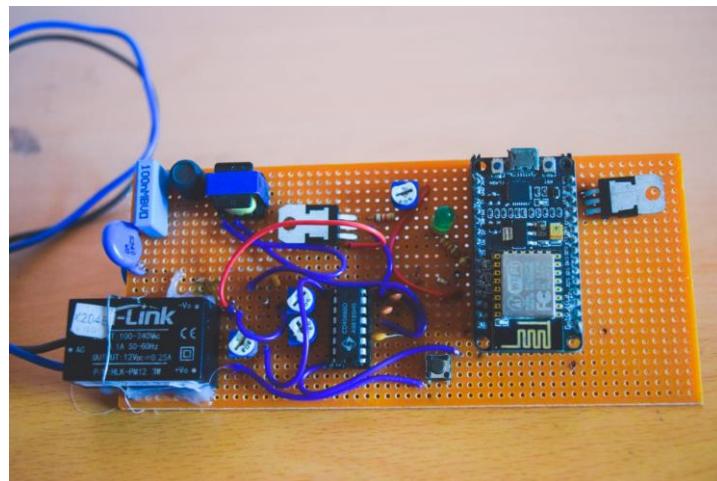


Figure 80: Designed Signal Transmitter after the conclusions

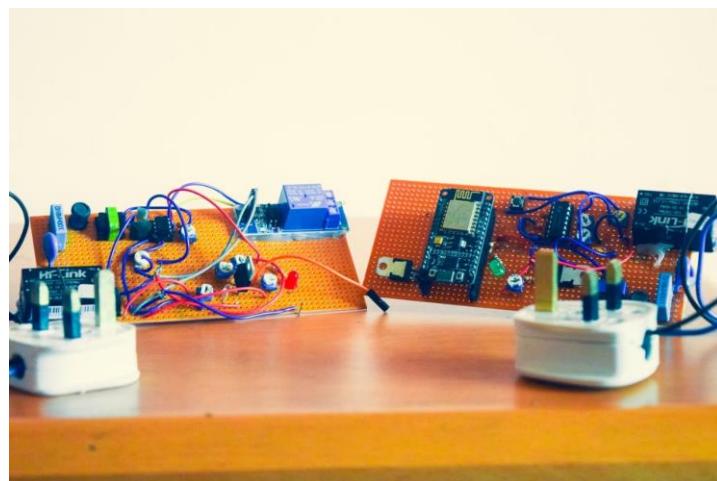


Figure 81: Final Prototype after Stage 1

2.2.10 Test 10: Monitoring Data output from Receiver (LM567)

Equipment:

- Designed Sender
- Designed Reciver
- Arduino Uno

Software:

- Arduino IDE

Theory:

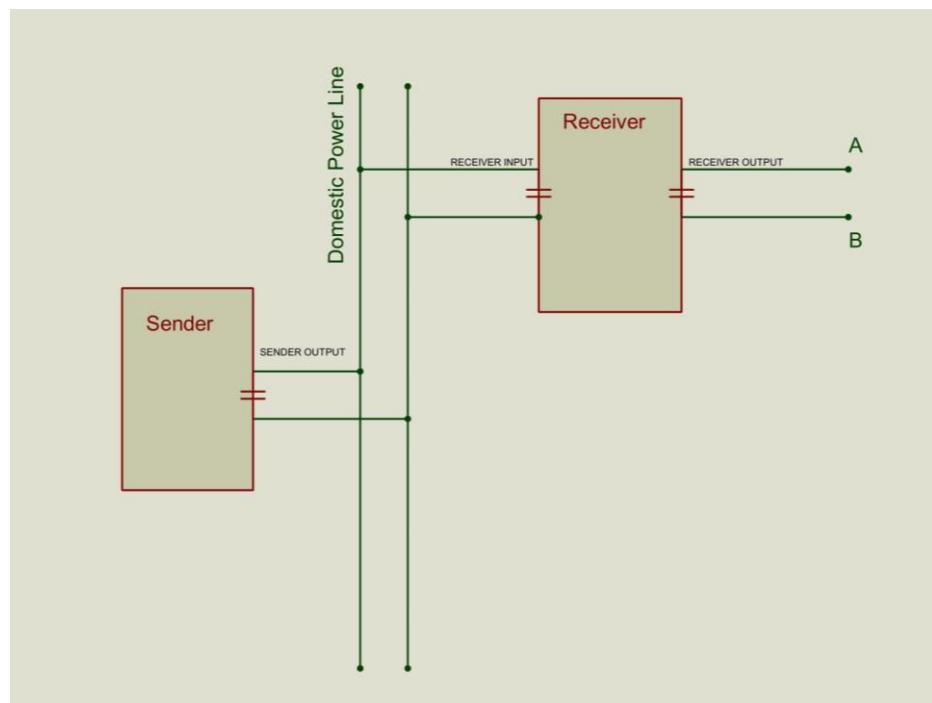


Figure 82 : Test Arrangement

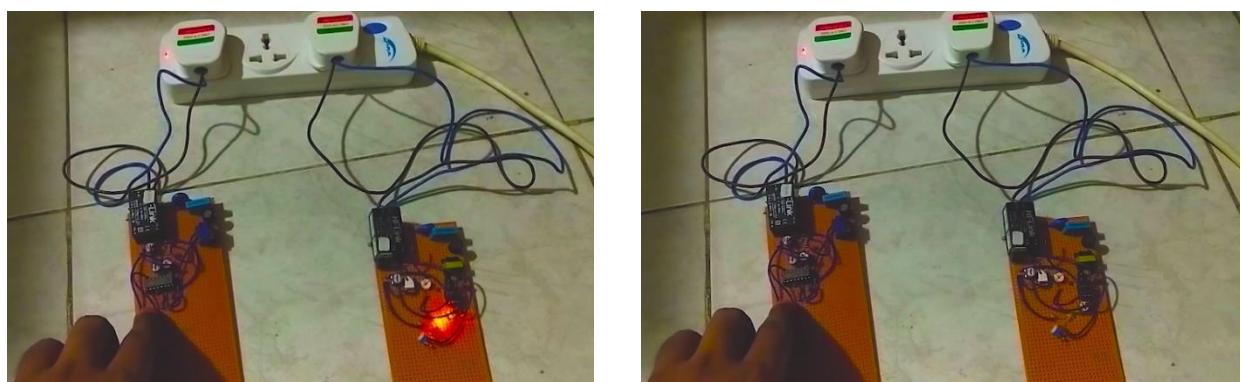


Figure 83: State 1 and State 0

Procedure:

1. Setup was arranged according to the Figure 8.
2. Output A was connected to Digital input pin 8 of Arduino Uno Board.
3. Output B was Grounded
4. State 0 and State 1 Signal from the Sender was given and was digitally read at Digital input pin 8 using the Serial monitor.

Discussion:



Figure 84: Serial Monitor output at State 0



Figure 85: Serial Monitor output at State 1

As observed the State 1 was floating and it was cannot be kept stable.

Conclusion:

1. Seems a proper filter must be developed.
2. Digital filtering can be tried.

2.2.11 Test 11: Digital Filter Design

Equipment:

- Arduino mega
- Signal Generator

Software:

- Arduino IDE
- MATLAB

Theory:

As a solution band pass filter needed to be design. There are few advantages of using digital filtering than an analog filter in this project.

Analog Filter,

1. Analog filters are used for filtering analog signals.
2. Analog filters are designed with various components like resistor, inductor and capacitor
3. Analog filters less accurate & because of component tolerance of active components & more sensitive to environmental changes.
4. Less flexible
5. Filter representation is in terms of system components.
6. An analog filter can only be changed by redesigning the filter circuit.

Digital Filter,

1. Digital filters are used for filtering digital sequences.
2. Digital Filters are designed with digital hardware like FF, counters shift registers, ALU and software s like C or assembly language.
3. Digital filters are less sensitive to the environmental changes, noise and disturbances. Thus periodic calibration can be avoided. Also they are extremely stable.
4. These are most flexible as software programs & control programs can be easily modified. Several input signals can be filtered by one digital filter.
5. Digital filters are represented by the difference equation.
6. A digital filter is programmable, its operation is determined by a program stored in the processor's memory. This means the digital filter can easily be changed without affecting the circuitry (hardware).

Filters are used in a wide variety of applications. Most of the time, the final goal of using a filter is to achieve a kind of frequency selectivity on the spectrum of the input signal. [14]

With design specifications known, we need to find a transfer function which will provide the required filtering. The rational transfer function of a digital filter is as in Equation 8.

$$H(z) = \frac{\sum_{k=0}^{M-1} b_k z^{-k}}{\sum_{k=0}^{N-1} a_k z^{-k}}$$

Equation 9 : The rational transfer function of a digital filter

Now that $\mathbf{H}(z)$ is known, Structure should be realized. In other words, there are many systems which can give the obtained transfer function and we must choose the appropriate one. For example, any of the direct form I, II, cascade, parallel, transposed, or lattice forms can be used to realize a particular transfer function. The main difference between the aforementioned realization structures is their sensitivity to using a finite length of bits. Note that in the final digital system, a finite length of bits will be used to represent a signal or a filter coefficient. Some realizations, such as direct forms, are very sensitive to quantization of the coefficients. However, cascade and parallel structures show smaller sensitivity and are preferred. [14]

FIR filters,

An FIR filter is a special case of Equation 8, An FIR filter is a special case of Equation 9, where $a_0=1$ and $a_k=0$ for $k=1,\dots,N-1$

Hence we obtain:

$$H(z) = \sum_{k=0}^{M-1} b_k z^{-k}$$

Equation 10: Modified rational transfer function of a digital filter

The direct form realization of Equation 9 for $M=3$ is shown in Figure 85. As shown in this figure, a digital filter can be implemented using only three elements:

1. Addition
2. Multiplication by a constant (necessary for the implementation of the coefficients)
3. Delay blocks

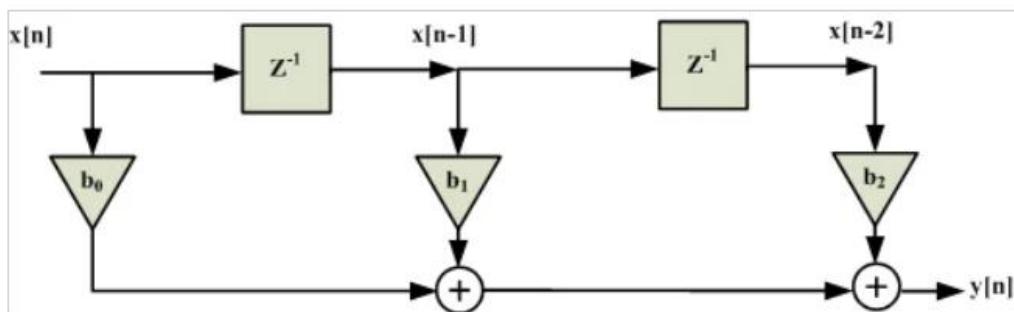


Figure 86 : Direct form of an FIR filter of order 2

There are three coefficients and two delay cells in Figure 85. Note that this filter is of order 2, the number of delay cells, not 3, the number of coefficients. [14]

An FIR filter has two important advantages over an IIR design:

Firstly, as shown in Figure 85, there is no feedback loop in the structure of an FIR filter. Due to not having a feedback loop, an FIR filter is inherently stable. Meanwhile, for an IIR filter, stability needed to be checked.

Secondly, an FIR filter can provide a linear-phase response. As a matter of fact, a linear-phase response is the main advantage of an FIR filter over an IIR design—otherwise, for the same filtering specifications, an IIR filter will lead to a lower order. [14]

Introduction to FIR Filter Design by Windowing,

Window method can be explained using an example. Suppose that it's needed to design a low pass filter with a cutoff frequency of ω_c , the desired frequency response will be:

$$H_d(\omega) = \begin{cases} 1 & |\omega| < \omega_c \\ 0 & \text{else} \end{cases}$$

Equation 11: Window function equation

To find the equivalent time-domain representation, inverse discrete-time Fourier transform needed to be calculated:

$$h_d[n] = \frac{1}{2\pi} \int_{-\pi}^{+\pi} H_d(\omega) e^{j\omega n} d\omega$$

Equation 12: Inverse discrete-time Fourier transform of window function

Substituting Equation 10 into Equation 11,

$$h_d[n] = \frac{1}{2\pi} \int_{-\omega_c}^{+\omega_c} e^{j\omega n} d\omega = \frac{\sin(n\omega_c)}{n\pi}$$

Equation 13: Simplified equation

Taking $\omega_c = \pi/4$ for Equation 12,

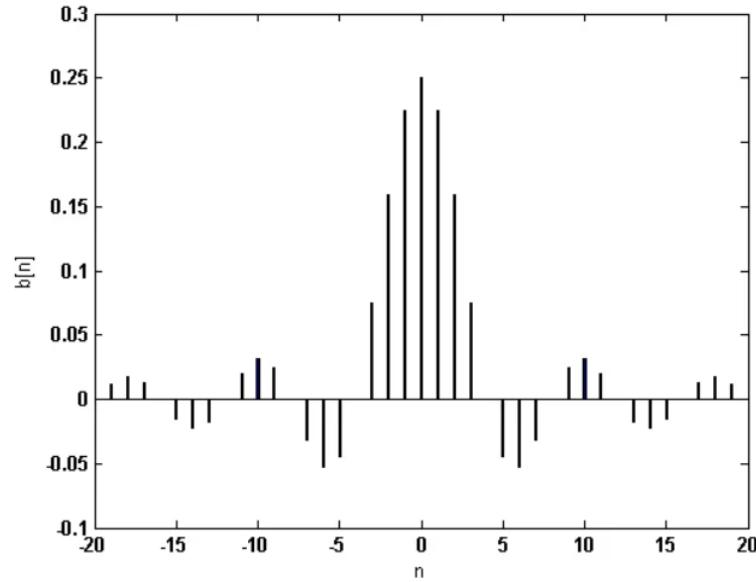


Figure 87: Graph of Equation 12 when $\omega_c = \pi/4$

Truncation of the impulse response is equivalent to multiplying $h_d[n]$ (or its shifted version) by a rectangular window, $w[n]$ which is equal to one for $n=0, \dots, M-1$ and zero otherwise. Therefore, considering the applied shift, the impulse response of the designed filter can be obtained: [14]

$$h[n] = h_d[n - \frac{M-1}{2}]w[n]$$

Equation 14 : Final multiplied equation of Digital Filter

Procedure:

1. Test signal was implied and the graph was potted.
2. Input signal was converted into frequency domain and the graph was potted.
3. The equation was applied and the graph was potted.
4. The hamming window was applied and the graph was potted.
5. Multiplication to make filter equation was done the output waveform was checked.
6. Signal was supplied as the input to the Arduino and it was sampled in an array
7. The weight value of the filter equation relevant to the cutoff frequency is calculated using MATLAB and saved in to an array of Arduino.
8. Each sampled input value was multiplied with the weight value which was saved in the array
9. Multiplied output was passed through FFT and the frequency was displayed.

Discussion:

Implementing test signal,

```
f1 = 2000;
f2 = 4000
fs =16000000; %sampling frequency 16Mhz
fc =3500; % cut off frequency 3.5 Khz
%subplot(2,2,1)
t = 0:1/fs:0.0015 ;
input_sig = sin(2*pi*f1*t)+ sin(2*pi*f2*t)+sin(4*pi*f2*t)
% input_sig = 5*sin(2*pi*f1*t)+ (100/230)*sin(2*pi*f2*t)
```

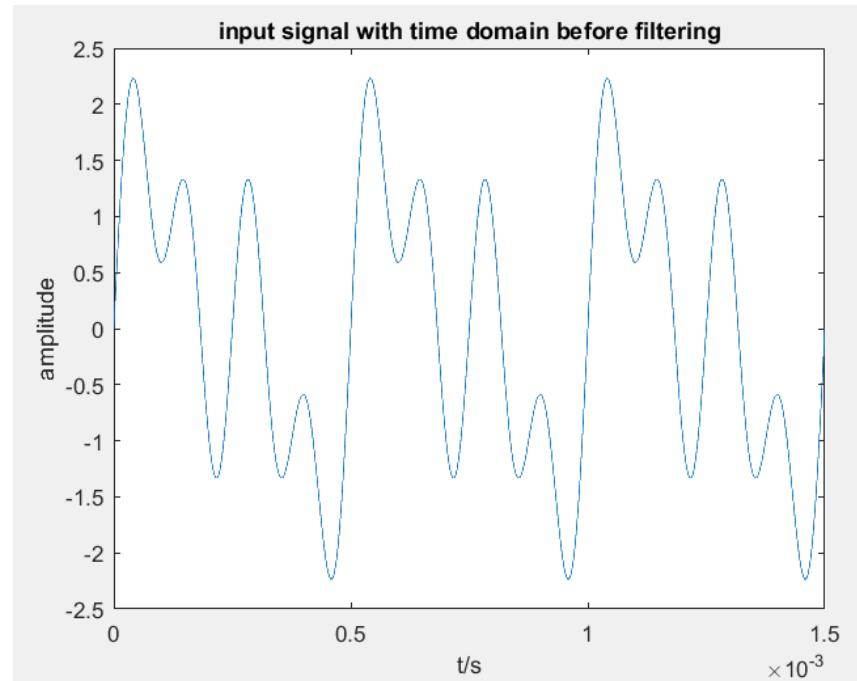


Figure 88 : Input signal with time domain before filtering

Converting the input signal into frequency domain,

```
F_s = fft(input_sig ,512)
amp_fs = abs(F_s);
f=(0:255)*fs/512 ;
plot(f,amp_fs(1:256))
```

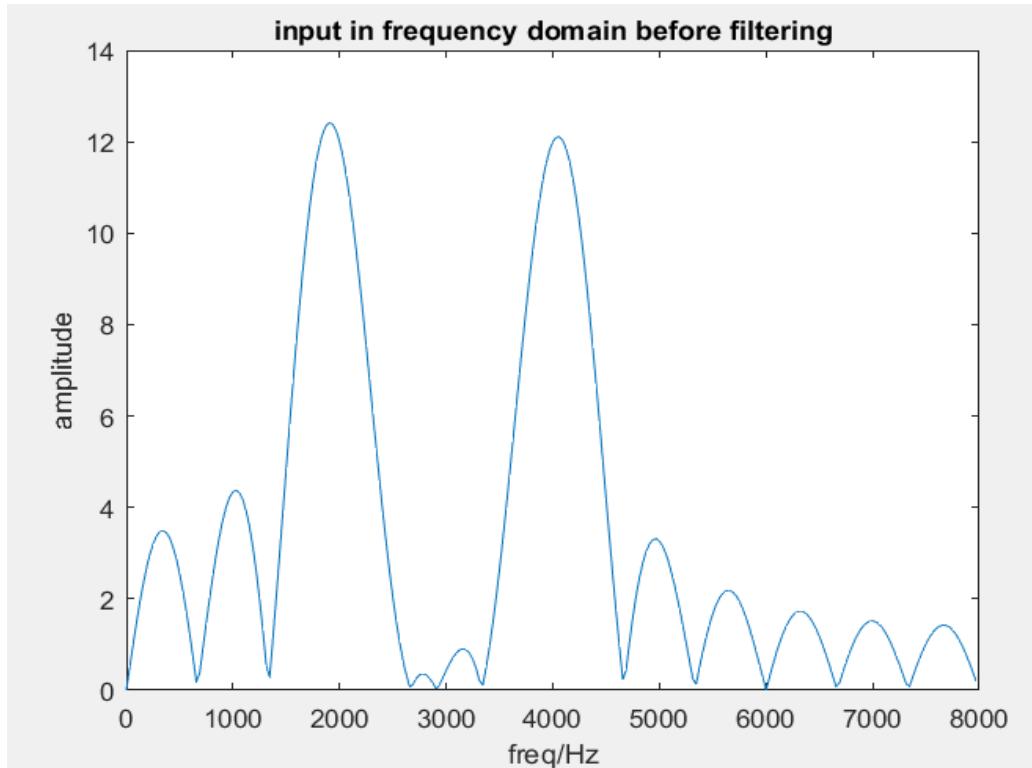


Figure 89: Input in frequency domain before filtering

Appling the equation,

```

]for n =1:(M+1)      %appling the equation
    if (n-1) == (M/2)
        w_lpf(n) = 2*ft;
    else
        w_lpf(n) = sin(2*pi*ft*((n-1)-(M/2)))./(pi*((n-1)-(M/2)));
    end
end

```

Appling the hamming window,

```

%with hamming window
]for m=1:(M+1)
    w_hm(m) = 0.54 -0.46*cos(2*pi*(m-1)/M);
end

```

Multiplication,

```

%w_n =w_lpf*w_hm
]for i=1:(M+1)
    b_cof(i)=w_lpf(i).*w_hm(i) ;
end

```

Output Waveform,

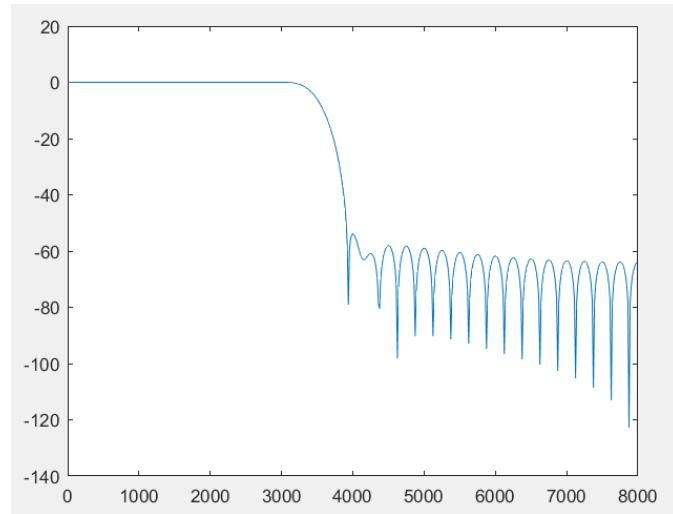


Figure 90: Designed Digital Filter

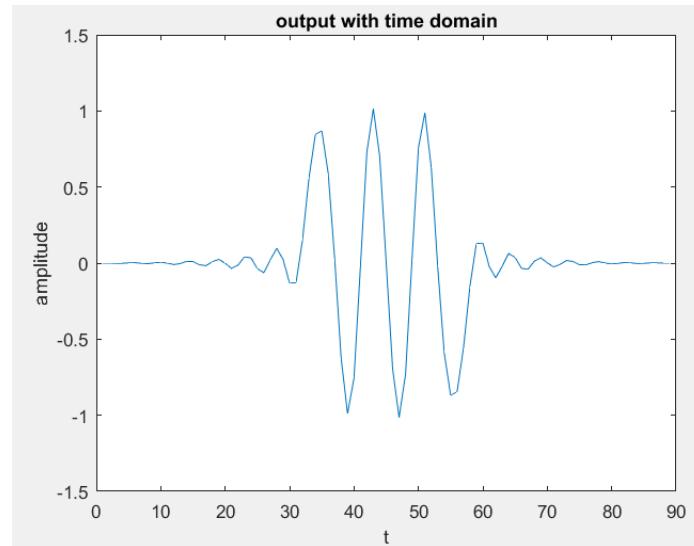


Figure 91; Output Waveform in time domain

As it was successful,

Signal was supplied as the input to the Arduino and it was sampled in an array

The weight value of the filter equation relevant to the cutoff frequency is calculated using MATLAB and saved in to an array of Arduino.

Each sampled input value was multiplied with the weight value which was saved in the array

Multiplied output was passed through FFT and the frequency was displayed.

```

void convolution(double *sig_src_arr,
                 double *sig_dest_arr ,
                 double *imp_response_arr,
                 uint32_t sig_src_length,
                 uint32_t imp_response_length
) {

    int i,j ;

    for(i=0;i<(sig_src_length+ imp_response_length);i++) {
        sig_dest_arr[i]=0;
    }

    for(i=0;i<sig_src_length;i++) {
        for(j=0;j<imp_response_length;j++) {
            sig_dest_arr[i+j] = sig_dest_arr[i+j]+(sig_src_arr[i]*imp_response_arr[j]);
        }
    }

}

test_6  weighth  weighth_2  weighth_3  weighth_4  wight_5

*/
#define FILTER_TAP_NUM 197

double ffImpulse_response[197] = {
    0.02556344209789435,
    0.03195711396384087,
    -0.013226796408190722,
    -0.05403228336740557,
    -0.027594825595883284,
    0.012881857339434031,
    0.0052096106847802914,
    -0.006272288746999264,
    0.01345884874152693,
    0.018627225885619273,
    0.0012412872802783676,
    0.003641418289906811,
    0.012554916345014922,
}

```

Figure 92: Arduino implementations with various weighted value arrays

Conclusion:

1. A band pass digital filter can be designed using this method.
2. The maximum cutoff frequency that can be obtained is 4 kHz.
3. Proper coupler that can give the maximum gain in the range of 2kHz – 4kHz need to be design.

2.2.12 Test 12: Design a new coupler

Equipment:

- High frequency Transformer (taken from 230v – 22v converter circuits)
- Capacitors (X1 type 2.2nF and X2 type 10nF)
- Signal Generator
- Oscilloscope
- CD4046

Theory:

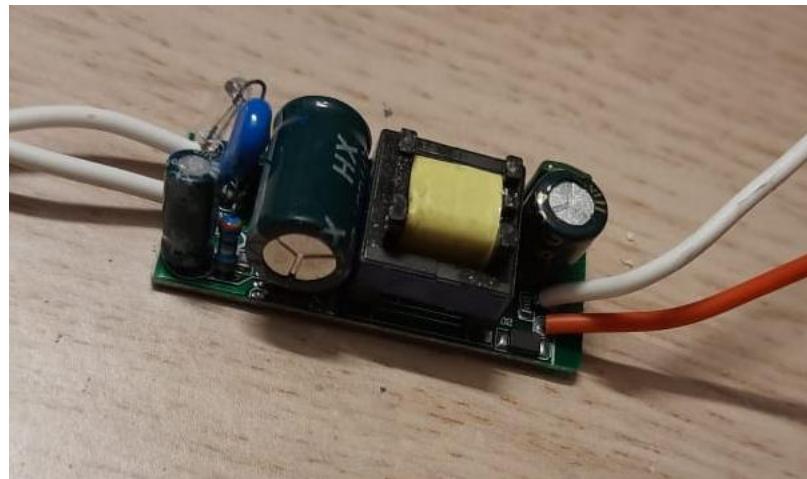


Figure 93: High frequency Transformer

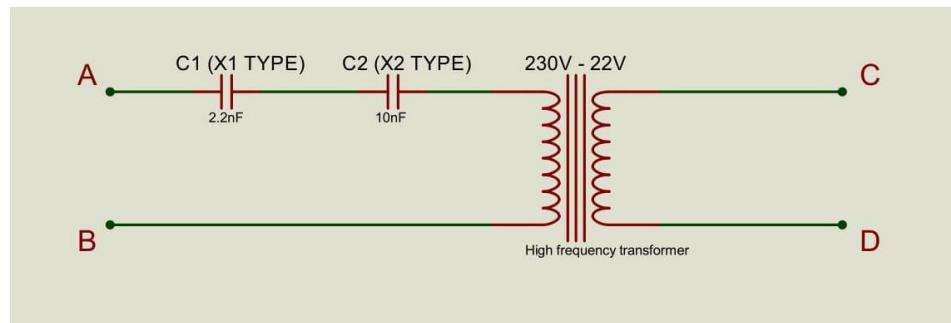


Figure 94: Coupler arrangement

Procedure:

1. Transformer was removed carefully from the circuit.
2. The circuit was set according to the Figure 93.
3. Signal was inputted using the signal generator from CD end and was observed using the Oscilloscope from AB end.
4. Signal Frequency was varied till a signal that has the maximum gain was found.
5. Signal generated from CD4046 was inputted and was observed using the Oscilloscope from AB end.

Discussion:

In the first stage of the project the transformers that were found were not identical and a change needed to be done. Major issue that occurred was finding a high frequency transformer and for this a transformer from an existing circuit needed to be taken. Only option was to take two transformers from 230v-22v converter circuits.

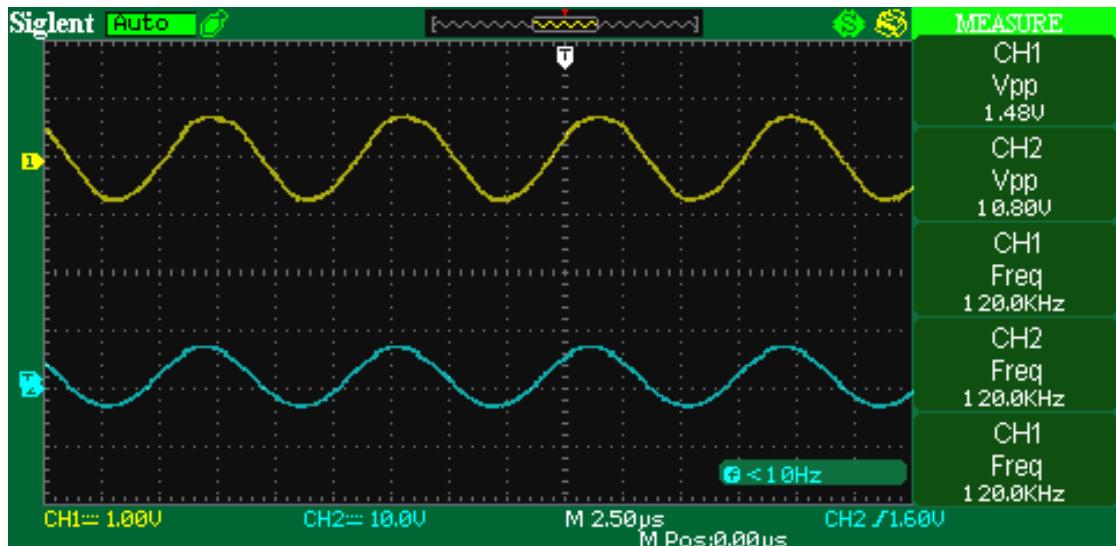


Figure 95: Signal input and the output when it has the maximum gain

At 120 kHz frequency the maximum gain was taken.

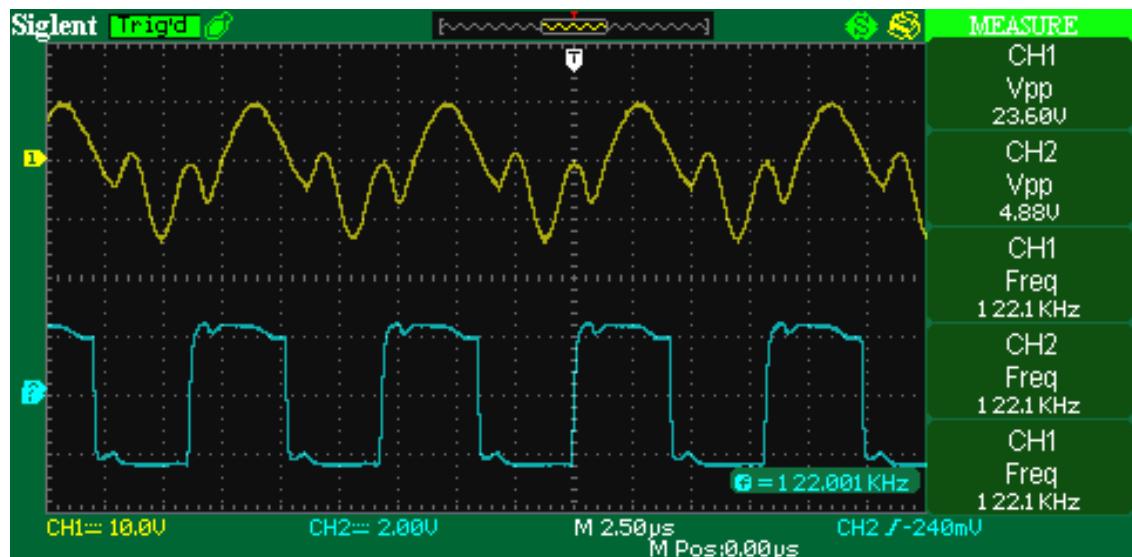


Figure 96: Signal input and the output when it was generated from CD4046

When the signal generated from CD4046 was inputted above signal was observed still with the maximum gain.

Conclusion:

1. The frequency that gave the maximum gain can be observed as 120 kHz
2. Then came a major issue with the digital filtering because it permitted only till 4 kHz frequency. Therefore the digital filtering cannot be used and the have to move on with the existing coupler since the transformer needed to be fixed.
3. Generating frequency from CD4046 need to be taken as 120 kHz.

2.2.13 Test 13: Modulator Design

Equipment:

- CD4046
- Resistors/capacitors
- Signal generator
- Oscilloscope
- Breadboard

Theory:

CD4046 was used as the modulator circuit. Signal input is given to pin 9 (VCO_in). Resister values supply to R1 (pin 11) and R2 (pin 12) in the Figure 96 generate separate frequencies for the signal state 1 and 0 at pin 9. VCO unit in CD4046 separately generate these 2 frequencies and this makes FSK Modulation.

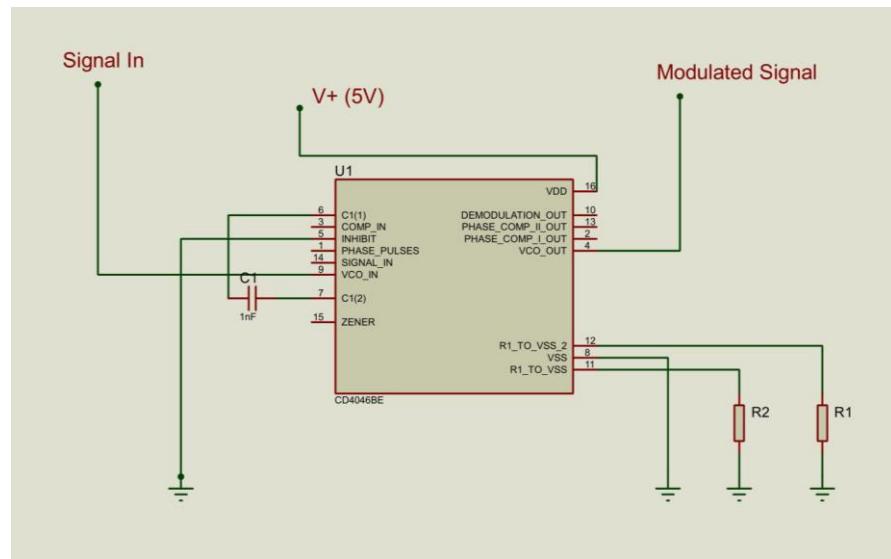


Figure 97: Designed Modulator circuit

Procedure:

1. Capacitor and resistor for VCO was calculated using an online calculator. [15]

R1 [kΩ]	23	3 kΩ < R1 < 300 kΩ
R2 [kΩ]	49	3 kΩ < R2 < 300 kΩ
C1 [pF]	4100	40 pF < C
FREQ.MIN [kHz]	62.197	$V_{TUN} = 1.1 \text{ V}$
FREQ.TYP [kHz]	88.721	$V_{TUN} = 2.5 \text{ V}$
FREQ.MAX [kHz]	120.199	$V_{TUN} = 3.9 \text{ V}$
K_{VCO}	20.715	kHz/V

Figure 98: VCO Online calculator

2. Circuit was designed on breadboard with the other components to CD4046 and power was given.
3. Signal generator was connected to pin 9(V_{co_in}) with offset of 2.5 V and 5v peak to peak 1 KHz square signal.
4. Output was monitored at pin 4 (V_{co_out}) by an oscilloscope comparing with input signal.
5. Modulated signal was pass through the coupler and monitor the output from the plug top.
6. Output wave form was monitored by receiver coupler when sender coupler send the signal and 230 v was supplied.

Discussion:

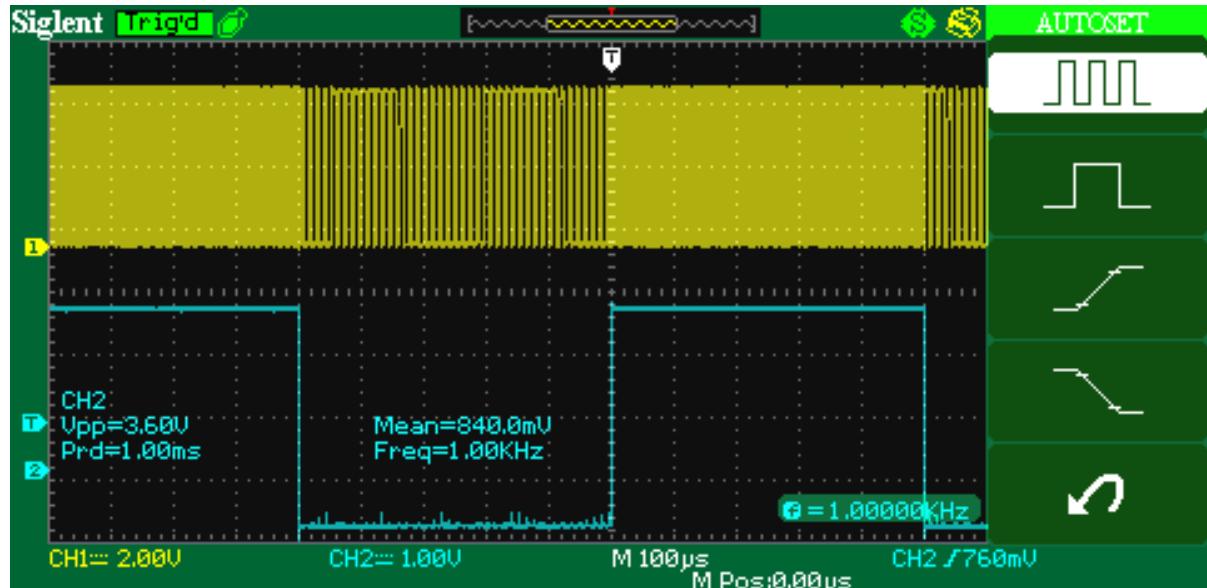


Figure 99: Modulated output signal with a 1 kHz signal input.

It can be observed here for the 0 state - 36 kHz and for 1 state - 121 kHz.

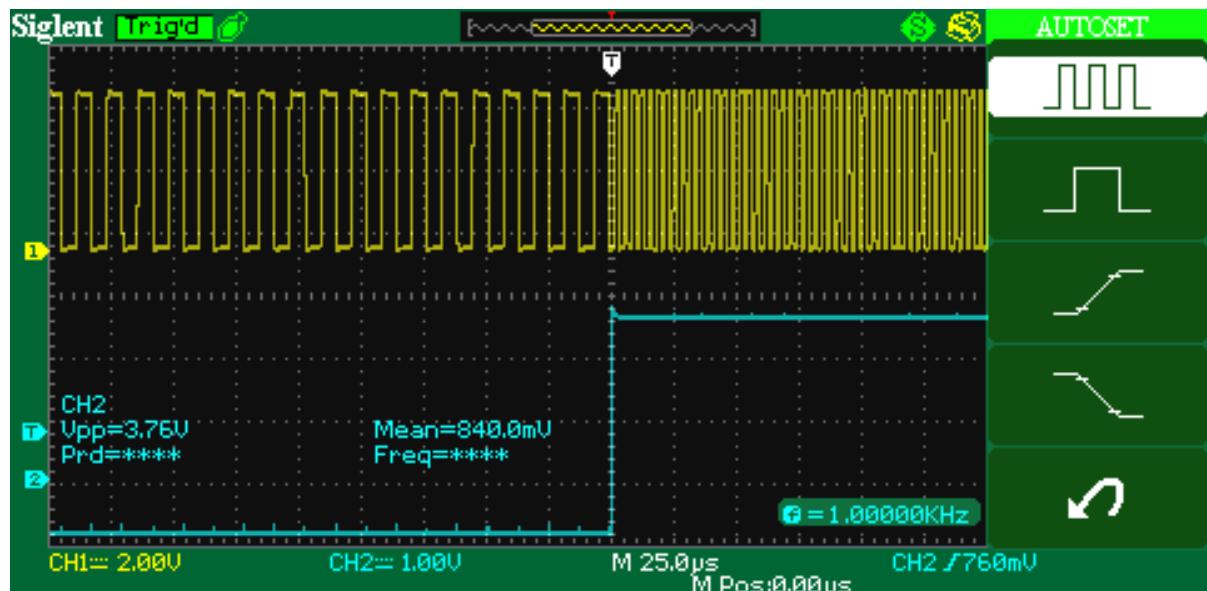


Figure 100: State 0 to State 1 interchange

During the state interchange (from 0 to 1) frequency was changed accurately without any delay for an input signal of 1 Khz. So this helps to keep duty cycle same at the demodulation point.

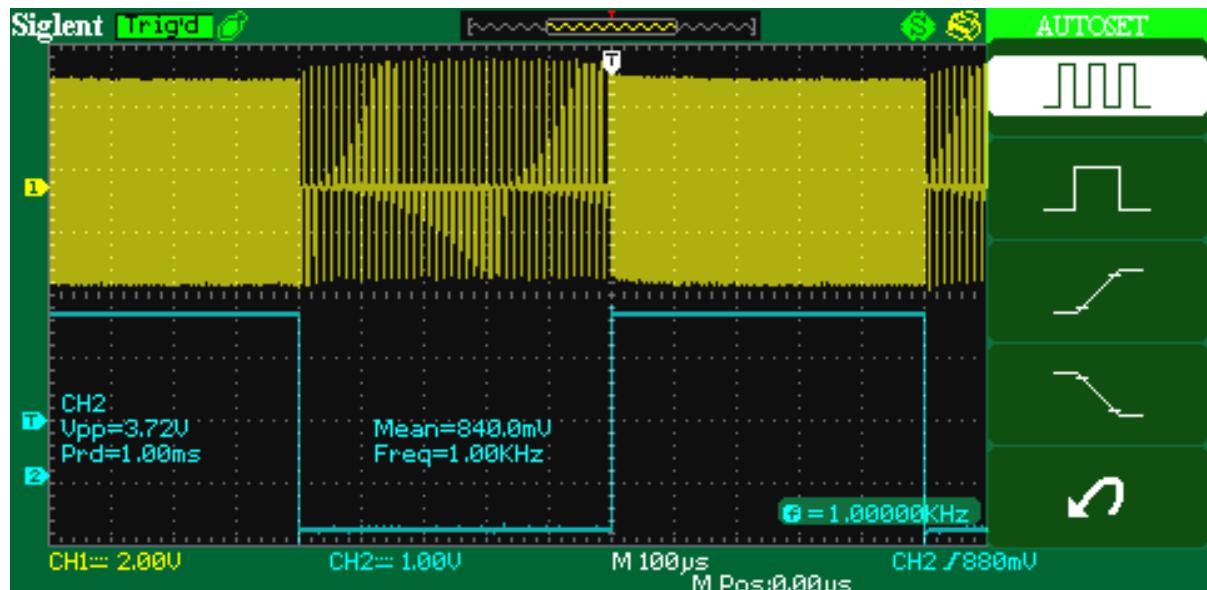


Figure 101: Output waveform from sender when the state 1 frequency was 87 kHz

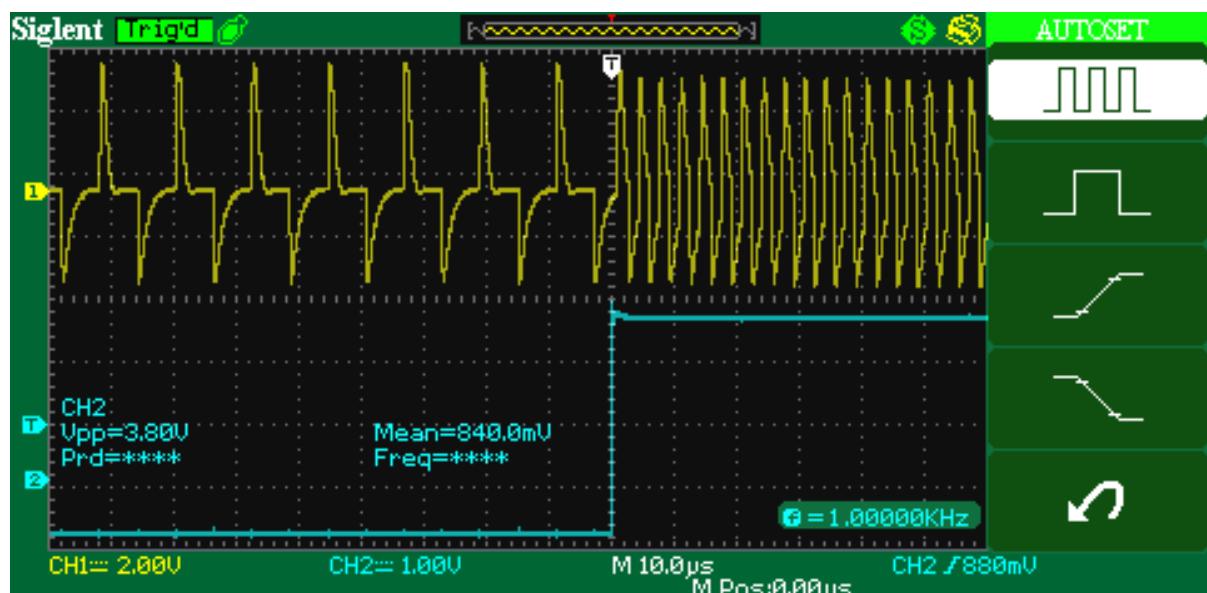


Figure 102: State 0 to State 1 interchange when state 1 frequency was 87 kHz

Shape of the modulated signal from the sender output was changed. But there was no issue for duty cycle.

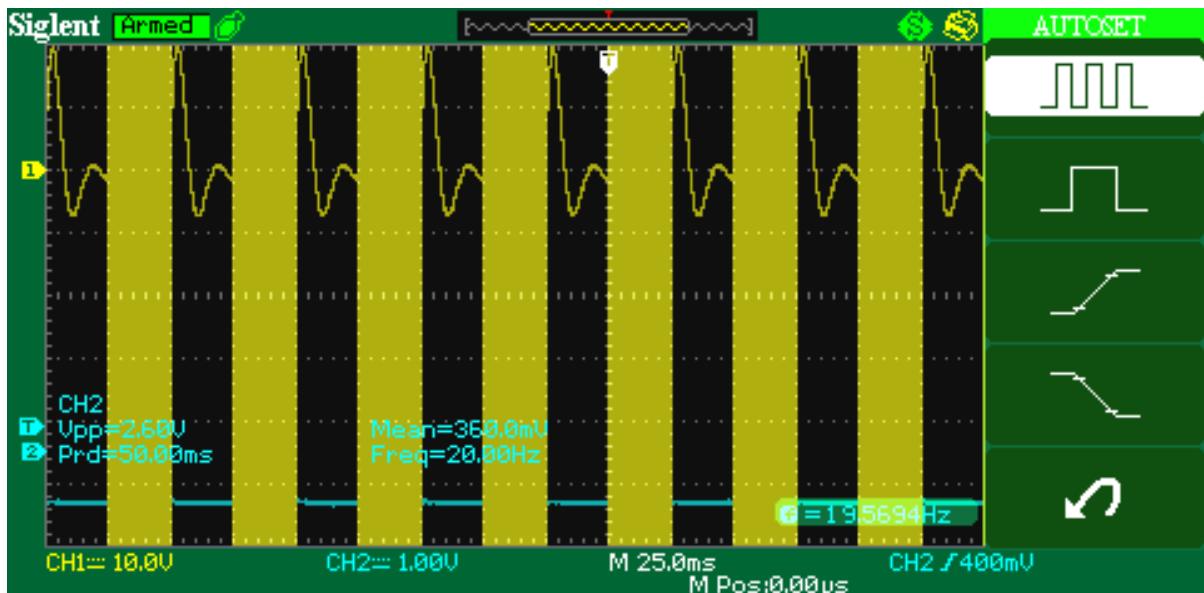


Figure 103: Output waveform from sender when the state 1 frequency was 120 kHz

When state 1 frequency was changed to 120 kHz and best output wave with highest Vpeak to peak could gain

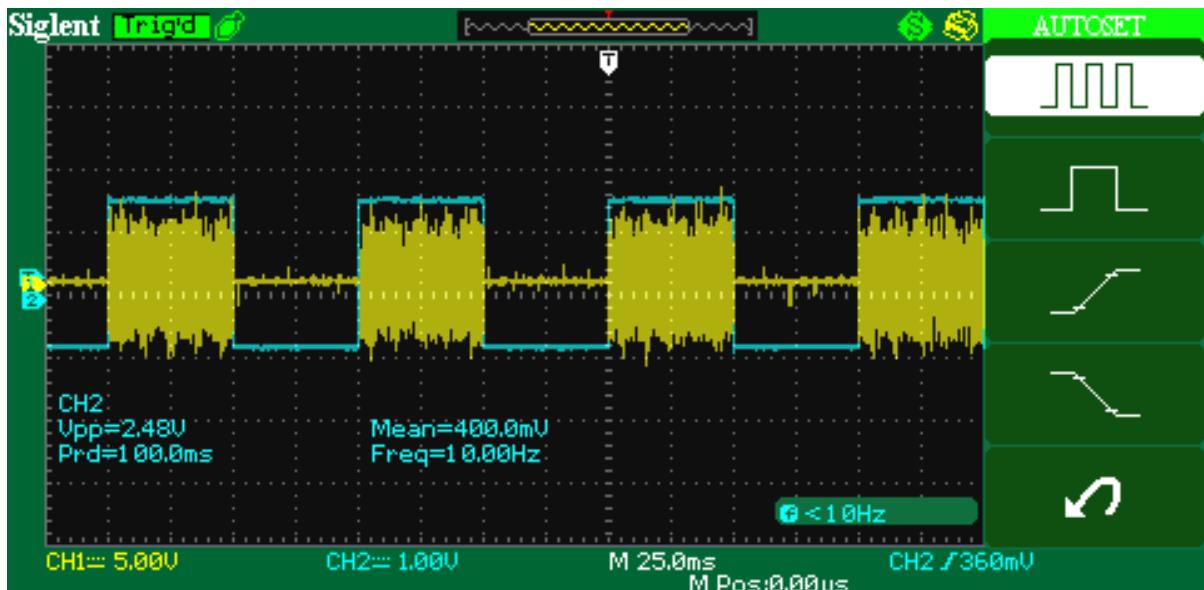


Figure 104: Wave observed after receiver coupler

Output wave observed after the coupler of the receiver was observed as above when sender send the signal through 230 v supply.

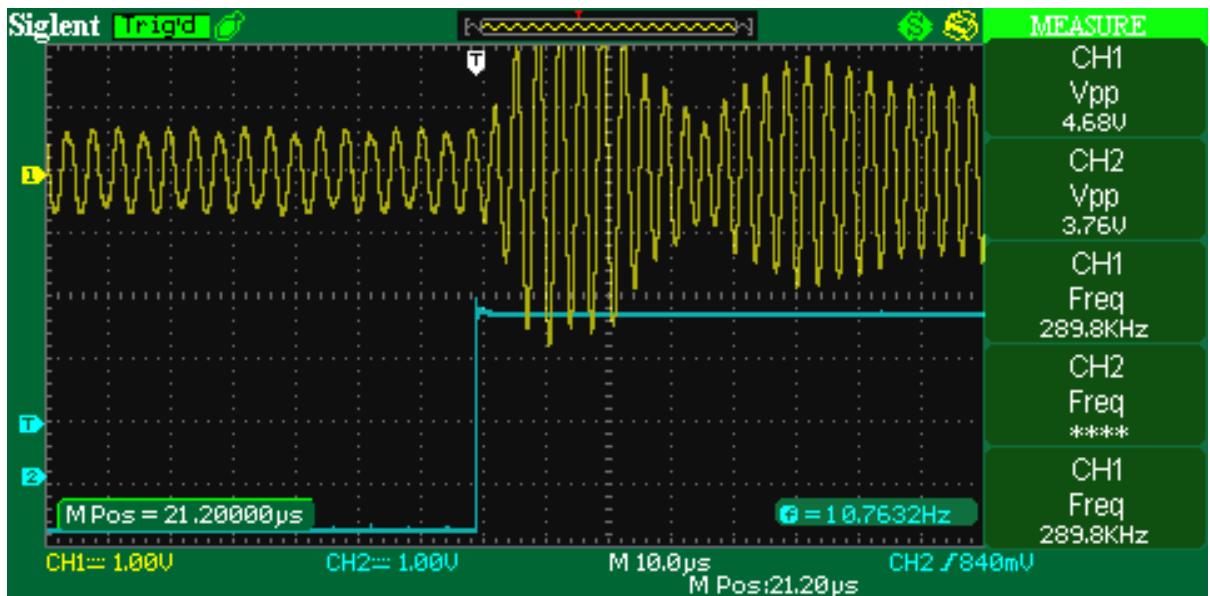


Figure 105: State 0 to State 1 interchange after the coupler of the receiver

Conclusion:

1. A message signal that has a data rate of 1000 bits per second can be transferred.
2. The message bit fail rate gets lower when the data rate gets lower.

2.2.14 Test 14: Demodulator Design

Equipment:

- CD4046
- Resistors and capacitors
- Signal generator
- Oscilloscope
- Modulated Sender (CD4046) circuit

Theory:

PLL Fundamentals

The basic PLL system is shown in Figure 1. The system consists of three parts: phase comparator, low-pass filter (LPF), and voltage-controlled oscillator (VCO). All parts are connected to form a closed-loop frequency-feedback system.

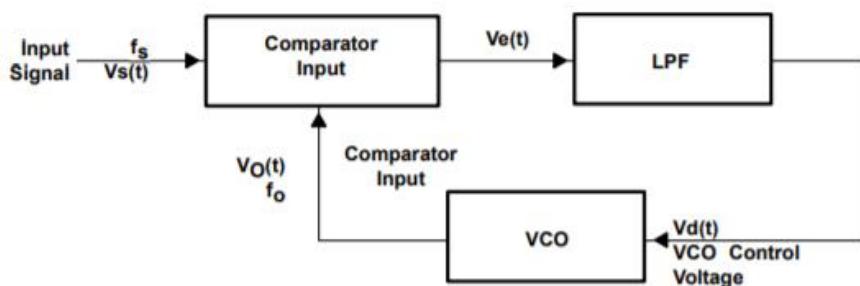


Figure 106: PLL Block Diagram

With no signal input applied to the PLL system, the error voltage at the output of the phase comparator is zero. The voltage, $Vd(t)$, from the LPF also is zero, which causes the VCO to operate at a set frequency, f_o , called the center frequency. When an input signal is applied to the PLL, the phase comparator compares the phase and frequency of the signal input with the VCO frequency and generates an error voltage proportional to the phase and frequency difference of the input signal and the VCO. The error voltage, $Ve(t)$, is filtered and applied to the control input of the VCO. $Vd(t)$ varies in a direction that reduces the frequency difference between the VCO and signal-input frequency. When the input frequency is sufficiently close to the VCO frequency, the closed-loop nature of the PLL forces the VCO to lock in frequency with the signal input. When the PLL is in lock, the VCO frequency is identical to the signal input, except for a finite phase difference. The range of frequencies over which the PLL can maintain this locked condition is defined as the lock range of the system. The lock range always is larger than the band of frequencies over which the PLL can acquire a locked condition with the signal input. This latter band of frequencies is defined as the capture range of the PLL system. [8]

Figure 43 shows a block diagram of the CD4046B, which has been implemented on a single monolithic integrated circuit. The PLL structure consists of a low-power, linear VCO and two different phase comparators, having a common signal-input amplifier and a common comparator input. A 5.2-V Zener diode is provided for supply regulation, if necessary. The VCO can be connected either directly or through frequency dividers to the comparator input of the phase comparators. The LPF is implemented through external parts because of the radical configuration changes from application to application and because some of the components cannot be integrated. The CD4046B is available in 16-lead ceramic dual-in-line packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead small outline package (NSR suffix) and in chip form (H suffix). [8]

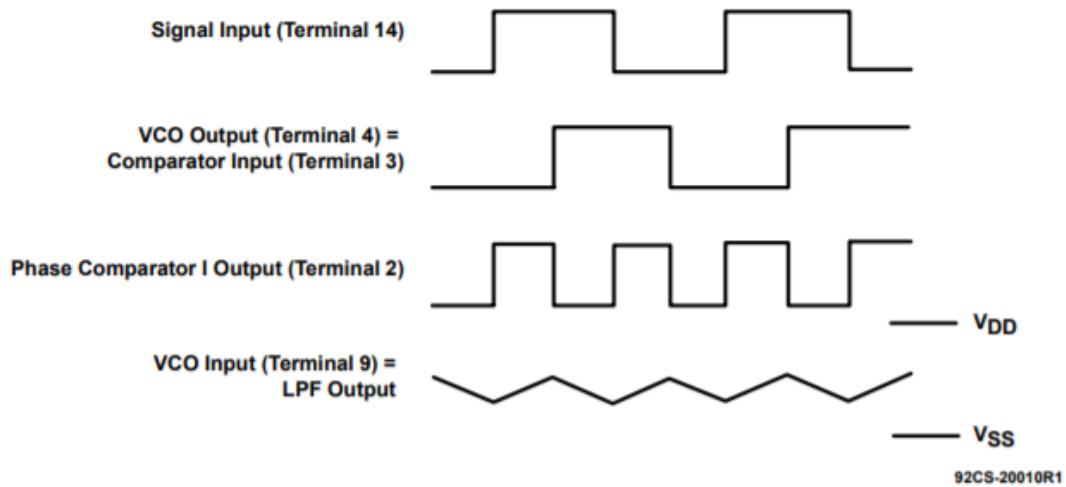
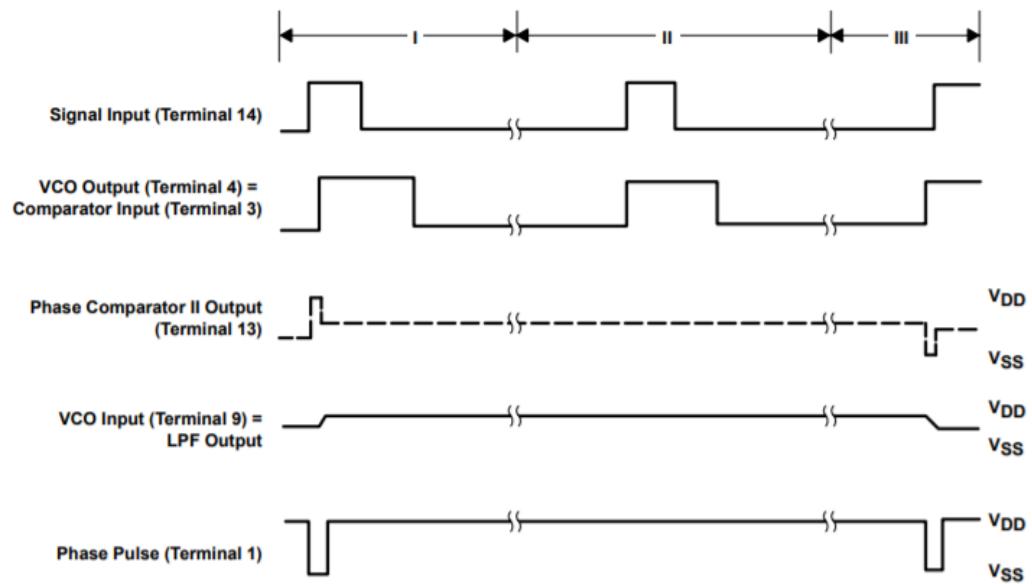


Figure 107: Typical Waveforms for the CD4046B Employing Phase Comparator I in Locked condition of f_o

Phase comparator II is an edge-controlled digital memory network. It consists of four flip-flop stages, control gating, and a 3-state output circuit comprising p and n drivers having a common output node.



NOTE A: Dashed line is an open-circuit condition.

Figure 108: Typical Waveforms for the CD4046B Employing Phase Comparator II in Locked Condition

FM Demodulation,

When a PLL is locked on an FM signal, the VCO tracks the instantaneous frequency of that signal. The VCO input voltage, which is the filtered error voltage from the phase detector, corresponds to the demodulated output. For this phase comparator 1 is used, [8]

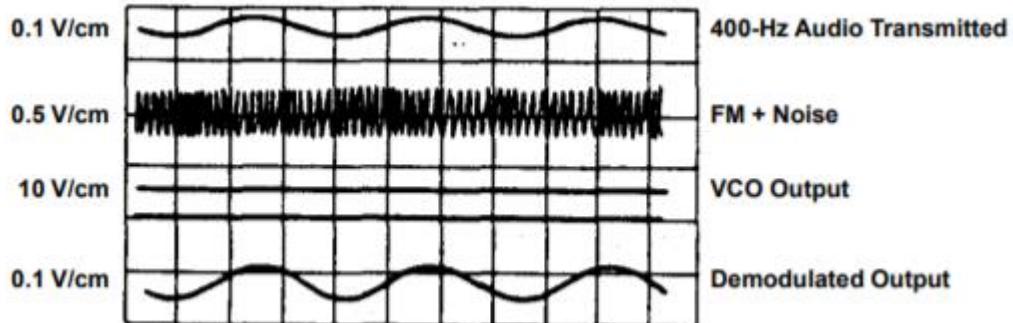


Figure 109: FM Demodulator Voltage Waveforms

Frequency Synthesizer,

The PLL system can function as a frequency-selective frequency multiplier by inserting a frequency divider into the feedback loop between the VCO output and the comparator input. For this phase comparator 1 is used,

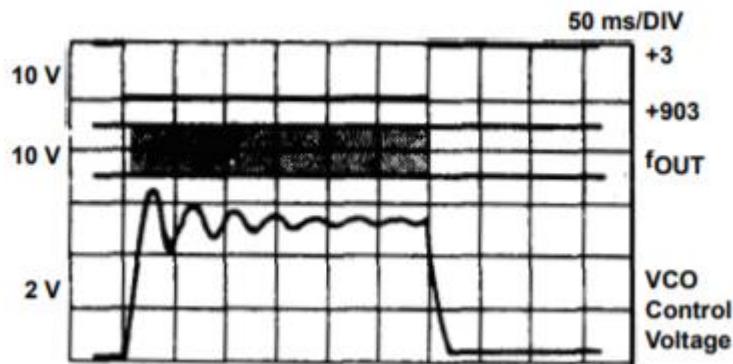


Figure 110: Frequency-Synthesizer Waveforms

Circuit sketch of demodulator,

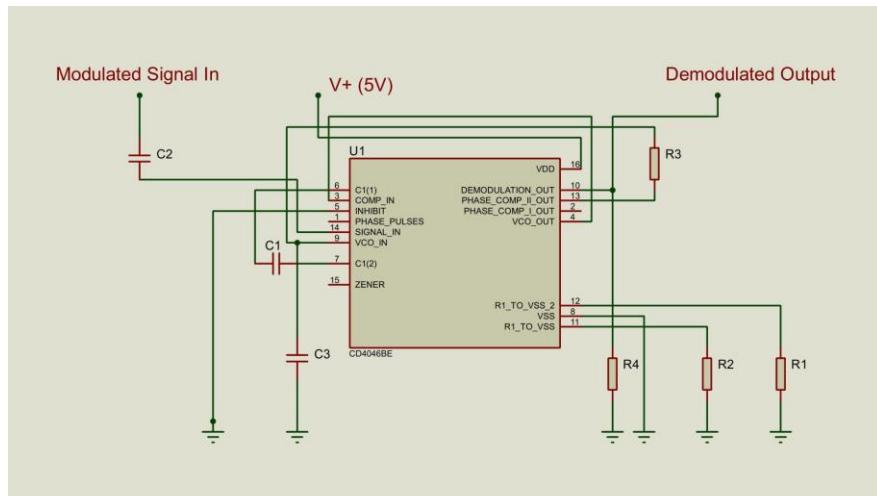


Figure 111: Circuit sketch of demodulator

Procedure:

1. Modulated output from the sender IC was directly connected to demodulator circuit.
2. VCO frequency of demodulator circuit was adjusted with sender IC VCO.
3. Demodulated output was taken after the phase comparator 2 and appropriate low pass filter.
4. Plug the sender and receiver to 230 v and demodulator circuit was joined to the receiver coupler.
5. Observe the demodulate output with power.
6. Some changes were done to the low pass filter (only the capacitor was changed) to get stable demodulated waveform.
7. Resister at demodulated output pin (pin 10) was changed to get a slim state 1

Discussion:

Modulated output from the IC (pin 4) is directly connected to demodulator circuit and check the output.

Yellow - Modulated signal

Blue - Demodulated signal

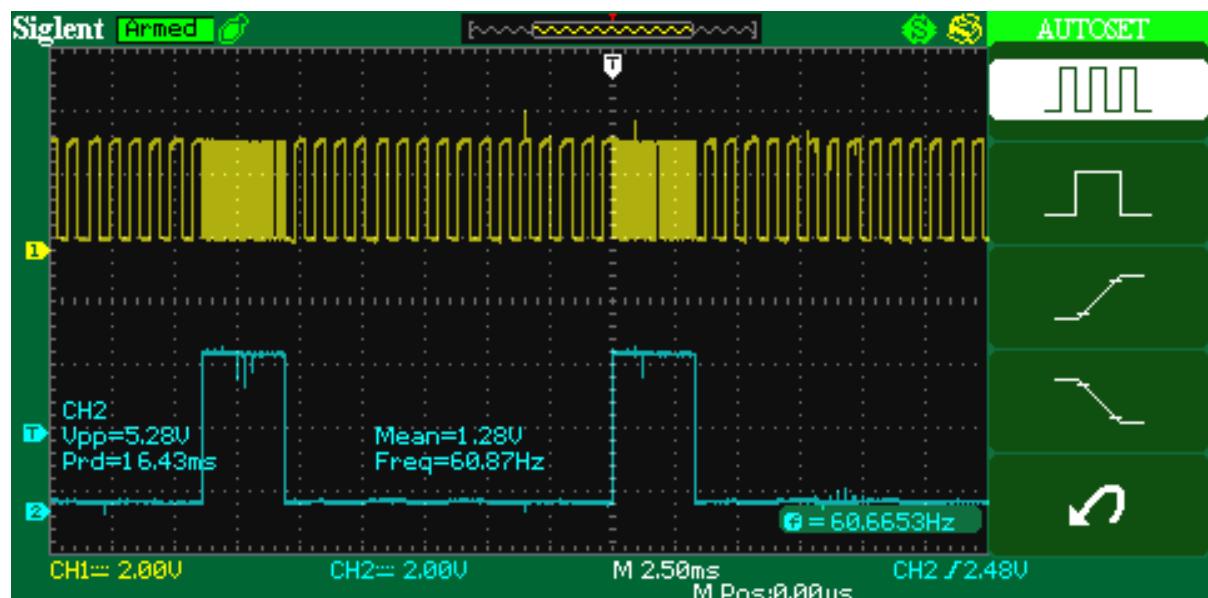


Figure 112: Modulated Output and Demodulated signal

Demodulated output was checked for same tuned circuit for above process, from the receiver circuit with 230 v power supply.

Blue - modulated output from sender.

Yellow - demodulated output.

Demodulated signal was not fine for the above tuned circuit specs. Signal was dropped in state 1 frequently. So the circuit specs have to be change.

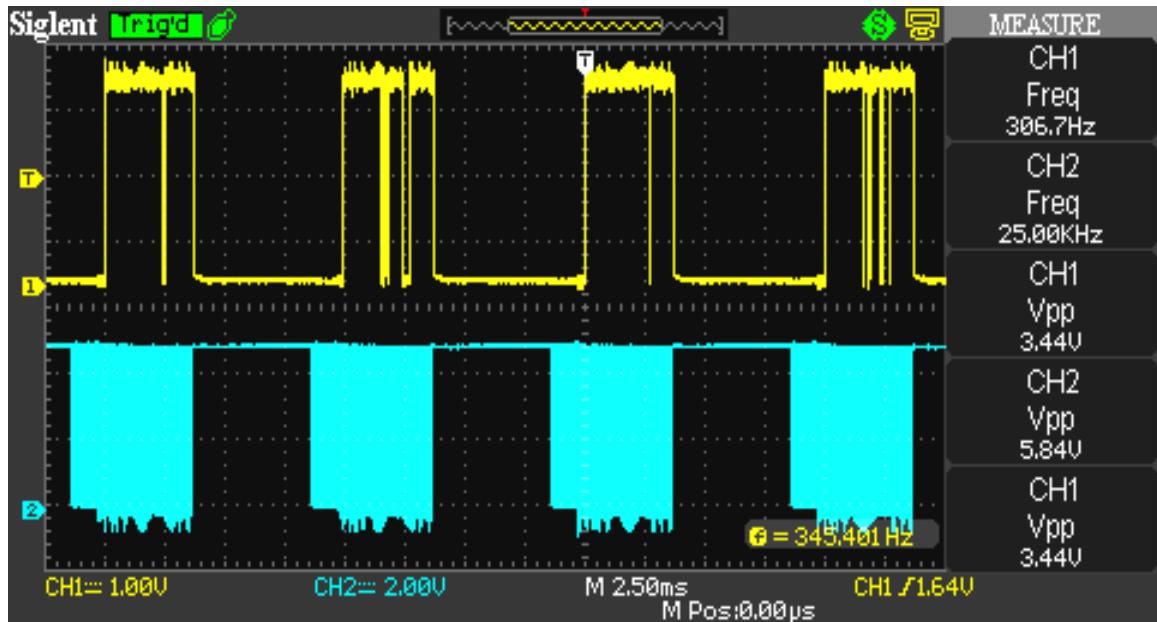


Figure 113: Modulated Output and Demodulated signal for same tuned circuit

Low pass filter was changed to 2.2 nF capacitor keeping the series resistor same and the output was observed. Above issue was solved to up to a certain extend. During the state 1 the density of top edge was high. This was an issue for identifying the state 1. So the signal have to be conditioned further

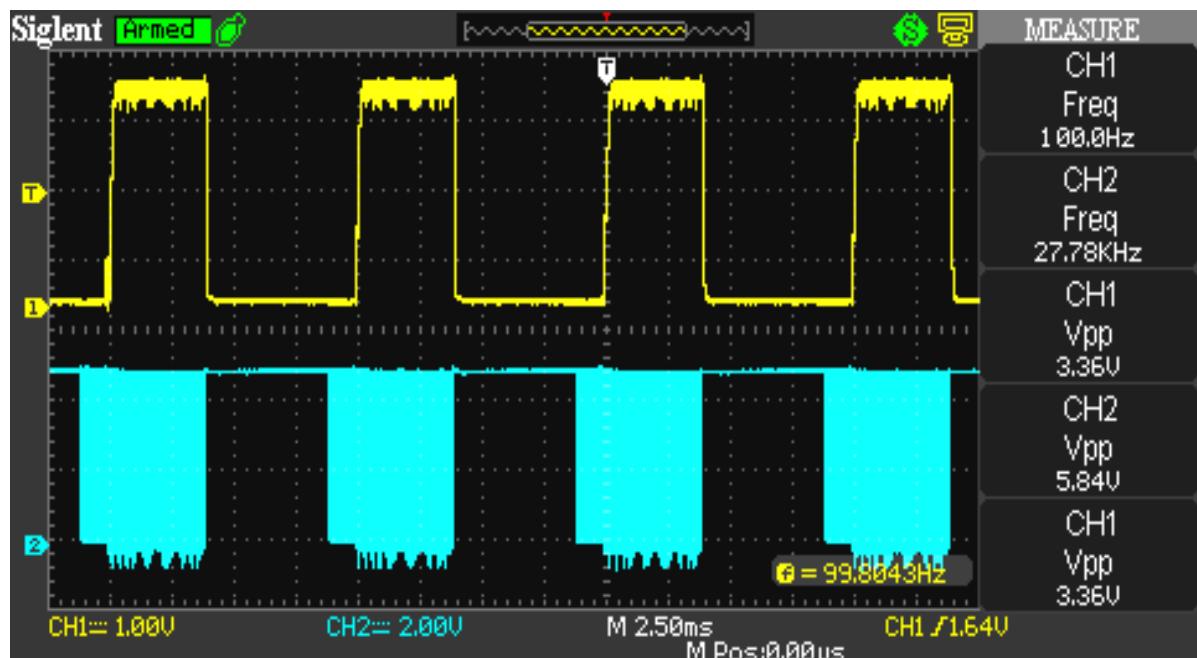


Figure 114: Modulated Output and Demodulated signal for same tuned circuit

Resister to pin 10 (demodulator output pin) was reduce to remove the density are and could to get a slim state 1.

Successfully demodulation was done.

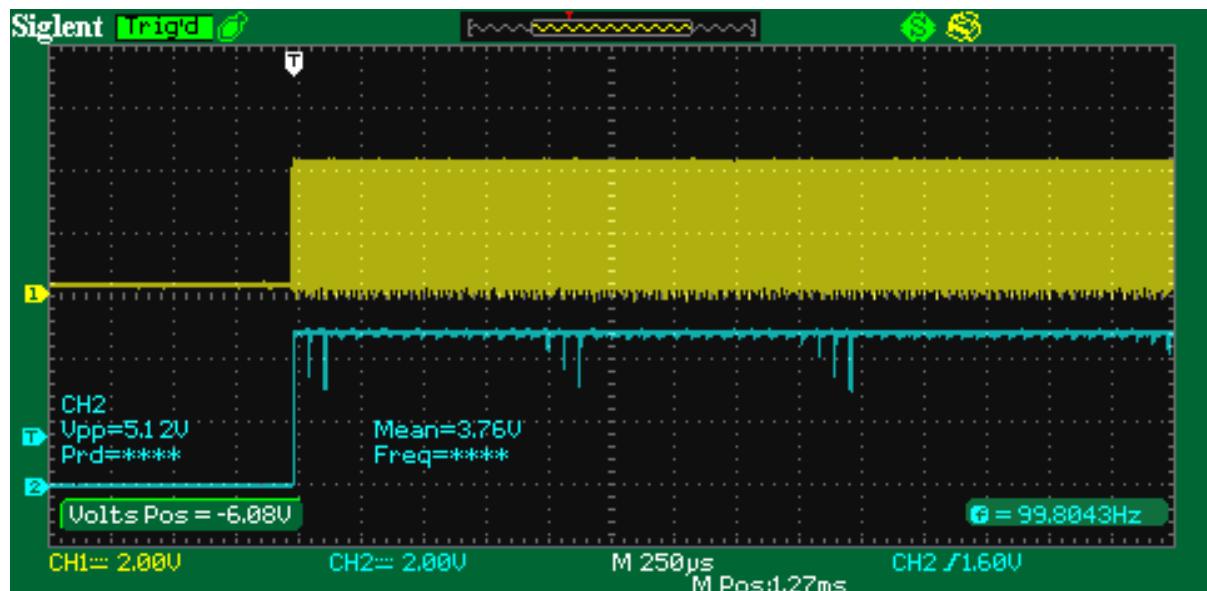


Figure 115: Demodulated output with a slim state 1

Output demodulator with the disturbances from grid (when phone charger or router was plugged).

Sometimes this was an issue for identifying the bit pattern.

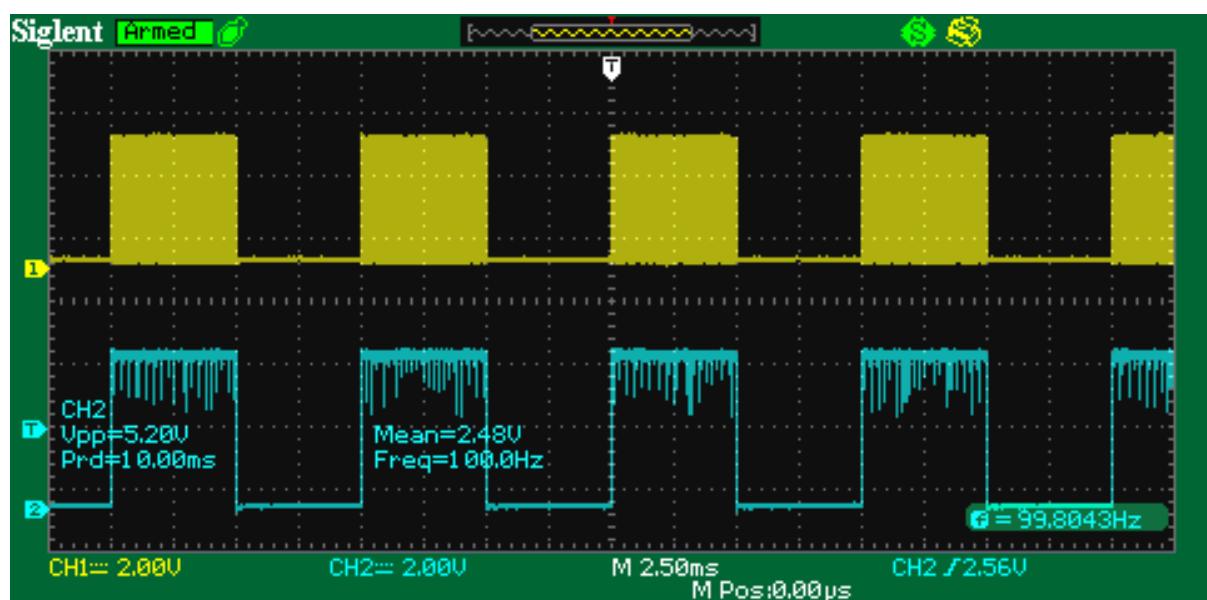


Figure 116: Demodulated output with disturbance

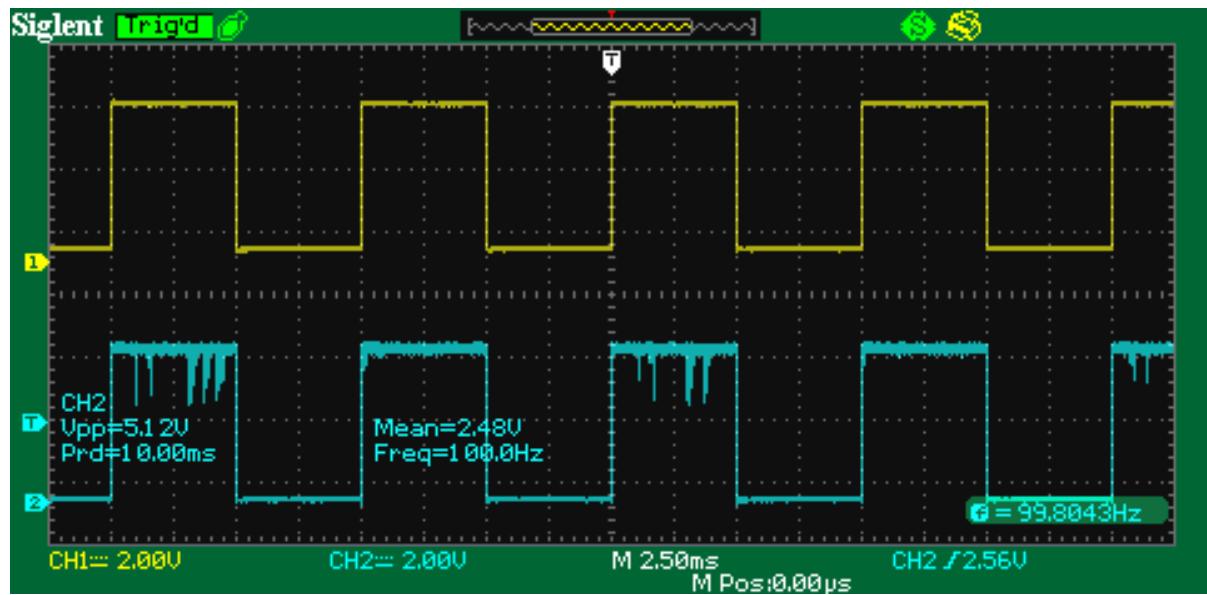


Figure 117: Demodulated output comparing to the original input signal

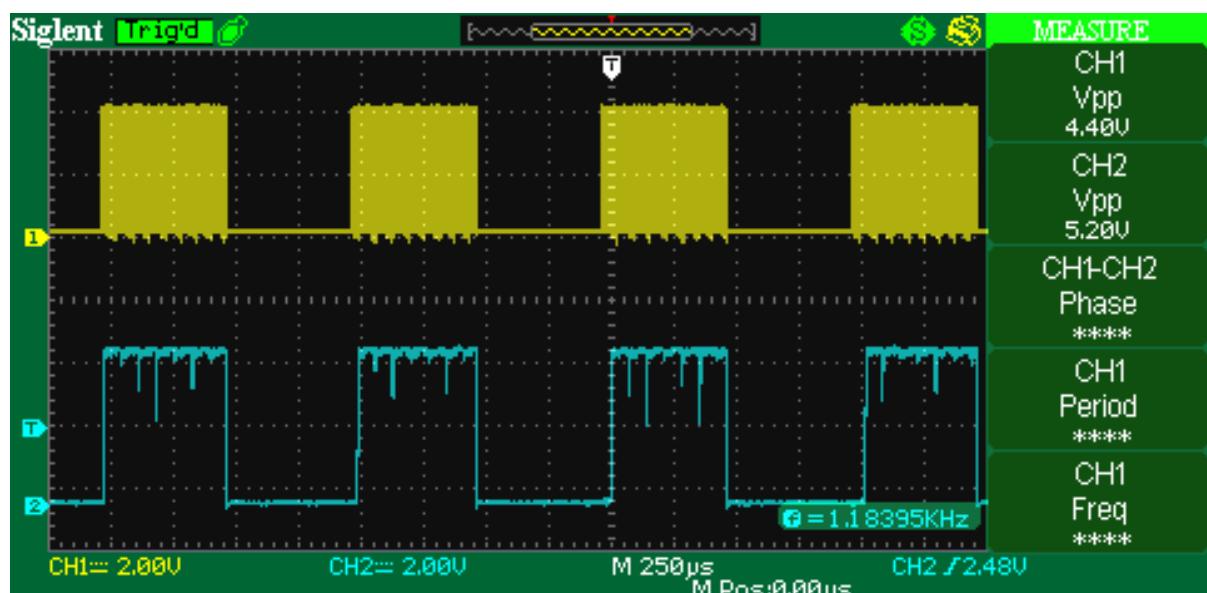


Figure 118: demodulated output comparing to the modulated signal from sender

Conclusion:

1. Signal can be demodulated using this method and when there are disturbances there are some issues and it is needed to be addressed in future.

2.2.15 Test 15: Synchronization between software and hardware

Equipment:

- Node MCU
- Push button

Software:

- Arduino IDE
- Firebase
- Flutter

Theory:

Firebase is a free cloud for Real-time database handing. The unit have to be controlled remotely and with the push button in it. An algorithm had be developed for synchronizing the value from push button and the mobile application. The values from the push button and application was passed to firebase and the data in firebase will pass to the nodemcu always. So the algorithm will identify which get changed (push button or the mobile app button) and pass the appropriate values for their status to be changed.

Simple logic for identifying and pass the status,

```
void check_the_state() {

    if(Read_from_firebase==1) {
        k=5 ;
    }else {
        k=3;}
    if(push_button_status==1){
        l=4 ;
    }else {
        l=7;}
    if(Read_from_firebase == push_button_status){
        ad1=l+k ;
    }else{
        ad2=l+k ;
    }
    if(ad1==10 && ad2==7 ){
        Read_from_firebase=1;

        if(Firebase.setInt(firebaseData, "/LED01", 1))
        { }else{ }
        swich_on();
        ad2=0;
    } else if(ad1==9 && ad2==12){

        Read_from_firebase=0;
        if(Firebase.setInt(firebaseData, "/LED01", 0))
        { }else{ }
        swich_off();
        ad2=0;
    } else if(ad1==10 && ad2==12){

        push_button_status=1;
        swich_on();
        ad2=0;
    } else if(ad1==9 && ad2==7){
        push_button_status=0;
        swich_off();
        ad2=0;
    }
}
```

Procedure:

1. Value of the push button was passed to the firebase via NodeMcu.
2. Code was changed in the mobile application to toggle real-time (set state) when the firebase value was changed.
3. Another option was added in app to change the value in firebase when the app button toggle.
4. Value in firebase was passed to Nodemcu and start to send the bit pattern with the state of 1 in firebase.
5. Problem was detected when simultaneously app button and push button is pressed.
6. Develop the above algorithm step by step to overcome this issue.

Discussion:

Design of the Mobile Application,



Figure 119: Design of the Mobile Application

OFF and ON State of the Button,

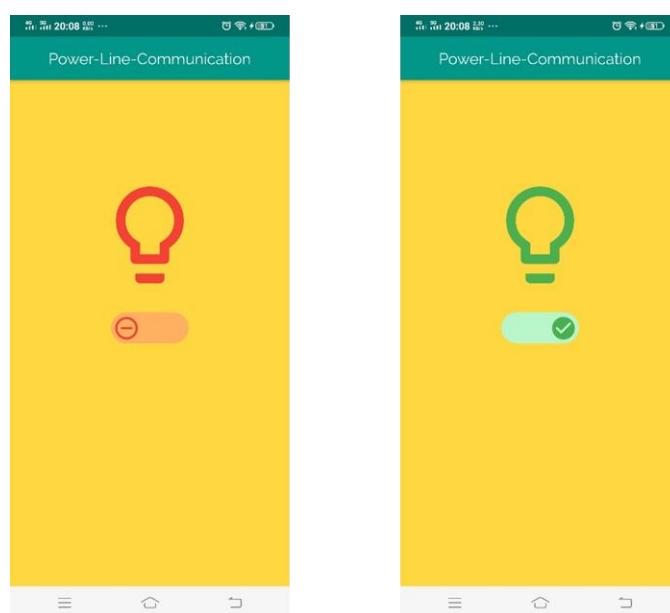


Figure 120: OFF and ON State of the Button

3 Finishing and Packaging

3.1 Finishing

PCB Design,

Breadboards are great for prototyping circuits, but they aren't so good for actually using the thing that is building. At some point, it will be probably needed to make a project more permanent. The best way to do that is to put it on a PCB.

In the design it has been divided to 6 PCB designs. This is because for the easiness of the identification of the components and for a better way of packaging the circuits.

3.1.1 Sender

3.1.1.1 Sender Isolator

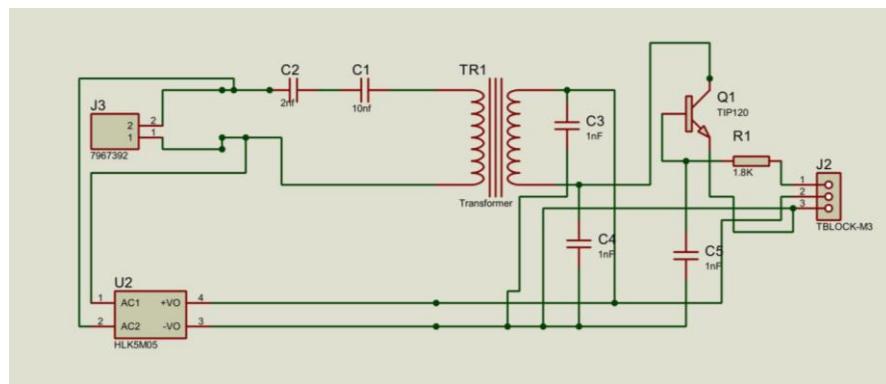


Figure 121: Sender Isolator Schematic

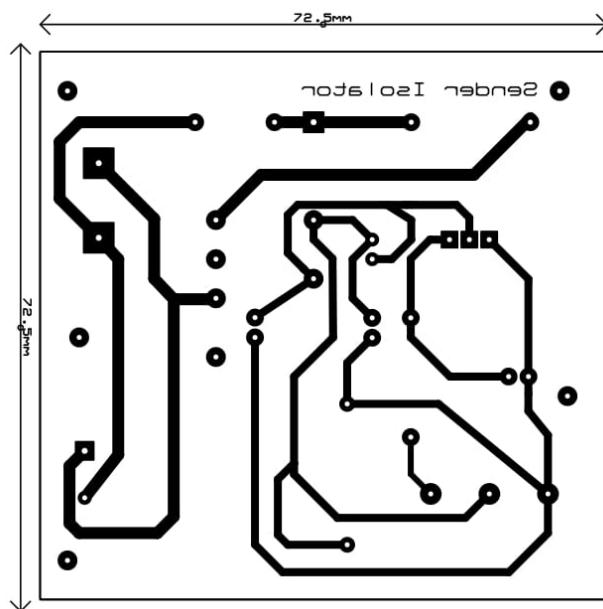


Figure 122: Sender Isolator PCB

3.1.1.2 Sender Chip

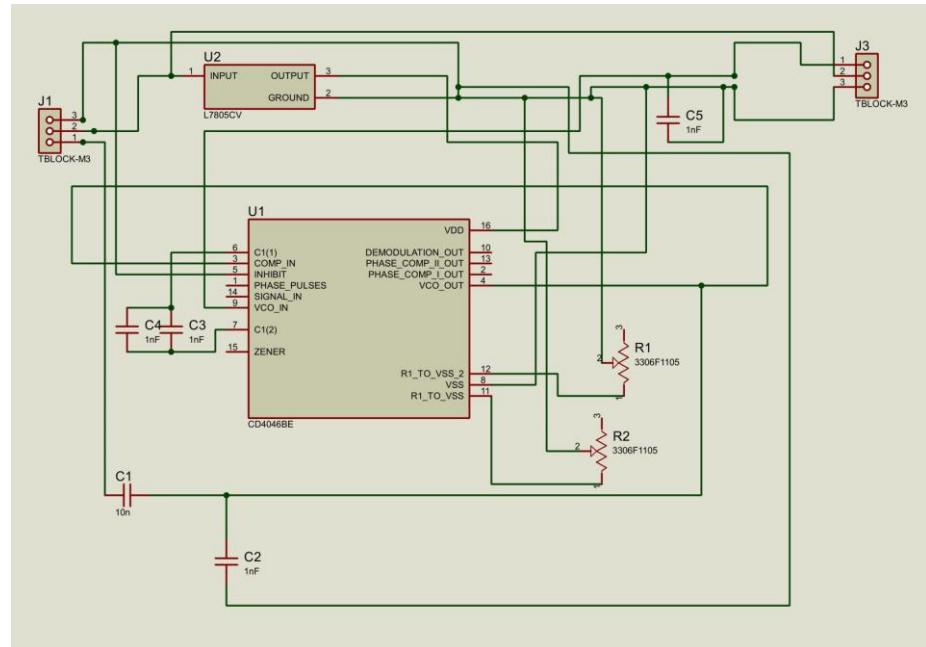


Figure 123: Sender Chip Schematic

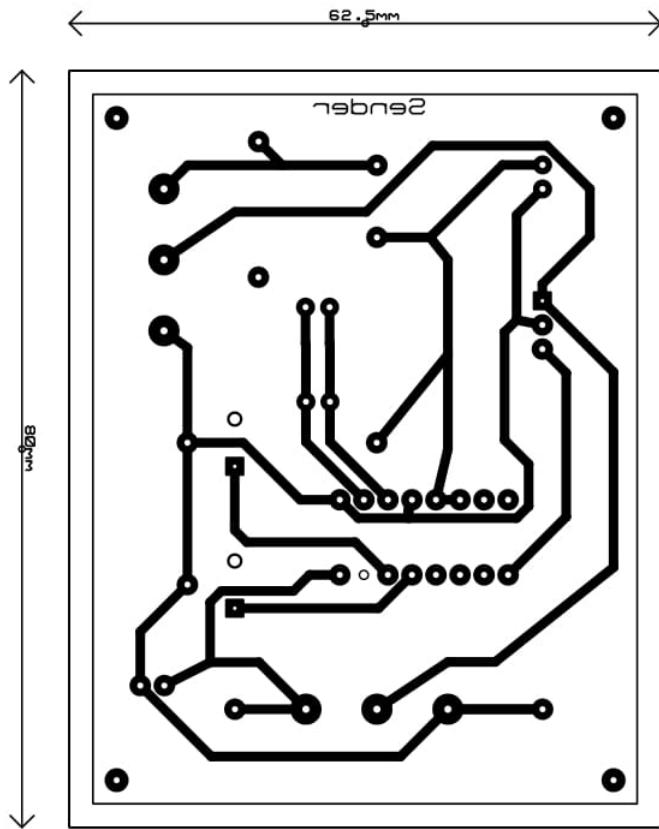


Figure 124: Sender Chip PCB

3.1.1.3 Sender IC

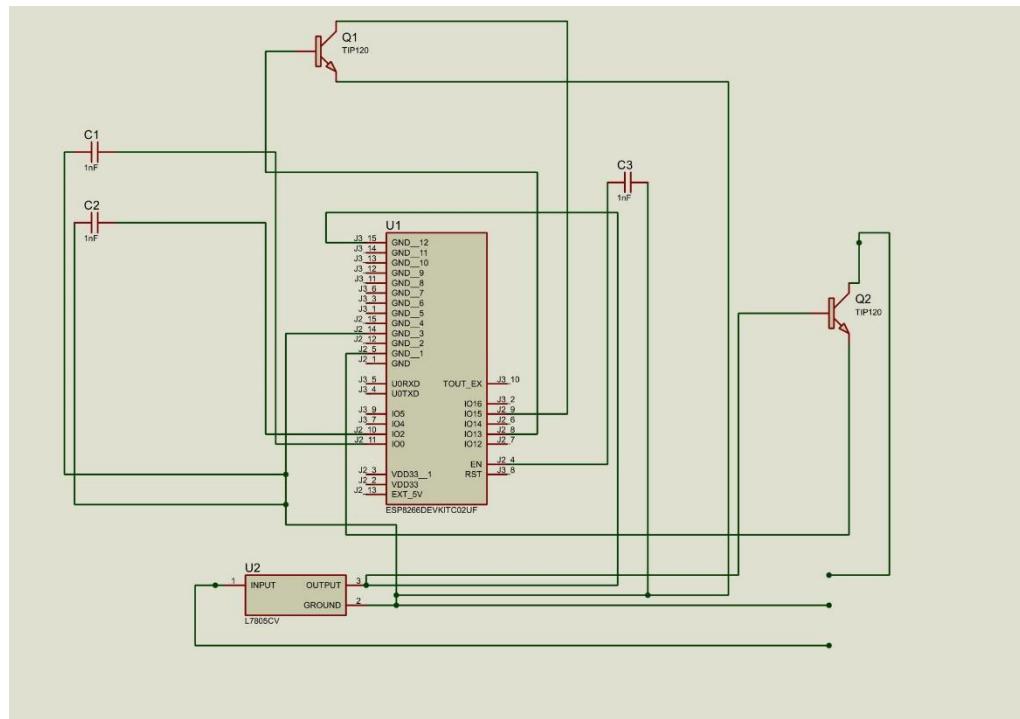


Figure 125: Sender IC Schematic

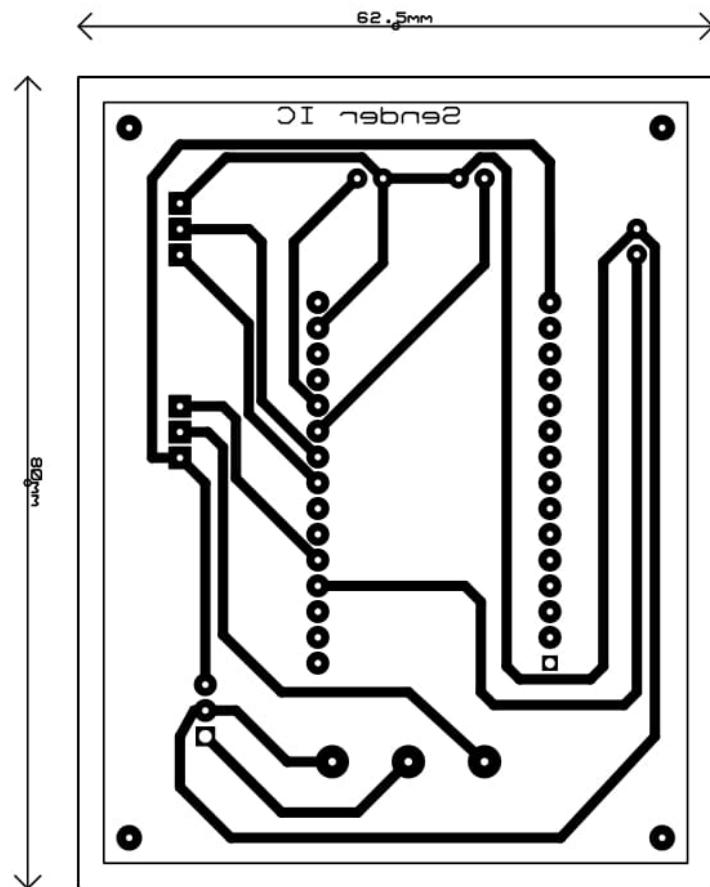


Figure 126: Sender IC PCB

3.1.2 Receiver

3.1.2.1 Receiver Isolator

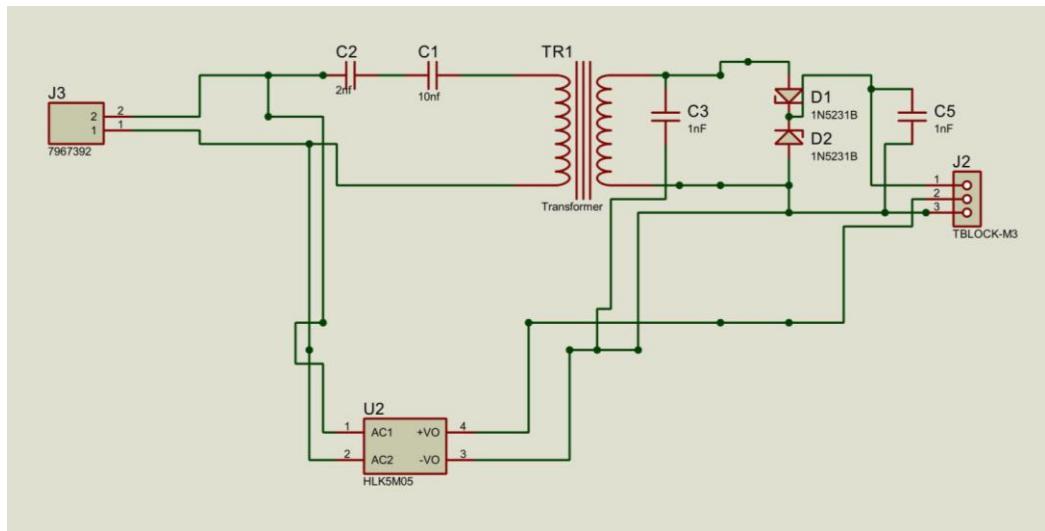


Figure 127: Receiver Isolator Schematic

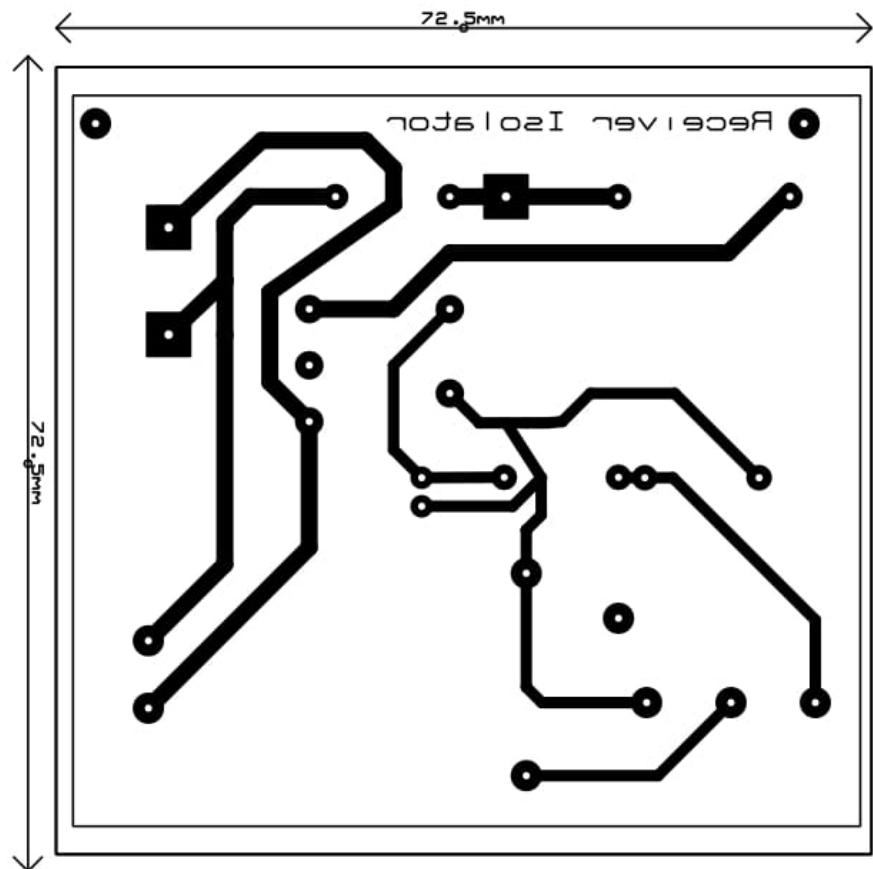


Figure 128: Receiver Isolator PCB

3.1.2.2 Receiver Chip

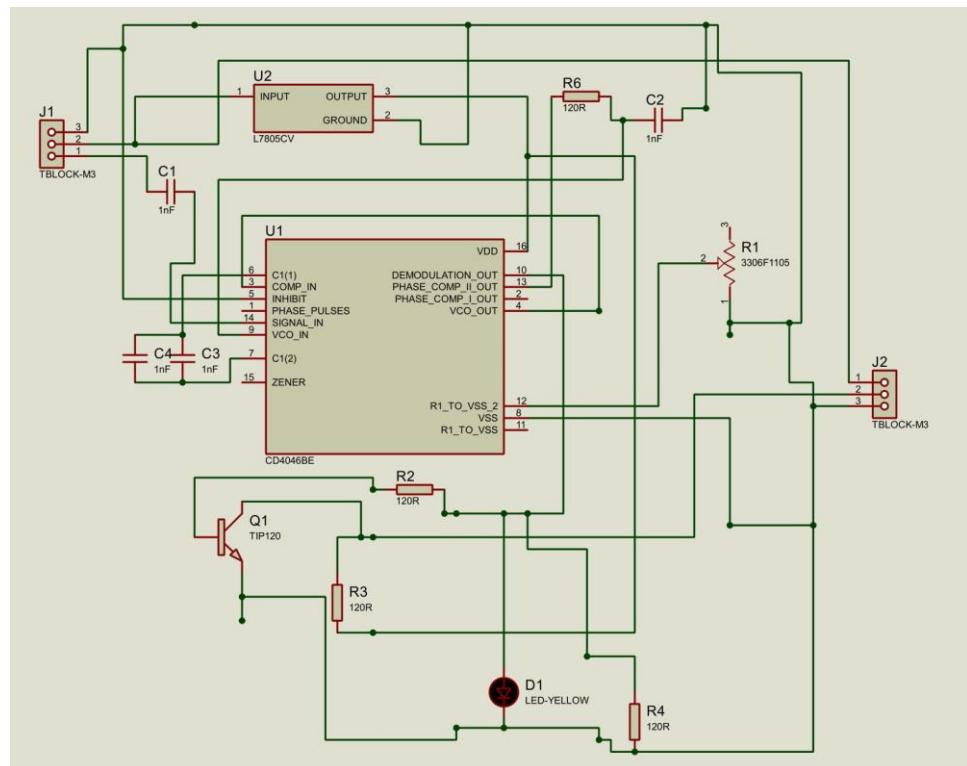


Figure 129: Receiver Chip Schematic

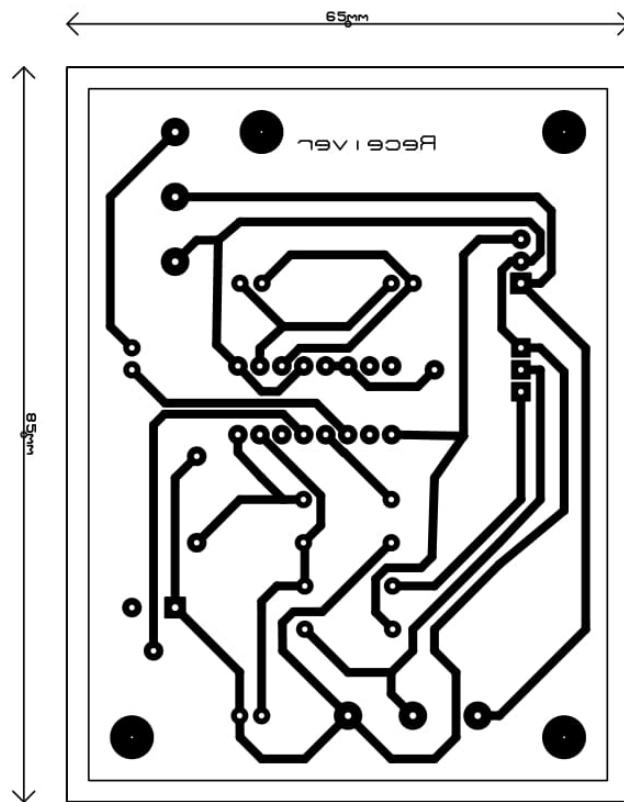


Figure 130: Receiver Chip PCB

3.1.2.3 Receiver IC

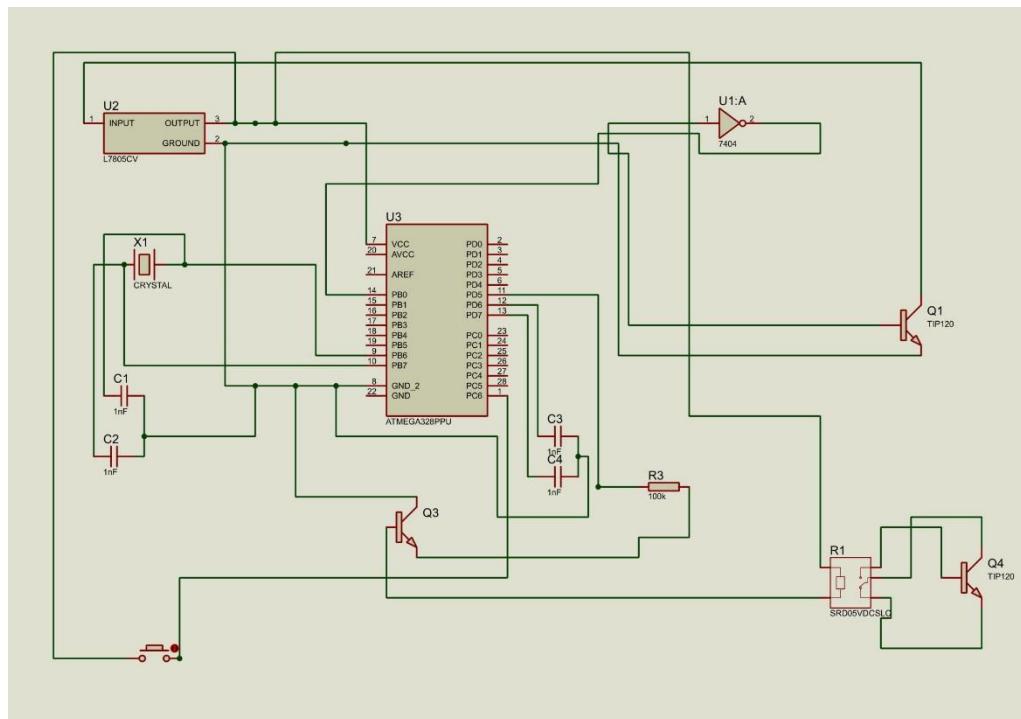


Figure 131: Receiver IC Schematic

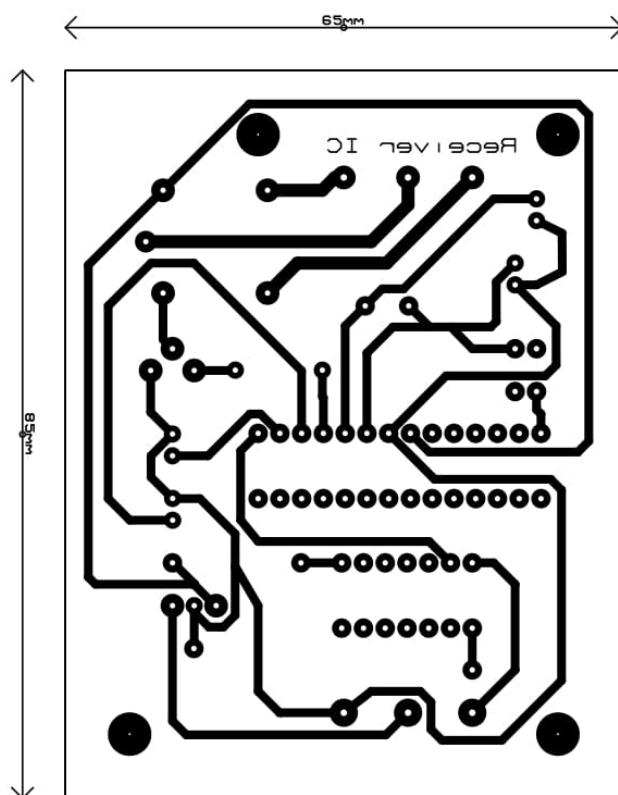


Figure 132: Receiver IC PCB

3.2 Packaging

As the main target was to make an Industry level Product proper packaging was also one of the main focuses. PCB was also designed in a way that can be arranged in a compacted way in a plastic box. In the final stage the 3D printing was not attained and still a proper packaging was done using PCB, Plastic boxes, spacers, terminal boxes, plug tops, plug bases, etc.

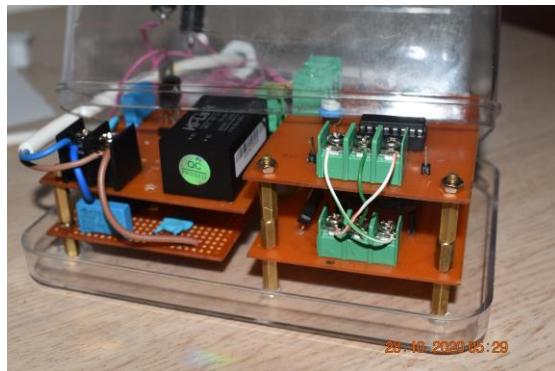


Figure 133: Final Packaging inside Sender and Receiver



Figure 134: Final Packaging outside Sender and Receiver

4 Project management.

4.1 Project Tasks

No.	Task Name	Start Date	End Date	Work Days	Task Allocation	Percent Complete
1	Research about the behavior when inputting and getting output of high frequency low voltage AC and Square signals to Low voltage (Relatively high than the Input) low frequency signal.	Sun 19-12-15	Sat 19-12-21	7	Navod Harshana	100%
2	Research about the behavior when inputting and getting output of high frequency low voltage AC and Square signals to High voltage (Domestic) low frequency signal.	Sun 19-12-22	Sat 19-12-28	7	Navod	100%
3	Research about Power Line Communication	Mon 19-12-16	Sat 20-01-04	16	Harshana	100%
4	Make an electronic circuit that can send controlled high frequency low voltage signal through domestic wiring, collect it from another end and recreate the sent signal.	Mon 19-12-30	Wed 20-01-22	18	Harshana Navod	100%
5	Research about the best modulation method to transmit data through the power network	Sun 20-01-12	Sat 20-03-21	52	Navod Harshana	100%
6	Create a prototype that can send and receive data from one socket to another in a power network.	Sun 20-01-19	Thu 20-04-30	75	Harshana Navod	100%
7	Develop home automation using the technique for an existing wiring of a home.	Sun 20-02-16	Sun 20-05-24	72	Navod Harshana	100%
8	Develop Mobile Application	Tue 20-08-18	Sun 20-10-20	45	Harshana	100%
9	Testing	Sun 20-01-19	Mon 20-10-26	202	Navod Harshana	100%
10	Finishing	Sun 20-08-16	Tue 20-10-27	53	Navod	100%

Figure 135: Task allocation and Completion ratios

4.2 Project Gantt chart with timeline and completion levels

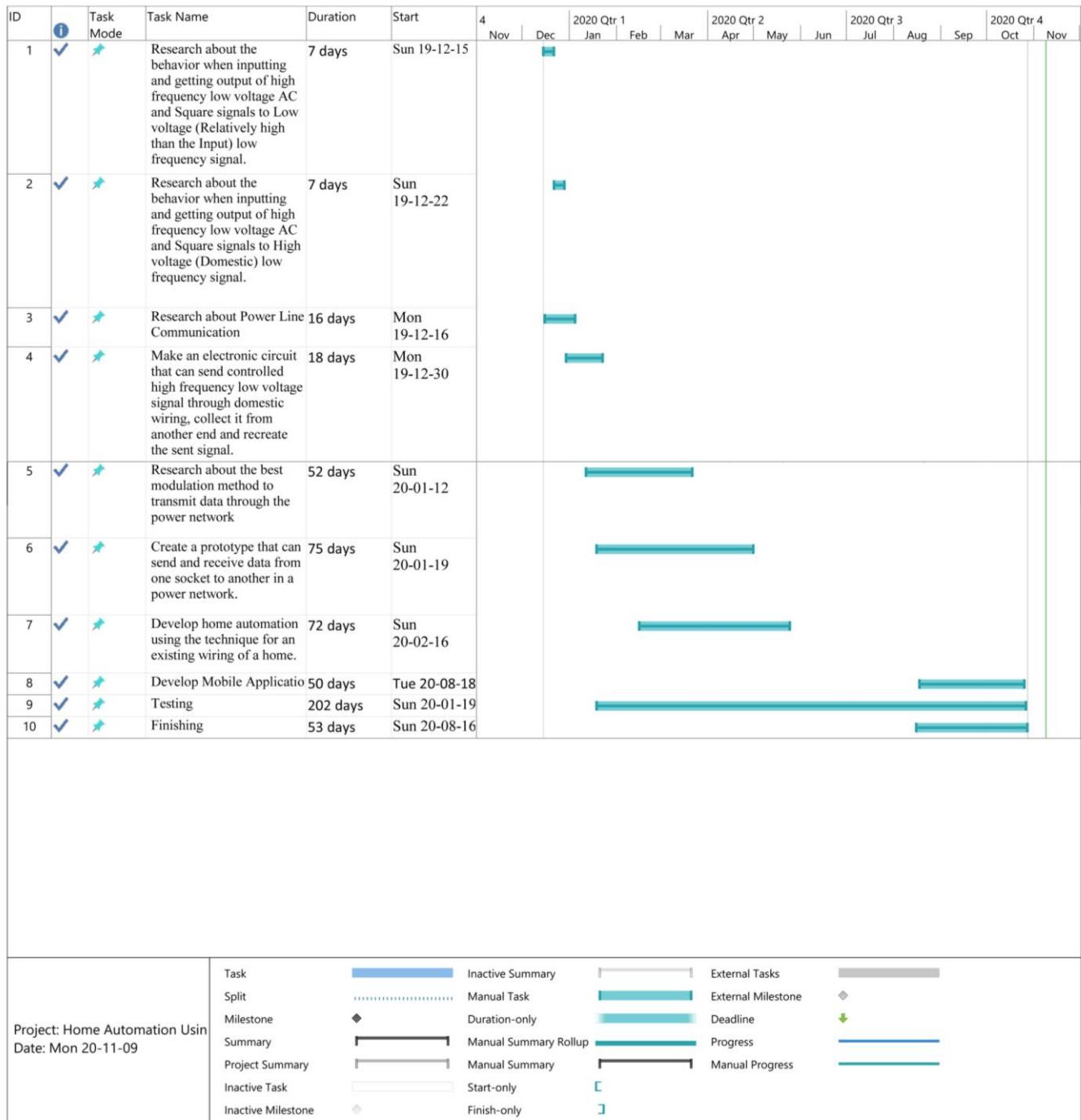


Figure 136: Project Gantt chart with timeline and completion levels

Project testing has been started earlier than expected and the other tasks have been carried according to the planned time line of the project.

4.3 Project Budget

4.3.1 Receiver-

Details	Name	Category Number	Number of units	Unit price (Rs)	Cost (Rs)
Receiver	Capacitors	C1 - 1 uF	1	5	5
		C2 - 1 uF	1	5	5
		C3 - 0.004 mF	1	5	5
		C4 - 2.2 uF	1	5	5
		C5 - 1 pF	1	2	2
		C6 - 100 nF + 2 nF	2	15	30
		C7 - 22pF	2	0.5	1
	Transistors	C828	1	4	4
		TIP120	1	40	40
	Resistors	20K pot	2	5	10
		10k	1	1	1
	Other	Transformer	1	200	200
		Relay 5V	1	50	50
		Hilink-5m05	1	750	750
		LED	3	3	9
		16MHz crystal	1	20	20
		L7805	2	15	30
	IC	IC7404	1	5	5
		CD4046	1	20	20
		Atmega 328P	1	350	350
		IC Base	4	5	20
	Finishing	PCB board	3	360	1080
		Plastic Box	1	150	150
		Spacers	12	15	180
		T block (3)	5	15	75
		T block (2)	1	15	15
		Plug Top	1	220	220
		Wire - 1.5m	1	100	100
		Plug base	1	400	400
	Total				3,782

Table 3: Budget for the Receiver

Total Cost for the Receiver is Rs. 3782/=

4.3.2 Transmitter-

Details	Name	Category Number	Number of units	Unit price (Rs)	Cost (Rs)
Transmitter	Capacitors	C1 - 1uF	1	5	5
		C2 - 102	1	2	2
		C3 - 102	1	2	2
		C4 - 2nF +100 nF	2	15	30
	Resistors	20K pot	2	5	10
		50K pot	1	5	5
	Transistors	TIP120	1	40	40
	IC	CD4046	1	20	20
		IC Base	1	5	5
	Controller	Nodemcu	1	900	900
	Other	Transformer	1	200	200
		Hilink-5mo5	1	750	750
		L7805	2	15	30
		LED	4	3	12
	Finishing	PCB Boards	3	360	1080
		Push Button	2	10	20
		T block (3)	4	15	60
		T block (2)	1	15	15
		Spacers	12	15	180
		Plastic Box	1	150	150
		Plug Top	1	220	220
		Wire - 1.5m	1	100	100
		Female rails	2	25	50
Total					3,886

Table 4: Budget for the Transmitter

Total Cost for the Transmitter is Rs. 3886/=

4.3.3 Manufacturing Cost -

Details	Cost (Rs)
Receiver	3782
Transmitter	3,886
Other	200
Total Cost	7868

Table 5: Total Manufacturing Cost

Total Manufacturing Cost is Rs. 7868/=

4.3.4 Total Cost of Project-

Details	Name	Category Number	Number of units	Unit price (Rs)	Cost (Rs)
All	Capacitors	C1 - 1 uF	4	5	20
		C2 - 1 uF	4	5	20
		C3 - 0.004 mF	4	5	20
		C4 - 2.2 uF	4	5	20
		C5 - 1 pF	4	2	8
		C6 - 100 nF + 2 nF	4	15	60
		C7 - 22pF	4	0.5	2
	Inductor				
		56 uF	4	15	60
	Transistors	C828	4	4	16
		TIP120	10	40	400
	Resistors	20K pot	10	5	50
		10k	10	1	10
		50K pot	10	5	50
	Other	Transformer	6	200	1200
		Relay 5V	2	50	100
		Hilink-5m05	2	750	1500
		Hilink-12m05	2	510	1020
		LED	10	3	30
		16MHz crystal	2	20	40
		L7805	10	15	150
		Toggle Switch	3	5	15
		Dot Board	6	50	300
		Lead	1	100	100
	IC	IC7404	3	5	15
		CD4046	10	20	200
		Atmega 328P	2	350	700
		IC Base	10	5	50
		Nodemcu	1	900	900
		LM567-CM	10	20	200
	Finishing	PCB board	9	360	3240
		Plastic Box	2	150	300
		spacers	35	15	525
		T block (3)	14	15	210
		T block (2)	6	15	90
		Plug Top	2	220	440
		Wire - 1.5m	2	100	200
		Push Button	5	10	50
		Plug base	1	400	400
		Female rails	4	25	100
Total					12,711

Table 6: Total Budget

4.3.5 Initial Budget plan:

Details		Number of units	Unit price	cost
Main Board	Raspberry Pi Board	1	9000	9000
	Display and Electronic equipment	1	6000	6000
Slave Devices	Electronic Equipment	2	5000	10000
Finishing				5000
Total				30000

Table 7: Initial Budget plan

Initial plan has not been exceeded.

At the end values can be seen to lower than estimations due to some conditions,

1. Usage of Microprocessor Raspberry Pi Board has not yet been done because of the usage of NodeMCU.
2. Display has not yet been used.
3. Finishing Costs has been lower because 3D printing was not done
4. Most of the Electronic Components have been bought from Pettah for low bulk prices.

5 Individual components

5.1 Description of the individual component

When conducting a Project, arranging tests is a must in order to check whether hypothesizes that has been set are right or wrong. Also, when conducting such tests, results that has not been considered can be observed and that can lead for developments that was not planned. Arranging such tests improves the thinking pattern, pre planning skills and organizing skills of an engineer. Up to now 15 tests has been arranged and for each test the observations and the conclusions of the previous tests has been used as inputs.

Checking the ability of superimposing one signal on to another was the major task in the beginning. For that research about the behavior when inputting a high frequency low voltage AC and Square signals to Low voltage (Relatively high than the Input) low frequency signal had to be done. For that the test 1 was arranged. As planned the outcome came and it confirmed that two signals can be superimposed according to the plan. Issue was to directly checking this method with the Domestic power. For that implementing Transformers was done in the Test 2, research about the behavior when inputting of high frequency low voltage AC and Square signals to High voltage (Domestic) low frequency signal.

The impact of 50Hz signal didn't allow the high frequency to pass and increasing the frequency had to be done. Also, a mechanism to cut off the 50Hz signal had to found. Test 3 and 4 were arranged to check the impact of increasing the input frequency. Was able to identify there is an impact of the transformer type and has to do further research on them. Issue was to find proper RF transformers in the Sri Lanka. For the Stage 1 transformers from Old phone chargers were removed and used till finding proper once.

In Test 3, it was not able to see the both signals from output when the first input is the Domestic Signal. This could lead to a severe issue because the domestic signal is already in the system. But in Test 4 this issue was not occurred and that concluded that higher the frequency the result is better.

As shown in the results of the previous tests a solution for the issue of having the 50Hz signal had to be taken. In Test 5, a filter was designed using the simulations of OrCAD Capture CIS – Lite Software. It was set and tested. Still the signal was not cut-offed and as a solution the capacitance was increased. This could be because of the transformer inductance and due to the lack of a proper transformer this was agreed to be kept for the first stage.

After the previous tests most of the basic issues were cleared for the first stage. The optimum frequency for transmitting through the filter in the range of 300 kHz – 500 kHz was to be found. For that the Test 6 was arranged and found out that 470 kHz is the optimum frequency to transmit in the arrangement. During the Test it can be seen that harmonics of the sending signal were occurred. Also, the Gain of the 2nd harmonic was lower than the Original signal and 3rd Harmonic. This need to be Clarify in the next stage.



Figure 137: Output from filter for 300 kHz and 500 kHz

As per the Optimum Frequency was set to be 470 kHz, in Test 6 CD4046 was arranged accordingly and set to send the frequency. Output was checked and sudden drop and rise of the voltage and the frequency of signal can be seen.

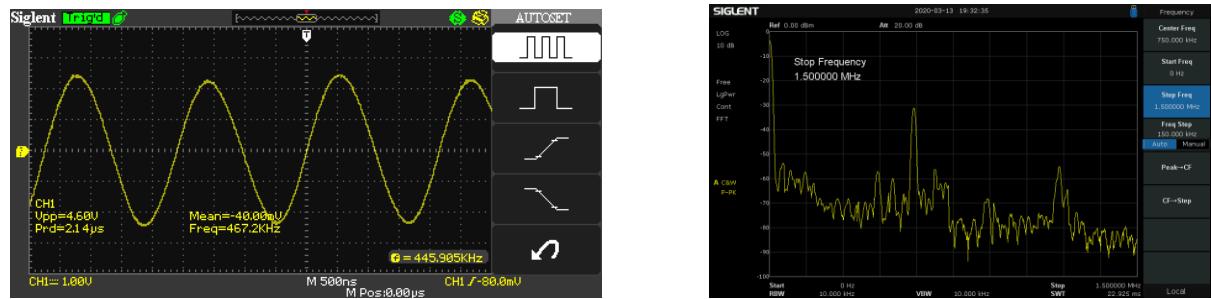


Figure 138: Output with the Signal

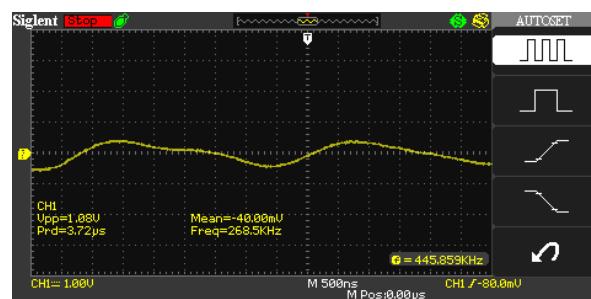


Figure 139: Output when the sudden drop occurs

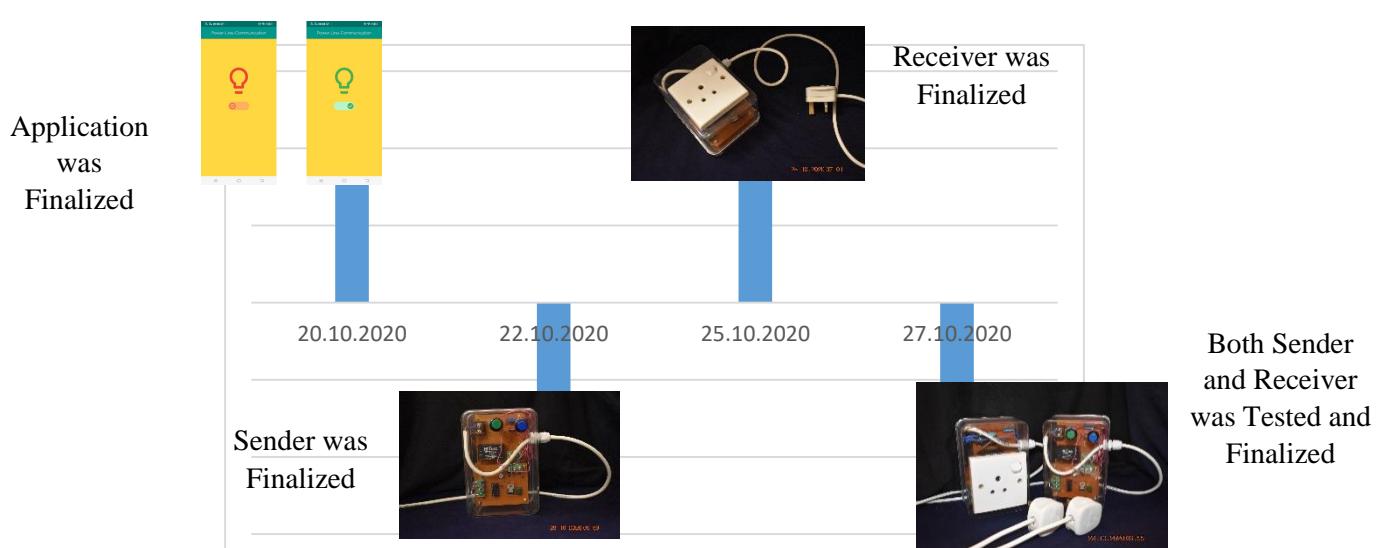
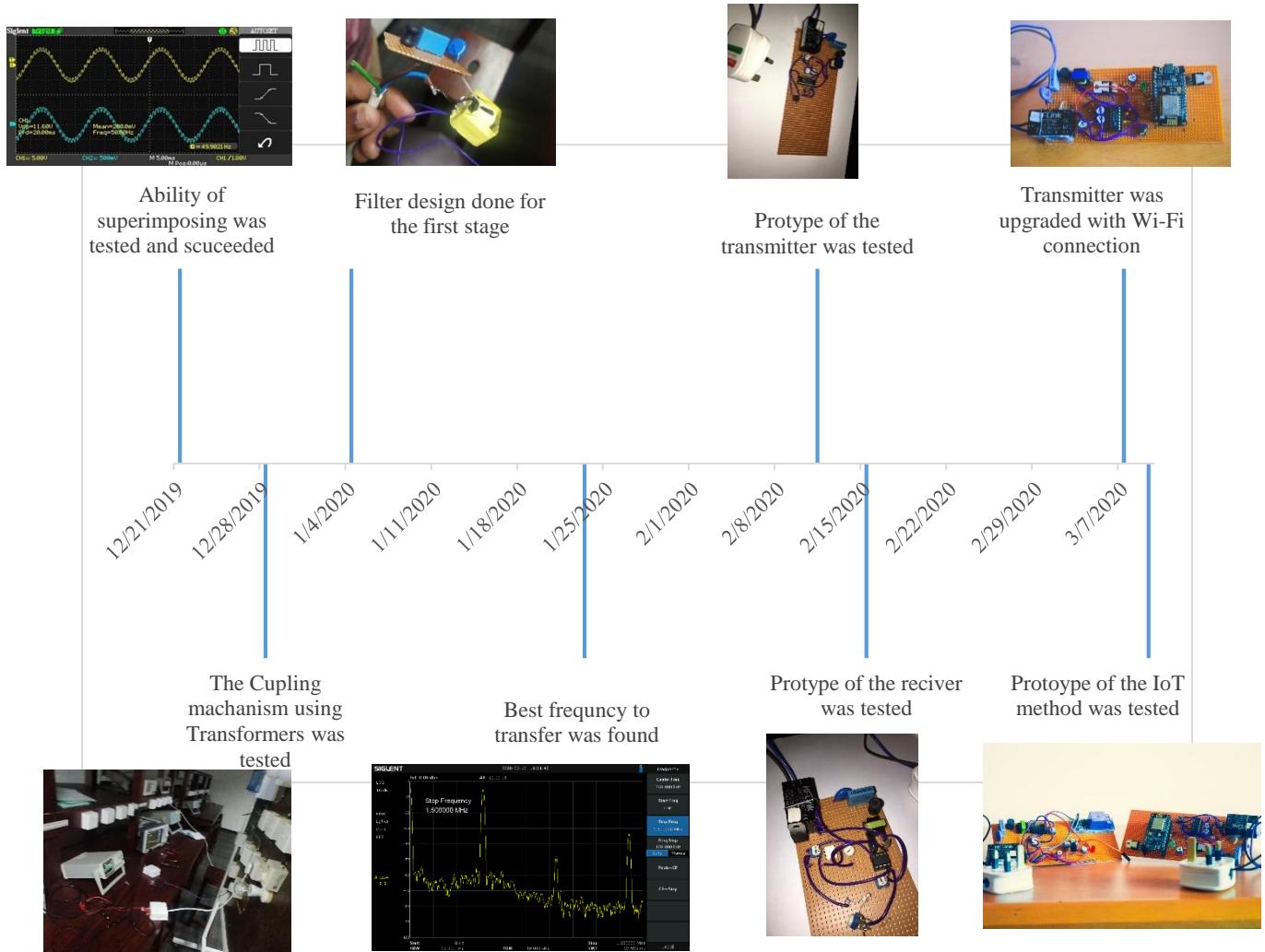
A study to identify the reason for this drop must be done. For now, an assumption can be made as the oscilloscope cannot detect the sudden variation of the Gain of the signal.

5.2 Individual budget

	Details	Date	Amount	Total
Income	Contribution from Navod	16/12/2019	1500	13000
	Contribution from Harshana	16/12/2019	1500	
	Contribution from Harshana	25/02/2020	1000	
	Contribution from Navod	25/02/2020	1000	
	Contribution from Harshana	2/3/2020	2000	
	Contribution from Navod	20/9/2020	2000	
	Contribution from Harshana	3/10/2020	2000	
	Contribution from Navod	23/10/2020	2000	
Expenses	Visit 1 to Pettah	7/1/2020	730	12711
	Visit 2 to Pettah	12/2/2020	1465	
	Visit 3 to Pettah	25/02/2020	2047	
	Visit 4 to Kegalle	2/3/2020	145	
	Visit 5 to Kegalle	20/9/2020	2350	
	Visit 6 to Pettah	3/10/2020	2274	
	Delivered Goods	23/10/2020	3700	
Cash in hand		25/10/2020		289

Table 8: Individual budget

5.3 Gantt chart showing milestones.



6 Discussion on the project

6.1 Final Stage

Sender and the receiver were completed to transfer and receive a bit pattern. Different periods for signal and duty cycle were tested for accurate transferring and receiving. Finally, 100 milli second of period and 50% of duty cycle were selected.

2 messages of 8 bits were arranged to transmit, one for "switch on" other for "switch off". A start bit of '1' was sent first to start the receiving processes and detect the bit pattern.

6.1.1 Sending the bit pattern for "switch on",
{11001011}

```
void swich_on() {  
  
    byte stream[8] ={1,1,0,0,1,0,1,1};  
  
    digitalWrite(D4 ,HIGH);  
    digitalWrite(D3 ,HIGH);  
    delay(100);  
  
    for(int i=0; i<8 ; i++)  
    {  
  
        digitalWrite(D4 ,stream[i]);  
        digitalWrite(D3 ,stream[i]);  
        delay(100);  
    }  
    digitalWrite(D4 ,LOW);  
    digitalWrite(D3 ,LOW);  
    digitalWrite(D7 ,HIGH);  
    //    delay(100);  
    //counter =2;  
}
```

6.1.2 Sending the bit pattern for "switch off",
{01110111}

```
void swich_off(){

    byte stream1[8] = {0,1,1,1,0,1,1,1};

    digitalWrite(D4 ,HIGH);
    digitalWrite(D3 ,HIGH);
    delay(100);

    for(int i=0; i<8 ; i++)
    {
        //  Serial.print (stream1[i]);
        digitalWrite(D4 ,stream1[i]);
        digitalWrite(D3 ,stream1[i]);
        delay(100);
    }
    digitalWrite(D4 ,LOW);
    digitalWrite(D3 ,LOW);
    digitalWrite(D7 ,LOW);
    // delay(100);
    // counter =0 ;
}
```

6.1.3 Detection of the bit pattern,

```
first_bit = digitalRead(8);
digitalWrite(7,digitalRead(8));
delay(100);
if(first_bit==1){
    to_while = true ;
    while(to_while){
        input_data = digitalRead(8);
        digitalWrite(7,digitalRead(8));

        if(bit_count < 9){
            inputbuffer[bit_count]=input_data ;
            Serial.print(input_data);
        }
        bit_count =bit_count+1 ;
        if(bit_count ==8){
            to_while = false ;
            bit_count =0 ;
        }
        delay(100);
    }
}
```

The bit pattern sent was detected and save in an array (inputbuffer). Array was compared with conditions and a state of 1 and 0 was given as output.



Figure 142: Sender when sending the bit pattern



Figure 143: Final Receiver



Figure 144: Final Product

6.2 Plans for the future implementation

6.2.1 Message Transferring

Still the circuit could clearly pass only a one state and it was assumed that not having the state is the inverse state, have to design for transferring at least 2 states, "1", "0" clearly. 2 frequencies should introduce for both separate as the basic concept in FSK modulation (FSK - frequency shift keying)

According to the planed output, a suitable protocol must be chosen. In the beginning X10 was chosen because it is simple. But using that technique cannot give the targeted product. Therefore, must go for I2C, and it is a duplex communication system. [16]

I2C Info – I2C Bus, Interface and Protocol

I2C is a serial protocol for two-wire interface to connect low-speed devices like microcontrollers, EEPROMs, A/D and D/A converters, I/O interfaces and other similar peripherals in embedded systems.

I2C bus is popular because it is simple to use, there can be more than one master, only upper bus speed is defined and only two wires are needed to connect almost unlimited number of I2C devices. I2C can use even slower microcontrollers with general-purpose I/O pins since they only need to generate correct start and stop condition in addition to functions for reading and writing a byte.

Each slave device has a unique address. Transfer from and to master device is serial and it is split into 8-bit packets. All these simple requirements make it very simple to implement I2C interface even with cheap microcontrollers that have no special I2C hardware controller. You only need 2 free I/O pins and few simple I2C routines to send and receive commands.

The initial I2C specifications defined maximum clock frequency of 100 kHz. This was later increased to 400 kHz as fast mode. There is also a High-speed mode which can go up to 3.4 MHz and there is also a 5 MHz ultra-fast mode. [16]

I2C uses only two wires: **SCL (serial clock)** and **SDA (serial data)**. Both need to be pulled up with a resistor to +Vdd. There are also I2C level shifters which can be used to connect to two I2C buses with different voltages.

Figure 142 shows how SCL and SDA behave in I2C protocol.

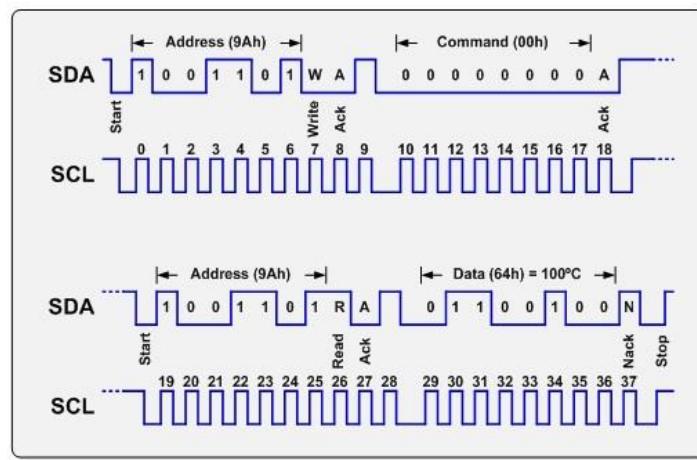


Figure 145: SCL and SDA behavior in I2C protocol

Signals coming from SDA and SCL should send separately at same time by PLC modem. So 4 frequency bands should introduce.

Example,

1. 100 kHz ----> SDA state 1
2. 200 KHz ----> SDA state 0
3. 300 KHz ----> SCL state 1
4. 400 KHz ----> SCL state 0

For both side of modem there should be a receiver circuit and the transmitting circuit.

To detect the frequencies (phase lockers) one modem needs 4 LM567

For transmitting 2 CD4046 will enough.

6.2.2 Check for Impacts of Harmonics

Harmonics are AC voltages and currents with frequencies that are integer multiples of the fundamental frequency. On a 50-Hz system, this could include 2nd order harmonics (100 Hz), 3rd order harmonics (150 Hz), 4th order harmonics (200 Hz), and so on. These can lead to capacitor failure due to harmonic resonance, conductor or transformer failures due to inductive heating, fuses blowing for no apparent reason but due to inductive heating and overload, motor failures due to overheating and voltage drop or overheating of metal enclosures due to inductive heating. [17]

As shown in the Test 6 which was arranged to find the optimum frequency to transmit in the arrangement, it can be seen that harmonics of the sending signal were occurred. Also, the gain of the 2nd harmonic was lower than the original signal and 3rd Harmonic. This need to be Clarify in the next stage. After testing whether the designed signal transmitter does the same, a band pass filter must be designed to clear this issue.

Band Pass filter,

Band Pass Filters can be used to isolate or filter out certain frequencies that lie within a particular band or range of frequencies. The cut-off frequency or f_c point in a simple RC passive filter can be accurately controlled using just a single resistor in series with a non-polarized capacitor, and depending upon which way around they are connected, we have seen that either a Low Pass or a High Pass filter is obtained.

One simple use for these types of passive filters is in audio amplifier applications or circuits such as in loudspeaker crossover filters or pre-amplifier tone controls. Sometimes it is necessary to only pass a certain range of frequencies that do not begin at 0Hz, (DC) or end at some upper high frequency point but are within a certain range or band of frequencies, either narrow or wide.

By connecting or “cascading” together a single Low Pass Filter circuit with a High Pass Filter circuit, we can produce another type of passive RC filter that passes a selected range or “band” of frequencies that can be either narrow or wide while attenuating all those outside of this range. This new type of passive filter arrangement produces a frequency selective filter known commonly as a Band Pass Filter or BPF for short. [18]

Band Pass Filter Circuit

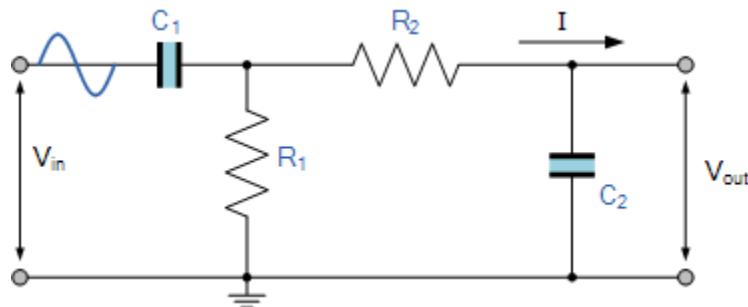


Figure 146: Band Pass Filter Design

Unlike the low pass filter which only pass signals of a low frequency range or the high pass filter which pass signals of a higher frequency range, a Band Pass Filters passes signals within a certain “band” or “spread” of frequencies without distorting the input signal or introducing extra noise. This band of frequencies can be any width and is commonly known as the filters Bandwidth.

Bandwidth is commonly defined as the frequency range that exists between two specified frequency cut-off points (f_c), that are 3dB below the maximum centre or resonant peak while attenuating or weakening the others outside of these two points.

Then for widely spread frequencies, we can simply define the term “bandwidth”, BW as being the difference between the lower cut-off frequency ($f_{c\text{LOWER}}$) and the higher cut-off frequency ($f_{c\text{HIGHER}}$) points. In other words, $BW = f_H - f_L$. Clearly for a pass band filter to function correctly, the cut-off frequency of the low pass filter must be higher than the cut-off frequency for the high pass filter. [17]

The “ideal” Band Pass Filter can also be used to isolate or filter out certain frequencies that lie within a particular band of frequencies, for example, noise cancellation. Band pass filters are known generally as second-order filters, (two-pole) because they have “two” reactive components, the capacitors, within their circuit design. One capacitor in the low pass circuit and another capacitor in the high pass circuit.

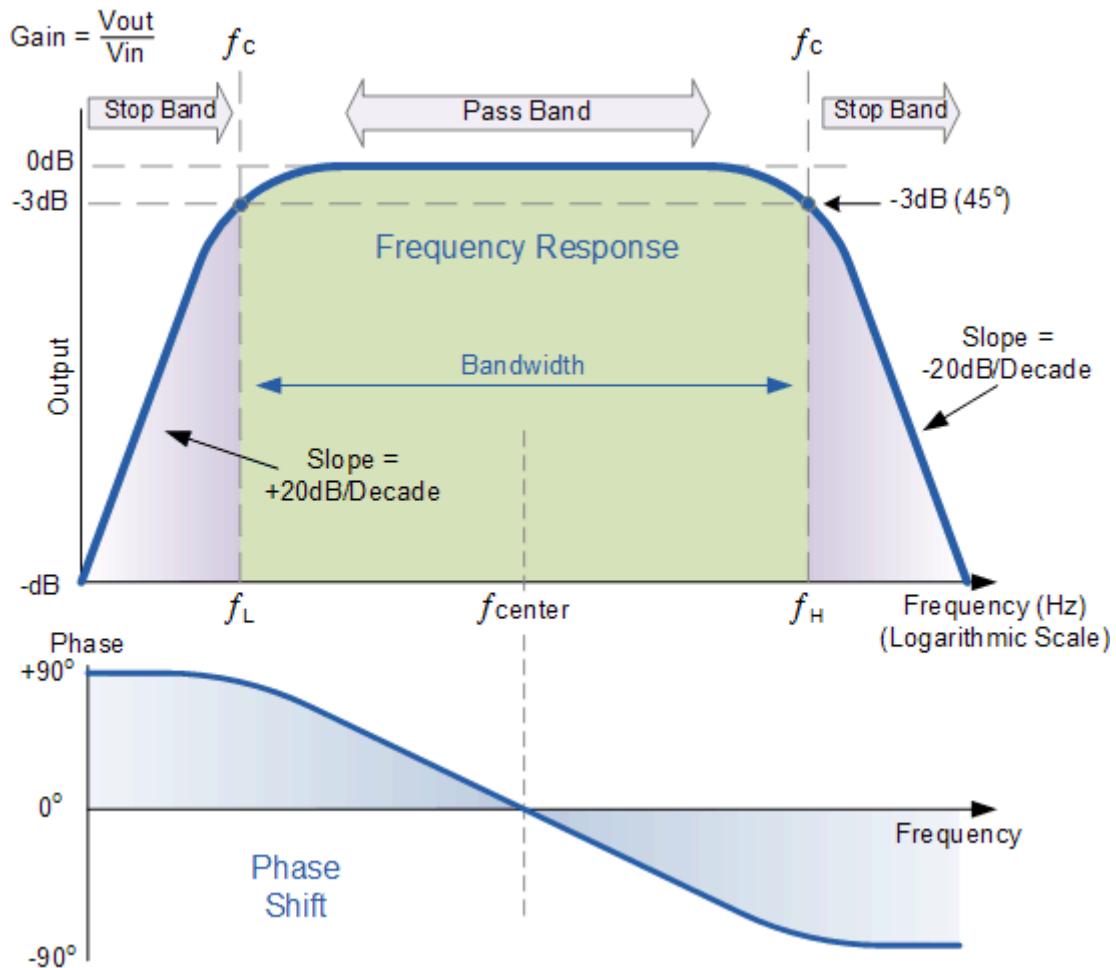


Figure 147: Frequency Response of a 2nd Order Band Pass Filter

6.2.3 Check for Impact of Loads

Signal attenuation due to the network loads can be of the order of 40 to 100 dB per kilometer. The main parameter determining the actual level of signal attenuation is the number of loads connected to the main line. As long as loads are evenly distributed over the main line, the relation between signal attenuation and distance can be considered to be approximately exponential. For the power line channel, the received average signal power can be modeled as a function of the distance between transmitter and receiver.

Depending on the country, the LV mains frequency voltage is 110 V to 230 V at 50 Hz or 60 Hz (phase to neutral) for LV lines. The common mode or zero sequence characteristic impedance for LV underground power cables is typically 10Ω to 50Ω , depending on the line current carrying capability and around 225Ω for overhead lines on cross-arms. For LV lines there normally are many branches, many PLC couplers and several hundred domestic and industrial appliances connected to the power line. As a result, the impedance seen on the power line varies significantly with time and frequency. In the 10 kHz to 150 kHz frequency range, the measured line impedance varies between 1Ω to 20Ω and tends to increase with frequency. The impedance of power lines in the 1 MHz to 30 MHz frequency range and found the impedance to vary widely from 10Ω to 300Ω , with an average impedance of about

50 Ω . Because of this wide variation in power line impedance and the time and frequency impedance variation of the loads connected to it, it is very difficult to obtain a low loss coupling and thus maximum power delivery of the PLC signals onto the power line without providing some impedance adjustment settings as part of the coupler design.

As can be seen from the output of the designed Signal Transmitter still the output of 12 Vpp cannot be obtained from the terminal. Also, the Line impedance and designed transmitter, receiver impedance must be considered in redesigning.

6.2.4 Product Level Upgrade

In narrowband PLC, performance is strongly influenced by signal attenuation, noise disturbances and interference. Attenuation starts with the coupling circuit. Losses due to mismatch of the network impedance to the coupling circuits can lead to an attenuation of 10 dB or more in Signal-to-Noise Ratio (SNR)

Adding of noise can be reduced by applying capacitors parallel with signal transmitting lines and match with line impedance. Choosing appropriate capacitors also important.

Stability of the signal generator and the phase locker should be considered, drooping the transmitting signal may cause code error.

The ideal PCB design starts with the discovery that a PCB is needed and continues through the final production boards. After determining why, the PCB is needed, the product's final concept should be decided. The concept includes the design's features, the functions the PCB must have and perform, interconnection with other circuits, placement, and the approximate final dimensions.

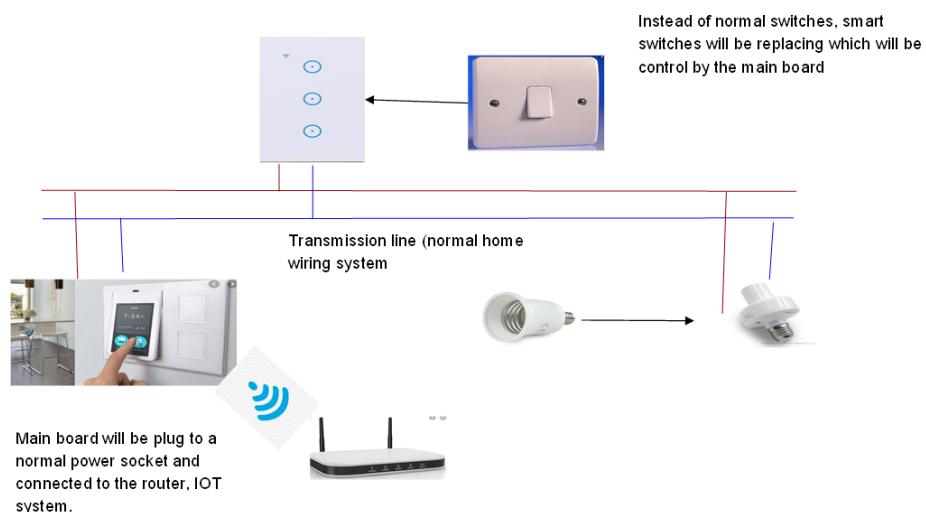


Figure 148: Expected Future Product

Designing of the main board and the Smart Plugs and 3D printing them, need to be done in future product.

7 Conclusion

Arranging tests is a must when doing a project in order to check whether hypothesizes that has been set are right or wrong. Also, when conducting such tests, results that has not been considered can be observed and that can lead for developments that was not planned. Arranging such tests improves the thinking pattern, pre planning skills and organizing skills of an engineer. At the end we have arranged 15 tests and for each test the observations and the conclusions of the previous tests has been used as inputs.

During the past course of the project, we were able to both determine the aspects that are required to develop the project as well as to increase the potential to answer the problems that arise within the work being done in the project. In the initial section of the project, we tried in an increasingly difficult manner to develop the coupler. The designing had to be rearranged for more than ten times. We also used a filter in order to actuate the plan. Although the expected results did not occur, these activities had huge effect on the success of the project, because each try, we had the opportunity to learn a new engineering aspect and led us to think in another path. In the end when the transformer used in the project was converted to a high frequency transformer the task became admiringly successful. This can be considered as a huge success in the path of the project.

For the initial tests, the project was done by using a signal generator and a spectrum analyzer. Both these are needed to be made by us in order to ascertain to the requirements of the project scope. For this two ICs were identified. It was also required to develop an oscillator, and for this the CD4046 IC was used. The main reason behind this choice is the availability of a V_{pp} value of 12V. This feature removed the requirement of adapting an extra amplification system. For the signal detector we used a phase locker LM567 in the first stage.

In the final stage LM567 have to be removed because it doesn't work as a frequency Synthesizer. So, for the demodulation CD4046 was used which a phase comparator is used for frequency synthesis. For the modulation CD4046 was used and Tip120 was used to step up modulated signal V_{pp} to 12V.

Finally, it can be stated that during this period of time we have been able to develop an IoT device, where a bit pattern is sent through the transmitter modem and the receiving is indicated by a LED. When the receiver identifies the relevant bit pattern, it energizes the relay and allows to get power form the plug base at the receiver. However, the distance complying with this activity is very small considering that we were only able to obtain a center frequency of 120 kHz. In the future we expect to develop a coupler to set the optimum frequency and obtain a much longer distance transmission through decreasing the attenuation. Hence, it can be stated that the final status of the project lies within the time plan of the project and hence we are satisfied with the observed results. However, as planned we are expecting this to be developed as an industrial level product and further increase the scope of the project thereby providing it more value.

Appendix

Codes and Application

Zip file – “Codes and Application”

Demonstrations

Demonstrations Folder - Videos and the Final Product Presentation

Datasheet of CD4046

Attachment 1

Datasheet of LM567 Tone Decoder

Attachment 2

Datasheet of TIP 120

Attachment 3

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