EENG 5550 HW 3 Report Template

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# Design

## Block diagrams

### Overall design

A diagram of a computer system

Description automatically generated with medium confidence

Figure 1-Example top module: FSM for Road Traffic lights

Overall component: FSM for Road Traffic lights

Parameters: FAST\_GREEN\_SLOW\_RED\_CLOCKS = 16'd5(fast road timer clock cycles),

FAST\_RED\_SLOW\_GREEN\_CLOCKS = 16'd10(Slow road clock cycles),

YELLOW\_CLOCKS = 16'd2(yellow clock cycles),

LEFT\_CLOCKS\_PER\_CAR = 16'd5(left turn clock cycles per each vehicle) ,

TCQ = 1 (1 clock cycle delay)

Input ports:

|  |  |  |
| --- | --- | --- |
| Port name | Bit width | Purpose |
| i\_clk | 1 | Clock – to change the states of FSM at the positive edge of clk. |
| i\_rst\_n | 1 | Reset to start the FSM when the reset is high |
| i\_r4\_car\_cnt | 4 | Input from the sensor i.e., the number of cars at the left turn |

Output ports:

|  |  |  |
| --- | --- | --- |
| Port name | Bit width | Purpose |
| o\_r1\_yellow , o\_r1\_red , o\_r1\_green , o\_r2\_yellow , o\_r2\_red , o\_r2\_green ,  o\_r3\_yellow , o\_r3\_red , o\_r3\_green, o\_r4\_yellow , o\_r4\_red , o\_r4\_green ,  o\_r4\_green\_l | 1 | Data outputs from the FSM for traffic lights green, red, and yellow of road1, road2, road3, and road4 and green light for the r4 left turn signal. |

Necessary intermediate signals:

|  |  |  |
| --- | --- | --- |
| Port name | Bit width | Purpose |
| r4\_left\_cars ,  r4\_left\_cars\_d; | 4 | To store the left turn cars sensor count in registers |
| curr\_cnt,  curr\_cnt\_d ; | 16 | To store the current cycle counter in registers |
| trig\_cnt | 1 | Counter trigger |

## Design Explanation

### Functionality

There will be 2 bidirectional roads, 1 vertical main road with a longer duration/timer and 1 horizontal small road with a shorter duration/timer. The

design will be implemented using FSMs for each of the traffic lights, having

states for each of the traffic light states (green/go, yellow/slow, red/stop).

The horizontal road also has the option for turning left and when the turning.

left option is active, its duration depends on the number of cars in the left.

lane. Assume timing information of all the lights in such a way as if thiscontroller is going to work in real life.

Module has a clock and sync reset of polarity negedge. The module takes only input of the number of cars going to left from road 4 from the microcontroller other than clock and rest. The output of DUT connects to 4 roads lights red, yellow, and green, here is the detailed explanation of FSM where these outputs get asserted. [11:56 PM, 4/11/2024] Santhosh Frd: when system is in reset the FSM will be in RESET state and all the roads will be showing RED light saying to stop the vehicles --> (reset release)FSM moves to RD1Y\_RD2R\_RD3Y\_RD4R state(road 1 and 3 YELLOW light) --> FSM moves to RD1G\_RD2R\_RD3G\_RD4R state (road 1 and 3 GREEN light) -->FSM moves to RD1Y\_RD2Y\_RD3Y\_RD4Y state(road 1 and 3 YELLOW light) -->FSM moves to RD1R\_RD2G\_RD3R\_RD4G state (road 1 and 3 GREEN light) --> RD1Y\_RD2Y\_RD3Y\_RD4Y --> RD1G\_RD2R\_RD3G\_RD4R.

and provided FSM is detailed diagram explaining the same.

# Results

## Generated Schematics

A screenshot of a computer program

Description automatically generated

Figure 3 – RTL Schematic of FSM of Road traffic lights

The above RTL schematic of FSM of road traffic lights shows the top module which has one clock, one reset, road4 car count signal, 4 red light signals, 4 green light signals, and 4 yellow light signals of all four roads which match with the information provided at the overall component inputs and output signals. Hence the generated schematic RTL is generated correctly.

Note: the overall RTL schematic is attached as a separate pdf.

## Waveforms

**Test Cases: I**

**ROAD 1 Active: (0 to 160 ns)**

A screenshot of a computer

Description automatically generated

Figure 5 – Test case 1 Waveforms

**Test Cases: II (160ns to 410ns)**

**ROAD 2 Active:**

A screenshot of a computer

Description automatically generated

Figure 5.1 – Test case 2 Waveforms

**Test Cases: III (410ns to 960ns)**

**ROAD 2 Left turn:**

A screenshot of a computer

Description automatically generated

Figure 5.2 – Test case 3 Waveforms

**Overall Test Cases Waveform:**

A screenshot of a computer

Description automatically generated

Figure 5.3 – Overall Waveforms

## Table/Calculations

### Overall Design

**Test Cases: I**

**ROAD 1 Active: (0 to 160 ns)**

* At reset time all red signals of 4 roads are set and other yellow and green signals are zero. Then Yellow signals of r3 and r1 are set for two cycles. After the 2 clock cycles, the green signals of r3 and r1 are set for 5 clock cycles at the time other roads are in red signal mode.
* From Test Case I Waveforms: At first, one clock cycle reset is set, and all 4 roads red signals r1\_red, r2\_red, r3\_red, and r4\_red are set remaining traffic signals are low. The next two clock cycles r1\_yellow, and r3\_ yellow are set remaining traffic signals are off except r2\_red, and r4\_red are set. And the next 5 clock cycles r1\_green, and r3\_ green are set remaining traffic signals are off except r2\_red, and r4\_red are set. The r1\_\* and r3\_\* signals are of Road1 and only r1\_green, and r3\_ green; r2\_red, and r4\_red are set which means Road1 is Active. Hence the generated waveform is correct, and the design works properly.

**Test Cases: II (160ns to 410ns)**

**ROAD 2 Active:**

* All the red signals of 4 roads are set and other yellow and green signals are zero at first. Then Yellow signals of r2 and r4 are set for two cycles. After the 2 clock cycles, the green signals of r2 and r4 are set for 10 clock cycles at the time other roads are in red signal mode.
* From Test Case II Waveforms: At first, all 4 roads' red signals r1\_red, r2\_red, r3\_red, and r4\_red are set remaining traffic signals are low. The next two clock cycles r2\_yellow, and r4\_ yellow are set remaining traffic signals are off except r1\_red, and r3\_red are set. And the next 10 clock cycles r2\_green, and r4\_ green are set remaining traffic signals are off except r1\_red, and r3\_red are set. The r2\_\* and r4\_\* signals are of Road2 and only r2\_green, and r4\_ green; r1\_red, and r3\_red are set which means Road2 is Active. Hence the generated waveform is correct, and the design works properly.

**Test Cases: III (410ns to 960ns)**

**ROAD 2 Left turn:**

* All the red signals of 4 roads are set and other yellow and green signals are zero at first. Then Yellow signals of r2 and r4 are set for two cycles. After the 2 clock cycles, the green signals of r2 and r4 are set for 10 clock cycles at the time other roads are in red signal mode. Then the input is given from the car count which is 1 then the r2\_yellow is set for 2 clock cycles and then r2\_red will be set. r4\_green\_l will be set for the number of cars X left turn clock time i.e., 1x5 = 5 clock cycles.
* From Test Case II Waveforms: input at i\_r4\_car\_cnt is 1. At first, all 4 roads' red signals r1\_red, r2\_red, r3\_red, and r4\_red are set remaining traffic signals are low. The next two clock cycles r2\_yellow, and r4\_ yellow are set remaining traffic signals are off except r1\_red, and r3\_red are set. And the next 10 clock cycles r2\_green, and r4\_ green are set remaining traffic signals are off except r1\_red, and r3\_red are set. Then the r2\_yellow is set for 2 clock cycles and then r2\_red will be set. r4\_green\_l will be set for 5 clock cycles. The r2\_\* and r4\_\* signals are of Road2 and only r4\_green, and r4\_ green\_1; r1\_red, r2\_red and r3\_red are set which means Road2 is Active with left turn. Hence the generated waveform is correct, and the design works properly.