

Design Of Two Stage CMOS Operational Amplifier in 28nm Technology

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Abstract — The paper discusses the design of two stage operational amplifier using miller compensation technique to increase the stability. This amplifier operates at a supply voltage of 1.8 V with 30 μ A current source and provides a DC gain of >40 dB, unity gain bandwidth of greater than 15 MHz, CMRR of ≥ 50 dB, phase margin of $\geq 60^\circ$, slew rate of ≥ 15 V/ μ s and power dissipation of ≤ 50 μ W.

Keywords — Miller compensation, slew rate, phase margin

I. REFERENCE CIRCUIT DETAILS

Today's market needs force the semiconductor industry to develop chips with higher stability, smaller sizes, and reduced power dissipation. Operational amplifiers are used in different circuits such as filters, comparators and data converters.

Two stage op-amps are highly used in present scenario due to their high gain and improved stability requirements of the circuit. The architecture used in first stage can be a differential op-amp, telescopic op-amp or folded cascode op-amp. The second stage of the two stage op-amp can be common source amplifier. Frequency compensation techniques are used to improve stability. Direct and indirect frequency compensation are two types of frequency compensation. Miller compensation or Direct Compensation have been used to compensate two-stage op-amps.

Parameters	Specifications
Technology	28nm
Supply voltage, V_{DD}	1.8V
DC Gain	40dB
Phase margin	$>60^\circ$
Unity gain frequency	15MHz
Slew rate	>15 V/ μ s
Power dissipation	<50 μ W
CMRR	>50 dB
I(current)	30 μ A
C_c	440fF

Transistor	Aspect ratio
Mn1,Mn2	2
Mp3,Mp4	13
Mn5	14
M1	14
Mn6	28
Mp7	55

II. REFERENCE CIRCUIT

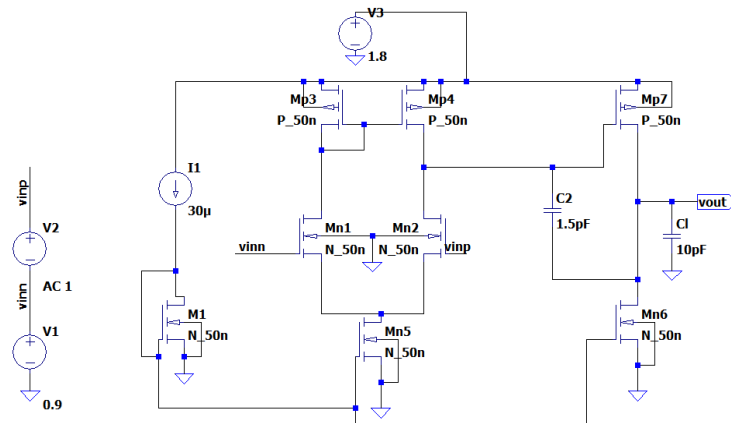


Figure 1: Two stage operational amplifier

III. REFERENCE WAVEFORMS

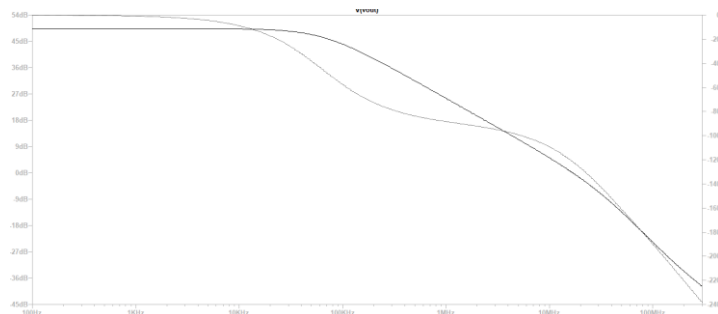


Figure 2 : AC analysis

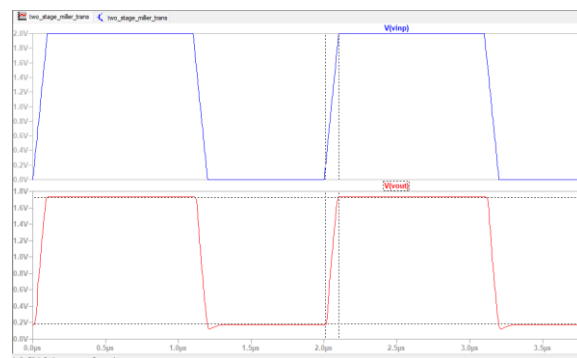


Figure 3: Transient analysis

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